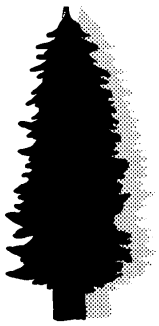

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Single-chip Performance of a GLAST Tracker Prototype Front-end ASIC GTFE64c

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Abstract

Performance of the prototype front-end ASIC GTFE64c for the GLAST tracker was investigated as a single, isolated chip mounted on a printed-circuit board specially designed for the tests and the measurements. Most of the tests were performed with test detectors or load capacitors attached to the electronics to simulate capacitive load on channel inputs in the real system. However, since electrical environment for the chip is different from one in the BTEM (Beam-Test Engineering Model) tracker, the measurement results will be different from the one obtained from the beam test at SLAC in 1999–2000. In this document the results of the measurements are described after a brief description of the test setup and the measurement methods.

Contents

1 Setup

A PC board to test a prototype ASIC of a GLAST front-end electronics chip GTFE64c was designed by E. Atwood and named LizBoard. On a LizBoard a front-end chip (GTFE64c) and a controller chip (GTRC/B) can be loaded with passive components such as bypass capacitors. A front-end chip on a LizBoard is controlled and read-out through a controller chip. A board is connected to a logic analysis system HP 16500A. The system sends out commands to a controller chip on a board and records digital signals coming out from the controller chip. A differential signal input of a front-end chip, EINP and EINN, was used to produce a calibration strobe in a front-end chip. To enable this input, EPON was kept logical high throughout the tests and measurements. A power supply HP 6626A was used to bias both chips and Keithly 237 to bias a detector ladder. Throughout the tests and the measurements, AVDD was fixed at 5 V, AVDD2 at 2 V, DVDD at 3 V, and detector bias at 100 V.

1.1 LizBoard

Two LizBoard's were loaded with a front-end chips (GTFE64c), a controller chip, and passive components. All the tests and the measurements in this document are performed on one of them. A skinny detector ladder is mounted on one of them and channels 16 to 47 are wire-bonded to a strip of the ladder for a capacitive load on channel input. The rest of 32 channel inputs are kept open. This front-end chip is called "chip 1" hereafter. On another board, a tiny piece of a PC board is glued to mount load capacitors. The piece has 5 traces[1] on it, so that a load capacitor can be mount each of them. These 5 traces are wire-bonded to channels 0, 16, 32, 48, and 63 to give a capacitive load on these channels. This front-end chip is called "chip 2" hereafter.

1.2 Skinny detector ladder

The skinny ladder consists of three skinny silicon strip detectors, each of which and has 32 strips at 194 μm pitch. The mechanical dimensions of the skinny ladder are identical to the detector ladders that were made of the detectors from a 6-inch wafer for the GLAST BTEM (Beam-Test Engineering Model) tracker, except for the ladder width. In fact, a skinny detector is a test piece built on a 6-inch wafer manufactured for a detector for the BTEM tracker.

1.3 Pico-probe and shield

A pico-probe model 12C was used for some of the measurements described later. To avoid pickups through a probe tip, a metal shield connected to the analog ground was always placed in front of a probe tip when the probe was in use. Several shields of different shape or of different sizes were tried and the one with the least pickup was chosen for the measurements. With the shield properly placed, pickups were kept below 2% in pulse height at shaper output.

[1] Similar traces are printed on LizBoard, but they were not used for the measurements in this document, because these traces happened to have a relatively large capacitive coupling to the ground layer of the board, which gives an extra capacitive load on a channel input.

2 Measurements and results

Performance of the analog section of the two front-end chips, chip 1 and chip 2 described in Section 1, was investigated on the LizBoard. In this section, methods of the measurements are briefly described and the results are listed. For common settings over the measurements, see Section 1.

2.1 Calibration of DAC's

Calibration DAC and threshold DAC of chip 1 and chip 2 were calibrated by measuring pulse height on the internal pads #13 (calibration DAC output), #12 (V_{thr}), and #11 (V_{ref}) for DAC values of 1, 8, 16, 24, 32, 40, 48, 56, and 63 both in the low range and in the high range. The pulse heights are fitted with a strait line to give a DAC gain for them. Listed below are the DAC gains obtained, where V_{cal} is step voltage of a calibration strobe, N_{caldac} is a DAC value set to the calibration DAC, and N_{thrdac} is one set to the threshold DAC.

For chip 1 (the one with the skinny detector ladder):

$$\begin{aligned} V_{cal} &= 12.21 + 5.863 \times N_{caldac} && \text{for calibration DAC; low range} \\ V_{cal} &= 28.61 + 24.70 \times N_{caldac} && \text{for calibration DAC; high range} \\ V_{thr} - V_{ref} &= 10.32 + 6.445 \times N_{thrdac} && \text{for threshold DAC; low range} \\ V_{thr} - V_{ref} &= 23.21 + 27.02 \times N_{thrdac} && \text{for threshold DAC; high range} \end{aligned}$$

For chip 2 (the one with load capacitors):

$$\begin{aligned} V_{cal} &= 10.88 + 6.184 \times N_{caldac} && \text{for calibration DAC; low range} \\ V_{cal} &= 26.51 + 25.41 \times N_{caldac} && \text{for calibration DAC; high range} \\ V_{thr} - V_{ref} &= 10.32 + 6.348 \times N_{thrdac} && \text{for threshold DAC; low range} \\ V_{thr} - V_{ref} &= 23.47 + 26.35 \times N_{thrdac} && \text{for threshold DAC; high range} \end{aligned}$$

Internal capacitors to inject charges were also calibrated for channels 0, 16, 32, 48, and 63 of chip 2 as follows. Lengths of fastOR signals (ToT, or time-over-threshold) were measured for various amount of charges injected through an 1.8-pF capacitor externally mounted on a channel input. It was found that ToT's depend linearly on charge amount for these channels for the range of 20 – 90 fC injections, and coefficients of the linear relationship were obtained. Then, charges in the similar range were injected through an internal capacitor by applying digital signals on the EINP/EINN pads with appropriate values set to the calibration DAC, and ToT's were measured. Again, ToT's depend linearly on step voltage, and coefficients of the linear relationship were determined. By combining the two linear relationship, step voltage is now related to injected charge, which gives a capacitance of the internal charge-injection capacitor. Table 1 lists the results.

Table 1. Internal capacitors for calibration strobe (chip 2)

Channel	Capacitance
0	43.4 fF
16	42.5 fF
32	41.4 fF
48	41.2 fF
63	40.8 fF

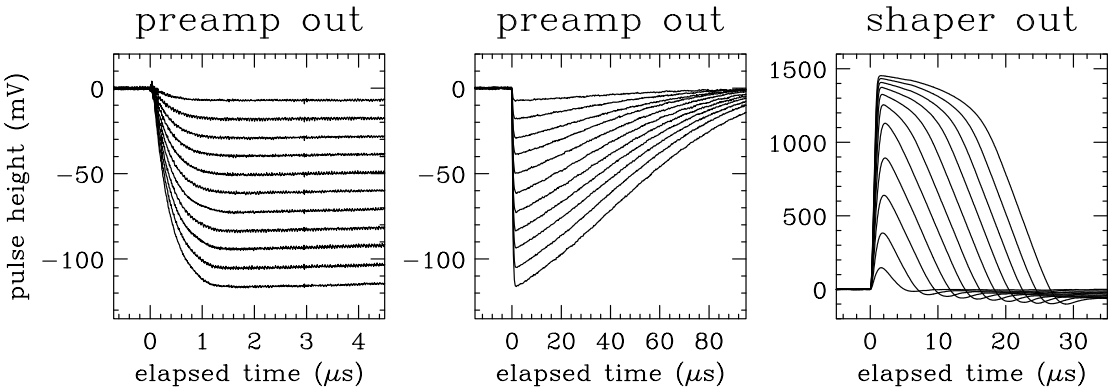

Fig. 1. Pulse shapes of the preamplifier output and the shaper output of channel 32 with 47 pF load on the input for various input charges (chip 2). Injected charges are approximately 1.2 fC, 2.8 fC, 4.3 fC, 5.8 fC, 7.4 fC, 8.9 fC, 10.4 fC, 12.0 fC, 13.5 fC, 15.0 fC, and 16.6 fC.

2.2 Pulse shape

Snap shots of pulse shapes at preamplifier output and at shaper output were taken for various amount of charges injected by reading out a Tektronix digital oscilloscope TDS 540. Channel 32 of chip 2 loaded by a capacitor of 47 pF was probed with a pico-probe and pulse shapes are averaged over 1000 pulses on the scope. Calibration DAC values to determine the amount of charge injected were 3, 9, 15, 21, 27, 33, 39, 45, 51, 57, and 63 and the DAC range was set to the low range. As the pulse injecting capacitor on the test input is calibrated as 41.4 fF, injected charges are approximately 1.2 fC, 2.8 fC, 4.3 fC, 5.8 fC, 7.4 fC, 8.9 fC, 10.4 fC, 12.0 fC, 13.5 fC, 15.0 fC, and 16.6 fC. Figure 1 shows the pulse shapes, indicating that pulse height of shaper output start saturating over about 10 fC, while that of preamplifier output is linear in the entire range of this measurement.

2.3 Amplifier gain

Preamplifier gains and shaper gains were measured by pico-probing the internal pads of chip 2 to measure pulse heights of preamplifier output and those of shaper outputs of channels 0, 16, 32, 48, and 63 of the chip with a load capacitance on its input. Charges were injected through the internal capacitors calibrated as in Section 2.1, and the calibration results listed in the section were used to calculate charge-to-voltage gains.

Amplifier gains were measured at 1.5 fC, to which a nominal threshold is set, and at 5.2 fC, which is close to a signal by a minimum ionizing particle (MIP) in a GLAST silicon strip detector. For 1.5 fC measurements, the calibration DAC's were set to 1, 2, 3, 4, and 5 of the low range, which corresponds to 0.9, 1.2, 1.5, 1.8, and 2.1 fC to inject. For a MIP measurements, they were set to 13, 14, 15, 16, and 17 of the high range, which simulate 4.6, 4.9, 5.2, 5.5, and 5.8 fC signals approximately. Tables 2 and 3 summarize the results.

Shaper gain of chip 1 was also measured with the skinny detector ladder wire-bonded to its channel inputs. It was measured one channel at a time by scanning a threshold voltage for each of the calibration DAC values listed above, namely, 1, 2, 3, 4, and 5 of the low range and 13, 14, 15, 16, and 17 of the high range. For each of the charge amount, pulse heights were measured by fitting an error function to a threshold scan curve, assuming that the median of an error function gives a pulse height of shaper output for that charge amount. The detectors were biased at 100 V and the total leakage current was 42–65 nA during the measurement. Shaper gain was

Table 2. Preamplifier gain of chip 2 with various capacitive loads

Load capacitance	Gain at 1.5 fC / 5.2 fC (mV/fC)				
	ch0	ch16	ch32	ch48	ch63
None	7.25/6.74	7.18/6.97	7.76/7.49	7.33/7.25	7.72/7.58
1.8 pF	6.88/6.81	7.41/6.94	7.76/7.30	7.56/7.02	7.25/6.49
23.5 pF	7.18/6.82	7.41/6.85	7.14/6.47	7.41/7.34	7.24/6.67
47 pF	6.81/6.50	7.70/7.18	6.59/7.06	7.33/6.93	7.01/6.99

Table 3. Shaper gain of chip 2 for various capacitive loads

Load capacitance	Gain at 1.5 fC / 5.2 fC (mV/fC)				
	ch0	ch16	ch32	ch48	ch63
None	147/166	162/176	159/179	156/178	153/170
1.8 pF	147/165	163/180	160/181	157/175	152/170
23.5 pF	145/165	157/176	159/171	152/167	148/164
47 pF	130/158	154/175	152/171	151/165	137/165

then calculated as a slope of a linear function fitting to the median-point thresholds against the amount of injected charge.

Figure 2 shows shaper gains of chip 1. Shaper gains of channels 16 to 47 were measured at 1.5 fC (the left four plots of the figure) and at 5.2 fC (the right four) with different capacitive loads to the channel inputs. All the channels of the front-end chip were measured their shaper gain for no capacitive load. In the figure, the top plots of the four on both sides (as indicated by "0 det") show those measured before the channel inputs were wire-bonded to the detector ladder. The second ones from the top ("1 det") show those with only one detector of the ladder is wire-bonded to the chip. The third ones ("2 det") show those with the second detector of the ladder wire-bonded to the first one which makes the effective ladder length two-detector length. And the bottom ones ("3 det") show those with all the detector wire-bonded to each other, which gives the same capacitive load to the channel inputs as to the ones in the BTEM tracker.

2.4 Threshold uniformity

Threshold uniformity over a chip is looked into as a byproduct of the gain measurements in Section 2.3. Figure 3 shows median-point threshold voltages of chip 1 over channels. Assuming charge injection capacitors should be identical to each other, their distribution over the chip indicates threshold uniformity of the chip. The standard deviations of the distributions range 7.1–7.4 mV for 1.5 fC injections and 20.7–21.1 mV for 5.2 fC injections.

2.5 Amplifier noise

Amplifier noise of chip 1 and chip 2 was measured with the skinny detector ladder (chip 1) and with load capacitors (chip 2) wire-bonded to their channel inputs. It was measured one channel at a time by scanning a threshold voltage with the calibration DAC set to 3 in the low range and 15 in the high range, where the former corresponds to charge injection of approximately 1.5 fC and the latter 5.2 fC. The detectors were biased at 100 V and the total leakage current was 42–65 nA during the measurement. For each of the charge amount, a threshold scan curve was fitted to by an error function, whose width (standard deviation) gives amplifier noise in pulse height at shaper output. Equivalent noise charge was then calculated by dividing it by shaper gain of that

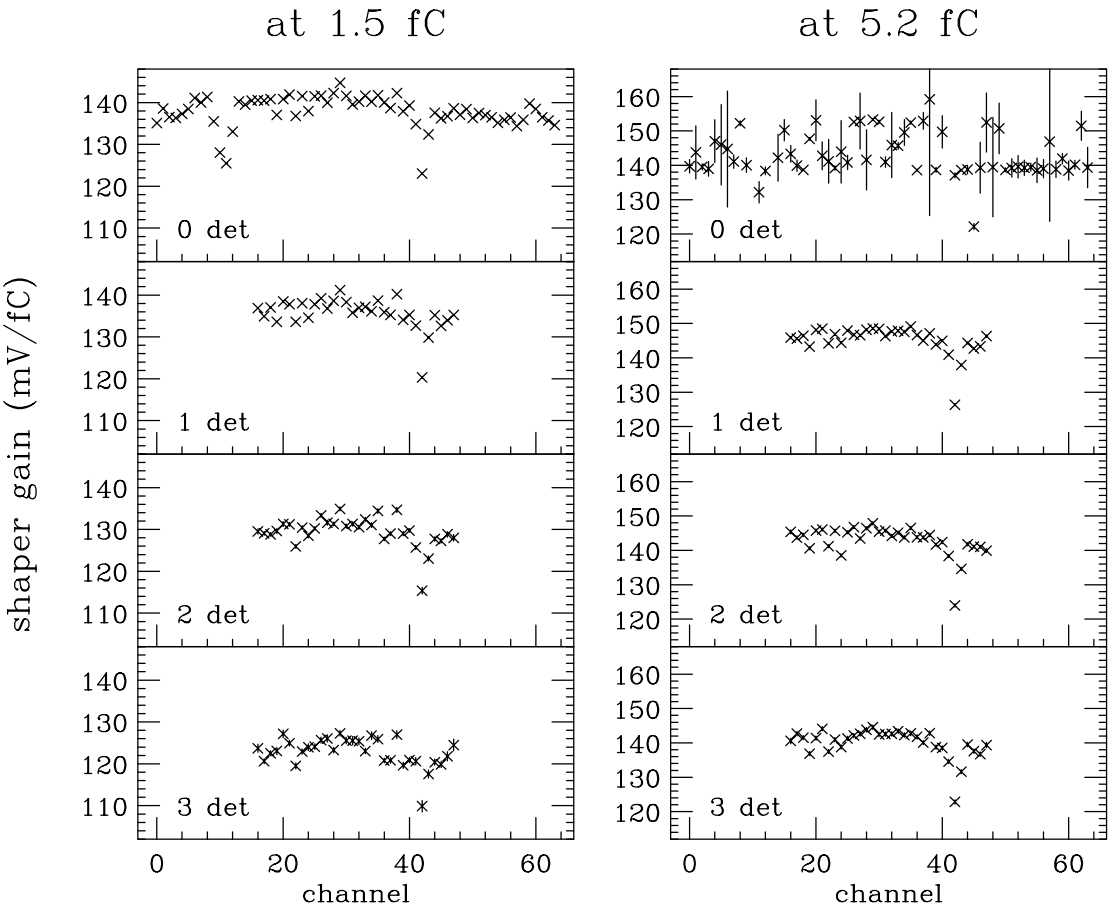

Fig. 2. Shaper gain of chip 1 with the skinny detector ladder wire-bonded at their input as a capacitive load. The left four plots show shaper gains measured at 1.5 fC and the right four plots at the 5.2 fC. In the plots, "0 det", "1 det", "2 det", and "3 det" indicate the electrical length of the ladder connected to the channel inputs of the front-end chip, where "3 det" corresponds to the full length of the ladder. For the plots with "2 det", for example, capacitive load to a channel input was two third of that of the BTEM tracker.

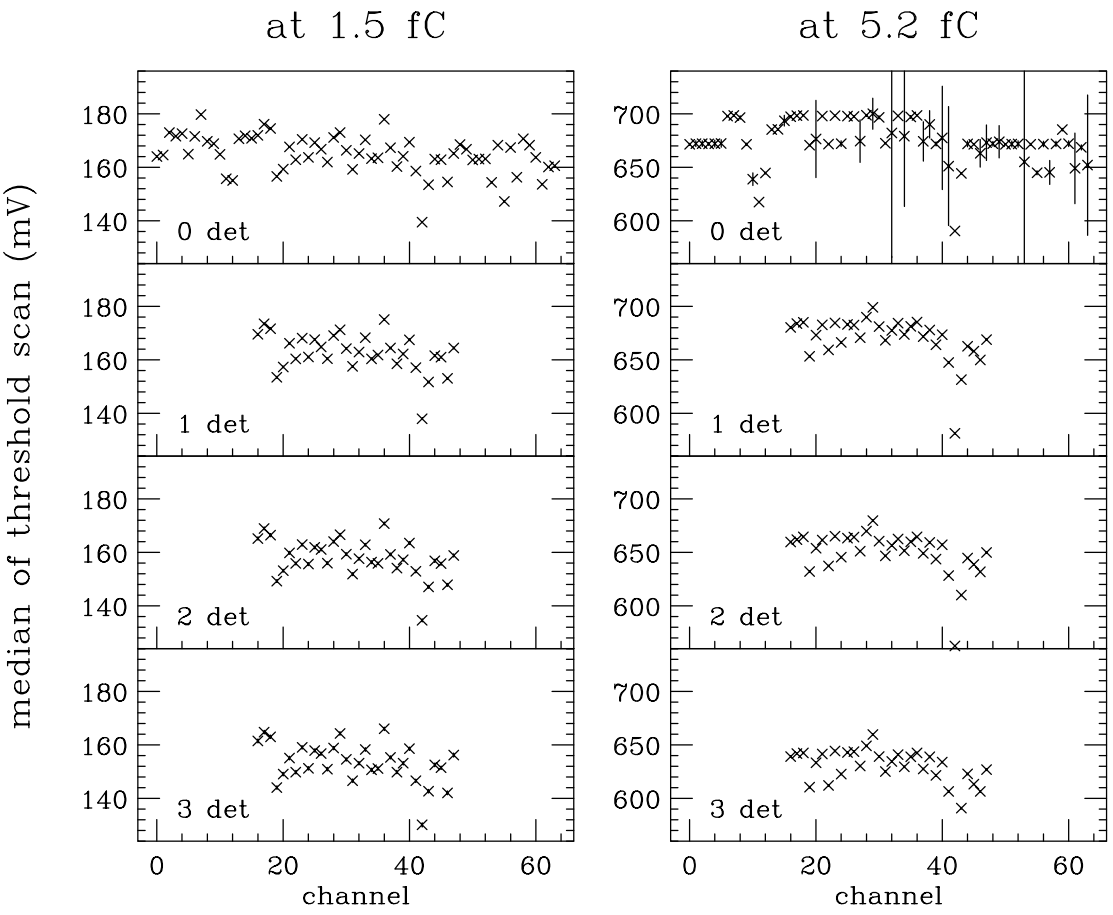

Fig. 3. Median-point threshold voltages of chip 1 with the skinny detector ladder wire-bonded at their input as a capacitive load. The left four plots show shaper gains measured at 1.5 fC and the right four plots at the 5.2 fC. In the plots, "0 det", "1 det", "2 det", and "3 det" indicate the electrical length of the ladder connected to the channel inputs of the front-end chip, where "3 det" corresponds to the full length of the ladder. For the plots with "2 det", for example, capacitive load to a channel input was two third of that of the BTEM tracker.

Table 4. Amplifier noise of chip 2 for various capacitive loads

Load capacitance	Equivalent noise charge at 1.5 fC / 5.2 fC (electron)				
	ch0	ch16	ch32	ch48	ch63
None	206/—	175/—	168/—	180/—	195/—
1.8 pF	220/—	198/—	193/—	213/—	222/—
23.5 pF	713/709	717/708	650/680	679/733	724/712
47 pF	1341/1255	1147/1148	1152/1164	1203/1223	1263/1223

Table 5. Effect of reverse bias of the first stage transistor (chip 2).

N-well	Source	Equivalent noise charge
2 V	2 V	1570 ± 23 electrons
5 V	2 V	1430 ± 24 electrons

channel obtained in Section 2.3. Table 4 lists equivalent noise charge of chip 2 with various load capacitors on the channel inputs, and Figure 4 shows that of chip 1 with the detector ladder of various electrical lengths. In the cases with small capacitive load, amplifier noise is smaller than a step size of threshold DAC in the high range, and noise could not be measured.

In the GTFE64c design, the first stage transistor of a channel is reverse-biased by applying a higher voltage to N-well (QVDD) than that to source (AVDD2) to improve noise performance. Improvement in noise performance was confirmed by measuring amplifier noise with and without the reverse bias. Noise was measured on channel 63 of the chip 2 with a load capacitor of 47 pF. The results are shown in Table 5. The table shows that noise would be higher by 9.8 ± 0.2 % without reverse-biasing the first stage transistor.

2.6 FastOR timing

Arrival times of fastOR signals were measured with chip 1 connected to the skinny detector ladder. Elapsed time between charge injection and leading (rising) edge of fastOR signals were measured by Tektronix digital oscilloscope TDS 640A. For each channel, 300 pulses were averaged in the oscilloscope's averaging mode and elapsed times at 10 %, 50 %, and 90 % of the full height of fastOR signals were measured with the charge injection time as the origin of time. The detectors were biased at 100 V and the total leakage current was 49 nA during the measurement. The results are shown in Fig. 5 with the 50 % times as the data points, and the 10 % times and the 90 % times as the end points of the error bars. The figure show that fastOR arrival times are uniform over a chip with timing jitter of ± 60 μs.

2.7 Time over threshold (ToT)

Characteristics of time over threshold (ToT) were investigated with chip 1 and chip 2 by measuring lengths of fastOR signals in various settings. First, lengths of fastOR signals were measured for a wide range of the amount of injected charge on chip 2. The results are plotted in Fig. 6. The amount of injected charge is calibrated by the results in Section 2.1. The ToT is almost linear up to 100 fC and saturates at around 100 μs. A notch in ToT is seen around 200 fC injection in the figure. The cause of the notch is not known yet. The charge amount does not correspond to saturation in shaper output nor saturation in preamplifier output. Second, threshold dependence of ToT behavior was looked into with chip 2. Fig. 7 shows plots ToT vs. charge amount with threshold set to 169 mV and 86.5 mV. The figure show difference in

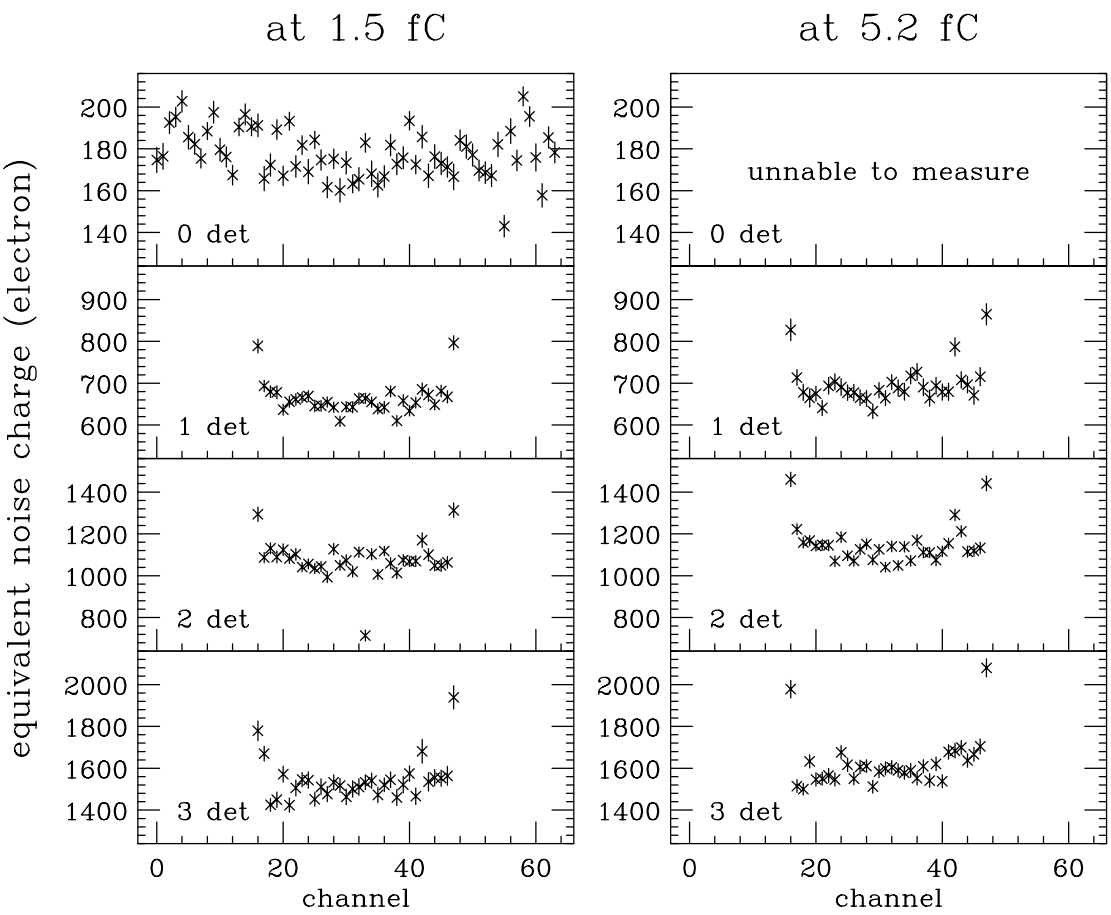

Fig. 4. Equivalent noise charge of amplifier noise at shaper output of chip 1 measured with the skinny detector ladder wire-bonded to its inputs as a capacitive load. The left four plots show amplifier noise measured at 1.5 fC and the right four plots at the 5.2 fC. In the plots, "0 det", "1 det", "2 det", and "3 det" indicate the electrical length of the ladder connected to the channel inputs of the front-end chip, where "3 det" corresponds to the full length of the ladder. For the plots with "2 det", for example, capacitive load to a channel input was two third of that of the BTEM tracker.

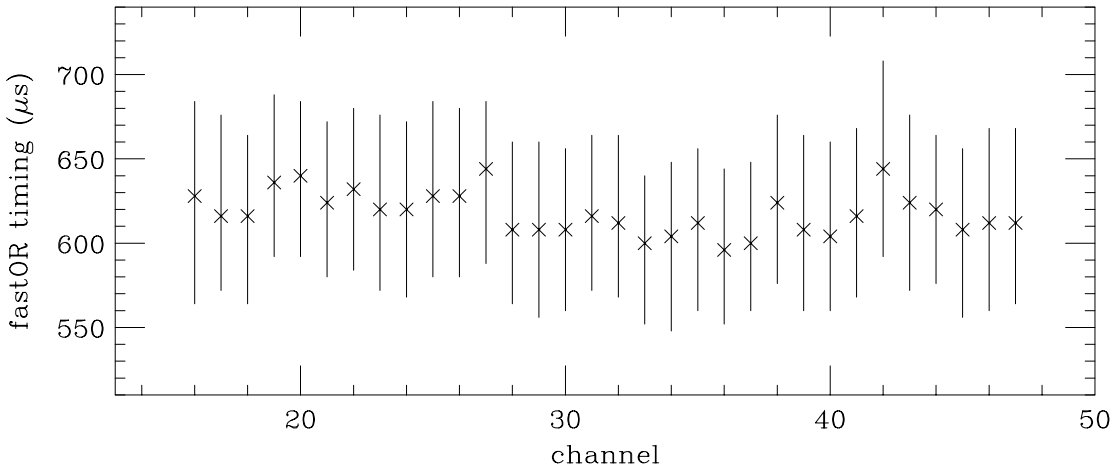

Fig. 5. Distribution of arrival time of fastOR signals over channels connected to a strip of the skinny detector ladder (chip 1), measuring from the time when charge is injected. Plotted are the averaged arrival times and error bars indicate timing jitters. The calibration DAC was set to 15 in the low range (about 1 MIP signals) and the threshold DAC was set to 25 in the low range for threshold of 169 mV.

Table 6. Time over threshold for two different capacitive loads (chip 2).

	ToT for 1 MIP[a] signals (μs)			ToT for 2 MIP[a] signals (μs)		
Channel	with 1.8 pF	with 47 pF	difference	with 1.8 pF	with 47 pF	difference
ch0	6.50	6.40	1.5 %	11.92	11.76	1.4 %
ch16	9.40	9.32	0.9 %	16.80	16.64	1.0 %
ch32	7.84	7.84	0.0 %	14.28	14.16	0.8 %
ch48	6.92	6.76	2.4 %	12.44	12.28	1.3 %
ch63	6.42	6.24	2.9 %	11.76	11.40	3.2 %

a) The calibration DAC was set to 16 in the low range for 1 MIP signals and 32 in the low range for 2 MIP signals.

threshold voltage affects largely at the low charge injection below 3 fC (see the bottom plots), but not very much at higher charge injection. Third, lengths of fastOR signals were measured with two different capacitive loads, 1.8 pF and 47 pF on channels 0, 16, 32, 48, and 63 of chip 2 for 1 MIP signals (the calibration DAC set to 16 in the low range) and for 2 MIP signals (the calibration DAC set to 32 in the low range). The results are listed in Table 6. The two ToT's of each channel for each signal size are identical to each other with a difference less than 4 % in length.

Finally, ToT distribution over channels were measured for 1 MIP signals (the calibration DAC set to 15 in the low range) and 2 MIP signals (the calibration DAC set to 33 in the low range). The threshold DAC was set to 25 in the low range, which gives 169 mV in threshold voltage. Fig. 8 shows the results on chip 1 and chip 2. The detectors were biased at 100 V and the total leakage current was 42 nA during the measurement on chip 1. Although some channels are connected to a load capacitor or a strip of the skinny detector ladder, such channels do not show significant difference from the other channels in the ToT distribution. This agrees with the result in the previous paragraph that ToT does not depend largely on capacitive load as shown in Table 6. However, the average in ToT over chip 1 is obviously different from that over chip 2. The

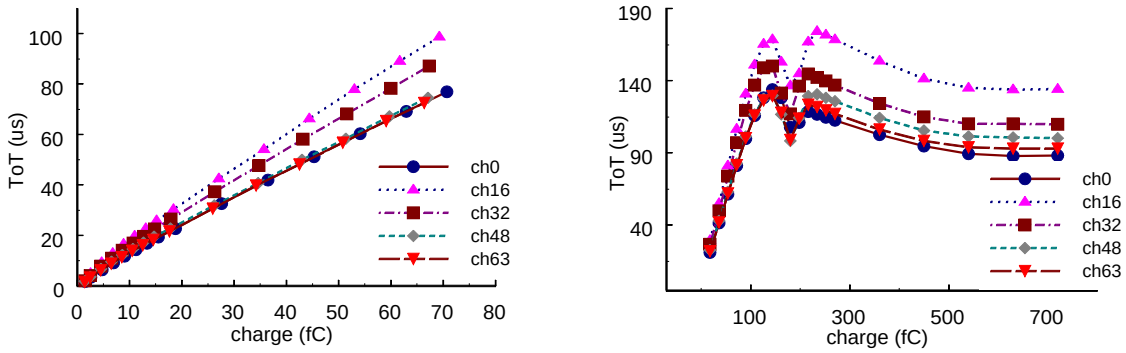

Fig. 6. Time over threshold (ToT) vs. injected charge in two ranges of charge amount injected (chip 2). The left plot shows ToT dependence on injected charged below 70 fC, and the right shows that up to 700 fC. The threshold DAC was set to 25 in the low range, corresponding to 169 mV equivalent to shaper output pulse height for 1.5 fC signals.

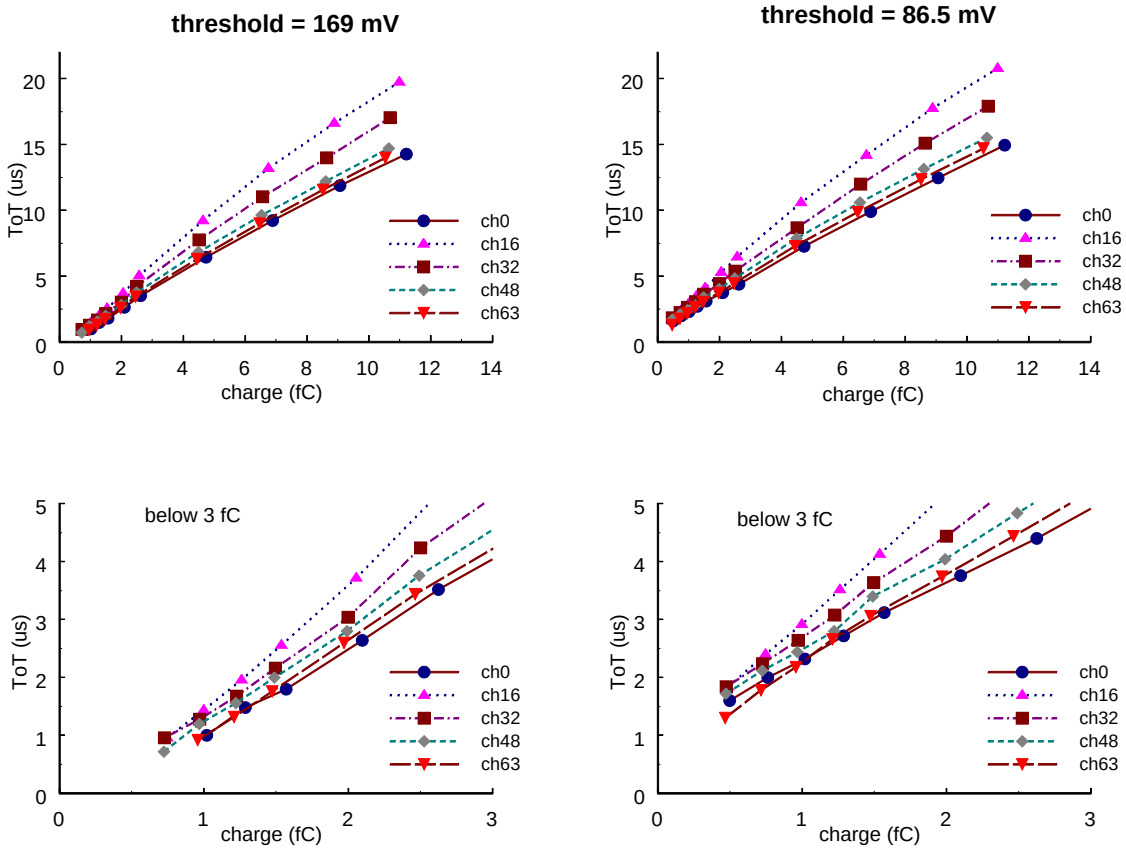

Fig. 7. Time over threshold in two threshold settings (chip 2). The left two plots show ToT vs. injected charge for threshold of 169 mV (the threshold DAC set to 25 in the low range), and the right two show that for threshold of 86.5 mV (the threshold DAC set to 12 in the low range). On each side, the bottom plot is expanded view of the top plot for charge injection below 3 fC.

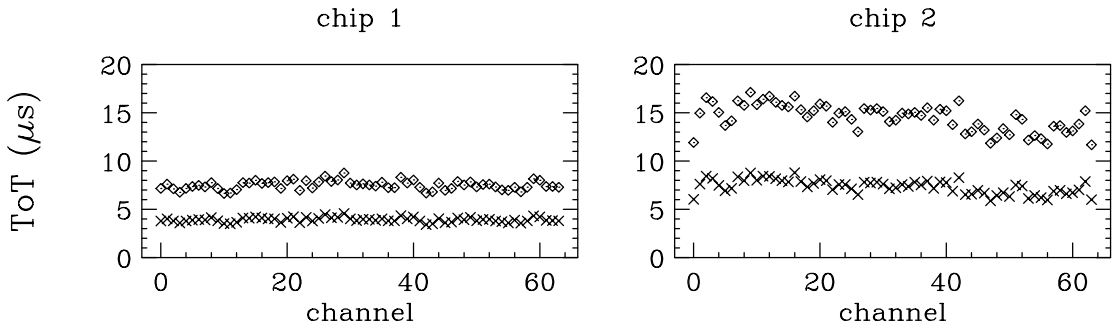

Fig. 8. Distribution of time over threshold of chip 1 (left panel) and chip 2 (right panel). In both panels, a cross is a ToT length for 1 MIP signal (5.2 fC in average with the calibration DAC set to 15 in the low range), and a diamond for 2 MIP signal (10.3 fC in average with the calibration DAC set to 33 in the low range). The threshold DAC was set to 25 in the low range for threshold of 169 mV. Channels 16 to 47 of chip 1 are wire-bonded to the skinny ladder, channels 0, 16, 32, 48, and 63 are loaded by a 47 pF capacitor, and the other channel inputs are kept open.

difference could be due to chip-to-chip variation in chip fabrication, although it is not conclusive from this measurement only.