GTFE16 User Guide

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Introduction

The GTFE16 chip is the first prototype of a front-end readout chip being developed at the Santa Cruz Institute for Particle Physics (SCIPP) for the GLAST silicon-strip tracker. It consists of 16 channels, each with a preamp, shaping amp, comparator, disable/enable flip flop, data latch, and trigger output. Bits may be shifted serially in and out of the disable register and the data register. The trigger output (IRQ) of the chip is a wired-OR of the 16 channels and must be pulled up with a 2 kohm resistor (included on the test board) to the digital 5-volt rail.

One clear shortcoming of the chip design is the IRQ output. This signal, which switches from 5 V to 0 with an appreciable amount of current, tends to jolt the amplifier inputs, resulting in instability if the threshold is too low. Operation of the chip with thresholds as low as about 1 fC to 1.5 fC is still okay. Going much below that, however, results in continual firing of the comparator. The problem is worse the larger is the detector capacitance and the larger is the capacitance on the IRQ output. It may be possible to reduce it by putting a resistor in series with the IRQ output, to limit its current and slow it down. That will result, of course, in a delayed trigger signal. We have not really played around with this much yet. We have, however, changed the design for the beam-test chip to have a differential IRQ output, with a low-voltage-swing, balanced current drive. The other digital inputs and outputs don't matter much, since they normally are not used while the amplifiers are actively acquiring data.

Test Board

The test PC board for the GTFE16 chip may be configured either with a single GLAST silicon-strip detector (240 μm pitch) or with a set of capacitors to simulate the detector load (both capacitance to ground and interstrip capacitance). The latter configuration is easier to deal with for testing the chip, since no detector bias is needed, and there is no added noise from leakage current. The capacitors loaded on the test board are 6.8 pF to ground on each channel, plus 12 pF to each of the neighboring channels. However, note that here "neighbor" refers to the next nearest channel on the chip, since only eight of the sixteen channels are wire bonded to the PC board. The channels with no connection exhibit very little noise, of course, compared with the others.

The configuration with a detector installed allows connection of all 16 channels but also requires the detector to be fully biased in order to operate the chip. The undepleted detector has far too much capacitance for the chip. The 500 μm thick GLAST detectors require about 140 V to deplete fully, but the capacitance is already low enough at considerably lower voltage (such as 50 V) that the chip can be operated successfully. The filter capacitors installed on the PC board for the detector bias are only rated to

100 V, but experience has indicated no problem at 140 V. Note that the bias must be applied such that the back side of the detector is at +140 V (or less) and the front side at ground potential. Getting that backwards may damage the chip as well as the detector. A supply with a current limit set at a few hundred μA is recommended for the detector bias.

The board with detector installed is milled out in a region beneath the detector to allow testing with electrons from beta sources. We have successfully carried out such tests with a Ruthenium-106 source (3.5 MeV endpoint). Strontium-90 (2.3 MeV) is also suitable and perhaps more readily available. We placed the source beneath the circuit board and a single scintillator trigger above the detector. Electrons that stop in the detector give enormous signals, so it is necessary to trigger on those that pass through and into the scintillator in order to get realistic signals.

Layout Error and Input Protection

The chip has a layout error that results in a low impedance from the 5 V supply to ground. We have repaired this by cutting the aluminum short with a UV laser. This results, however, in the input-protection bias floating for the channel input pads. That does not seem to cause any problem with the operation, although we are still evaluating whether it might cause an increase in noise. If desired, the input protection could be biased by connecting just one of the 16 channel input pads to a 5 V DC voltage source. That channel could not then be used for signals, of course.

Power Supplies and Bias Connections

The following power supplies are necessary for full operation of the chip (not including the detector bias supply). We have used common linear laboratory supplies, although batteries could also be used.

1. 5 V for AVDD and DVDD. In principle these should be separate supplies, but we have been doing most of the testing with a single 5 V supply. Using separate supplies might reduce the feedback from the IRQ (trigger) output. The chip functions fine (and at lower power) with this reduced to 4.5 V. It can even be reduced as far as 4.0 V, although that significantly increases the rise time of the analog output. In the quiescent state, you should expect the order of 300 μA of current to flow from this supply. The input labeled QVDD on the test board should also be connected to the same 5 V supply as AVDD.
2. 2 V for AVDD2. This should not be significantly less than 2 V, but it can be higher. In fact, it could be connected to AVDD. That just results in greater power consumption in the input transistor. The current drawn from this supply depends is programmed by the VI1 input, but with 160 kΩ in series with a 5 V supply for VI1, the nominal current from AVDD2 should be about 330 μA.
3. About 0.15 V across VTN and VTP, with VTP the more positive. The difference between these inputs controls the threshold of the comparator. Both inputs must be at least 0 V and not more than about 3 V. Otherwise the common mode voltage doesn't matter. No significant current flows into these inputs, so the voltages could be obtained by simply putting potentiometers across the 5 V or 2 V supply to form

voltage dividers. The actual threshold voltage that the comparator sees is increased from the difference VTP−VTN by a factor of about 1.5. It can be measured directly by a probe via the difference in voltage on the internal pads labeled VREF and THRESH. VREF, by the way, sets the quiescent output level of the shaper, which is seen by one input of the comparator differential amplifier. THRESH sets the DC level seen by the other input of the differential amp. VREF varies as the threshold voltage changes, but the difference THRESH−VREF is the actual threshold seen by the comparator and is only sensitive to the *difference* VTP−VTN. The amplifier gain is about 145 mV/fC with a 30 pF load, so a difference of 0.15 V on VTN and VTP results in a threshold of around 1.5 fC. These numbers should be considered approximate—you might try to measure the threshold on your own chip.

4. About 5 V on the VI1 input. This controls the bias current of the input transistor. The input on the chip sits at around 1.06 V, while there is a 162 kΩ resistor placed between the chip and the corresponding connector on the PC board. This results in about 24 μA of current programmed into the current mirrors. In each channel the current gets divided between the input transistor and the cascode transistor, with about 4 μA of it flowing through the cascode (the exact value varies with AVDD). The current can be increased by going above 5 V, or by reducing the resistance that we put on the PC board. It can also be lowered, which results in greater noise and a longer peaking time.
5. Optional: somewhere between 3.5 and 5 V on the VIR input. There is a 10 kΩ resistor between this input and the corresponding pad on the chip, so this voltage actually adjusts a current in the chip. It adjusts, in fact, the reset current of the preamp and hence controls the slope of the falling edge of the preamp output. If this input is left disconnected, the chip functions, but the preamp output tends to fall a little bit too fast (and the rate varies from chip to chip). The result is excessive undershoot in the shaper output. It is hard to control this reset current in the manufacture of the chip, because it is so small (around a tenth of a nanoamp, which is obtained by mirroring down the current that you input). It should be noted also that this tiny current is easily affected by light shining on the chip. Normal ambient room light does not have any noticeable effect, but a microscope light shining on the chip can easily double the current and result in a very large shaper undershoot. If you do connect this input and happen to have the current adjusted too high or too low, the amplifier will not function at all. The easiest way to set it is by probing the amplifier output, but it can also be adjusted by looking at the trigger output. Lower the voltage until the output goes dead (the preamp doesn't reset and becomes saturated) and then back off a little bit until it operates reliably. That will set the reset time at more-or-less its maximum possible value. The current flowing in or out of the input is tiny (a few μA), so the necessary voltage can be obtained by using a potentiometer as a simple voltage divider.

We have fully tested the chips installed on any test boards that we have distributed. However, the chips are somewhat fragile, especially in the presence of static discharge. The digital inputs are particularly easy to blow out, so care should be taken

when handling the test board and when making and breaking connections. In principle, the 5 V supply should be turned on first, before the other supplies and clock signals are turned on. Likewise, it should be turned off last. However, we have often broken this rule without any ill effects.

Connections Required to the Test Board for Operation

The connections required for full operation of the chip are shown in Figure 1. QVDD should be connected to the same supply as AVDD. The two grounds, AGND and DGND, are not really separate. They both connect to the substrate on the chip, and there

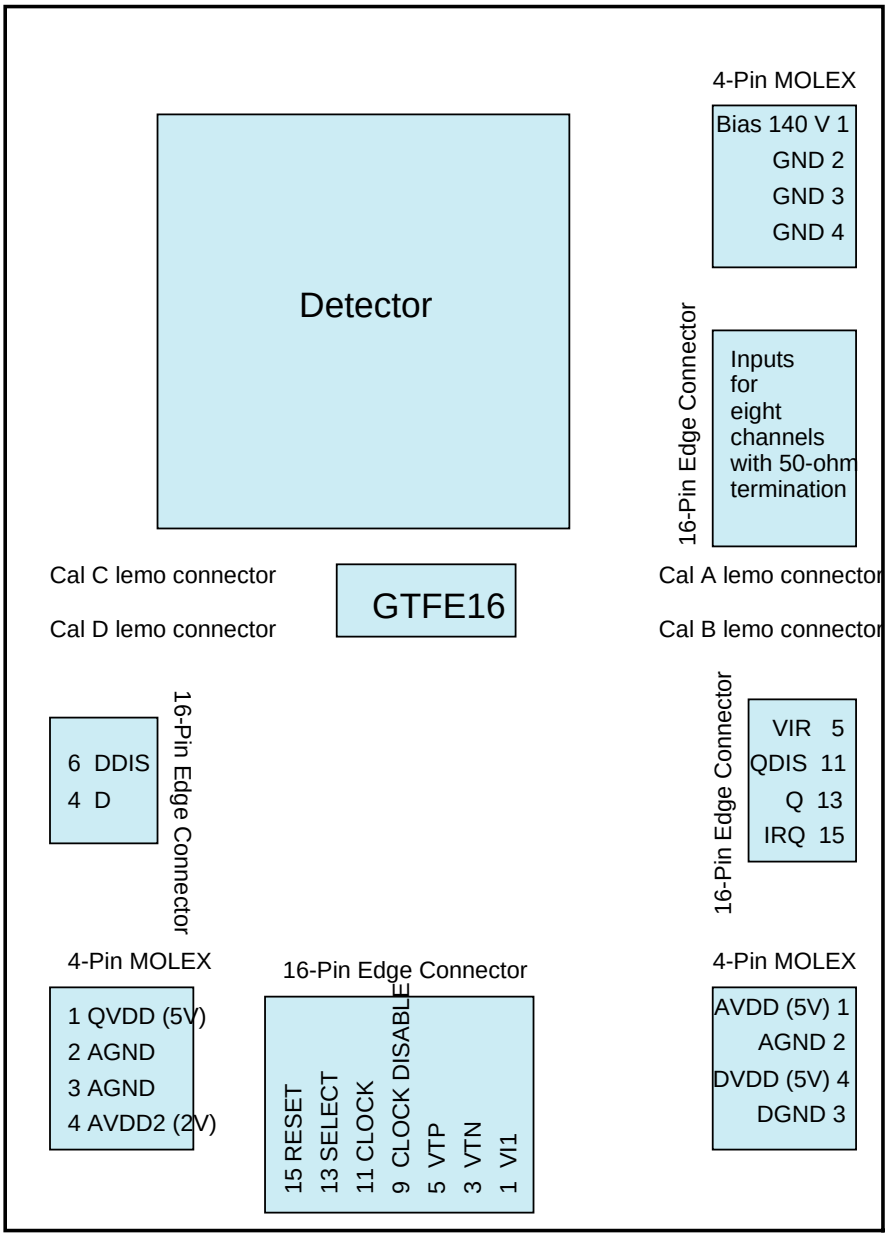

Figure 1. Arrangement of the connectors on the GTFE16 test board, showing the inputs and outputs that need to be used to operate the chip.

is a 10 Ω resistor between them on the PC board. Some experimentation with the grounds and with separate supplies for AVDD and DVDD could be done to see if it is possible to reduce feedback from the IRQ output into the amplifiers. The 16-pin connector for the channel inputs does not normally need to be used, and for boards with detectors installed it is not connected to the chip or not even installed at all. On all of the 16-pin connectors, at least half of the pins are connected to ground, but note that on the one on the left-hand side, the top row of pins is ground, while on the others it is the bottom row. The input labeled D and the output labeled QDIS are not used in normal operation, but they might prove useful for testing the digital section.

Testing the Chip by Injecting Calibration Signals

The analog half of the chip may be tested without making any of the digital connections, but only if an active probe is available for probing the internal pads. A passive scope probe has too much capacitance. On each channel there is a pad at the preamp output and another at the shaper output. We use a 7x magnification stereo microscope and a micromanipulator onto which is mounted a Picoprobe.

Table 1. Connection scheme for the four calibration inputs. Channels are numbered from right to left, looking in the direction from the chip toward the detector.

Calibration Input	Channels Connected
A	4, 8, 12, 16
B	3, 7, 11, 15
C	2, 6, 10, 14
D	1, 5, 9, 13

To get a test signal into the chip, connect a 50 Ω cable from a pulser to one of the four calibration inputs. Note that each input connects capacitively to four of the sixteen channels, as shown in Table 1. The capacitors are about 75 fF. The input signal is divided by approximately 10 on the PC board before going into the chip. Therefore, to get a 4 fC charge of the proper polarity injected, apply a step voltage from zero up to about +530 mV. A rise time of around 30 ns is appropriate for modeling a real signal. Keep the voltage high for about 100 μs, and then bring it back to zero. Ideally, bring it back down slowly, if you can control that. If not, be sure to wait a fairly long time afterwards (a millisecond is more than enough), to allow the chip to recover from the wrong-polarity signal.

In the case of the board with load capacitors installed in place of a detector, a test pulse can also be injected into individual channels via the external capacitors. Each of the eight inputs has a 50 Ω resistor to ground to facilitate this. We have used this feature in order to calibrate the internal calibration capacitors (on a different chip, but they should not vary more than a few percent). However, since the external capacitors are quite large, it is necessary to inject a very small step voltage in order to get a reasonable signal.

The preamp output should be negative-going in the case that a positive charge is input. It peaks on the order of 100 ns (depending on the detector capacitance) and then falls slowly back to the baseline over several microseconds (depending on the VIR setting). The peak amplitude is about 43 mV for a 6.7 fC signal (1-MIP in the 500 μm thick detectors). The shaper output is positive going, for the same input signal, and peaks in 1.5 to 2 μs. Its peak amplitude is about 970 mV for the same signal.

Digital Readout of the GTFE16 Chip

The simplest way to operate the chip without a probe is by observing only the IRQ output. To do so, however, first requires loading of the disable register. The disable register normally has all channels disabled upon power-up. Here is the procedure for loading it, assuming that some sort of digital pattern generator is available.

1. Hold the RESET input high at all times (just tie it to DVDD).
2. Connect one pattern generator output to the CLKD input (disable-register clock). This output should be a clock the will pulse for exactly 16 periods (we use a 2 μs period).
3. Connect a second pattern generator output to the DDIS input. To enable one channel, this output should go high for one clock period. For example, to enable channel 5, DDIS should go high for the 5th clock period out of the set of 16 clock periods. To see if the shift register is working, you can run the 16-clock sequence a second time and observe whether the bit come out of the QDIS output.

This sequence is illustrated in Figure 2. After it is executed, then a sufficiently large (*i.e.* above threshold) pulse input to Channel 5 (via Calibration Input D) will cause the IRQ output to drop from DVDD to GND. It will return to DVDD when the signal falls back below threshold. The time required for that depends on the size of the signal but is at least about 2 μs. If the threshold is too low, then the IRQ output will continue pulsing, as it feeds noise back into the amplifier input.

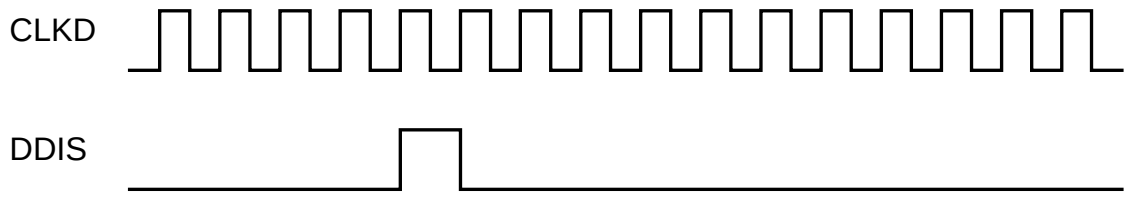

Figure 2. Digital waveforms needed as input in order to enable channel number 5. Time progresses from left to right in this figure.

Note that the digital inputs have pads on the PC board for termination resistors to be installed. We have not installed any such resistors, however, since we have been using short cables for controlling the chip. The output drivers on the chip are not very powerful and cannot drive a terminated cable. A short coax cable connected to a high-impedance scope input is okay. A scope probe is even better, of course. The longer the cable is that is connected to the IRQ output, the more will be the feedback of the signal into the amplifiers, and the slower the IRQ signal will switch.

A more elaborate way to operate the chip makes use of the data latch, as follows.

1. Hold RESET high at all times.
2. Enable all 16 channels by clocking CLKD 16 times while holding DDIS high. If some channels are known to be very noisy, you may want to enable only the good channels.
3. While holding the SEL input low, send a calibration pulse to the chip. Then, in about 2 μs, send a single pulse to the CLOCK input. This latches the comparator outputs. To be more authentic, you could use the IRQ output to generate this clock. In fact, if you are looking at real asynchronous data, such as from a beta source, then you must make use of a coincidence of the IRQ output with the external scintillator trigger to provide the clock for the latch.
4. After the data are latched, switch the SEL input to high. Then send at least 15 more pulses to CLOCK to shift the data out the Q output. To test this shift register, you can clock bits into the D input and then on out the Q output. Otherwise, tie the D input to ground in order to reload the register with zeroes as it is read out.

This scheme is illustrated in Figure 3 for the case that Calibration Input B is pulsed, resulting in hits on channels 3, 7, 11, and 15.

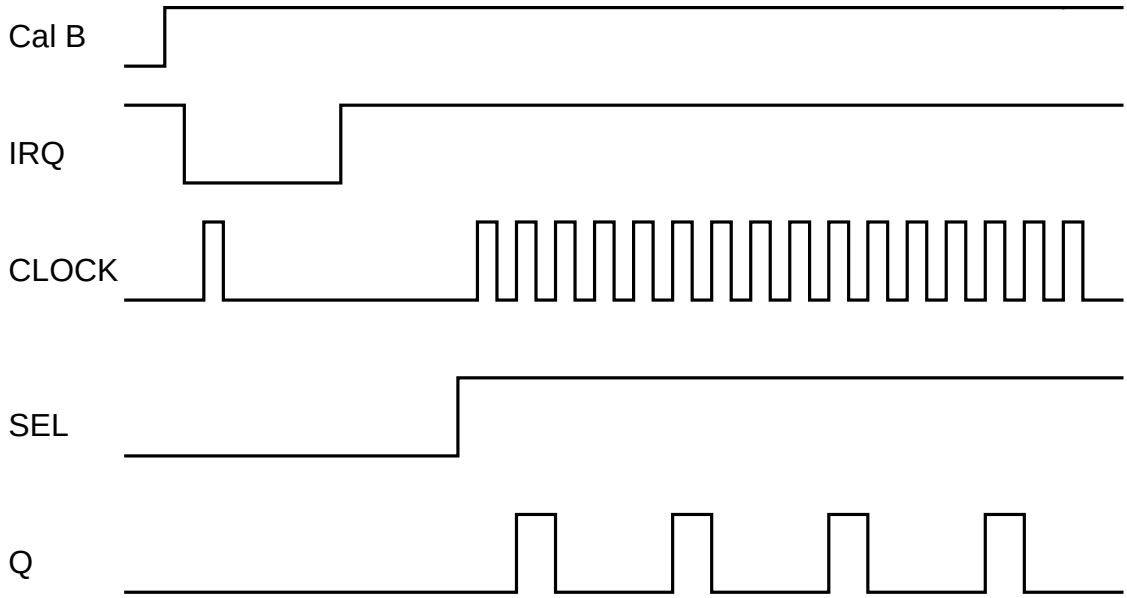

Figure 3. Timing diagram for readout of the chip with all channels enabled and a pulse introduced into Calibration Input B. The comparators for channels 3, 7, 11, and 15 fire. The 16 comparator outputs are latched and then shifted out the Q output.

Note that the content of the register for the first channel is visible at Q as soon as the data are latched. Hence the first clock pulse sent after switching SEL makes the content of channel two visible at Q, and so forth.