

# GLAST Tracker Action Items

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<b>Task ID</b>	2	<b>Project ID</b>	1		
<b>Task Description</b>	Fix SSD strip pitch				
<b>Lead</b>	Hartmut Sadrozinski				
<b>Open-Date</b>	<b>Action-ID</b>	<b>Action Description</b>	<b>Person-Responsible</b>	<b>Close-Date</b>	<b>How Closed</b>
3/29/00	30	Derive a specification on Signal/Noise for the tracker.	Hartmut Sadrozinski	4/12/00	Hartmut wrote up a note on signal-to-noise issues. This will be used to formulate a spec in the tracker requirements document.
4/12/00	38	Call Taka to arrange a meeting to organize work on the efficiency measurements.	Wilko Kroeger		
4/12/00	34	Communicate with Steve Ritz about the science implications of a change in pitch.	Robert Johnson	4/13/00	Spoke to Steve on the phone. At the 15% level we don't expect to fall off of any cliffs. He still is concerned about the loss of psf at highest energies.
4/12/00	33	Send configurations to Guido and Takashi for comparative electric field calculations near the detector implants.	Hartmut Sadrozinski		
4/12/00	32	Measure at the detection efficiency for inclined hadrons in the beam-test data.	Robert Johnson		

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**Task ID** 7                                  **Project ID** 3

**Task Description** Research adhesive for edge gluing of detectors.

**Lead**

Open-Date	Action-ID	Action Description	Person-Responsible	Close-Date	How Closed
3/7/00	2	Test UV curing adhesives for detector edge gluing before finalizing the jig design.	Eduardo		
3/7/00	1	Contact Hiroshima about using some of the 9.5cm square detectors from Hamamatsu for testing ladder assembly methods.	Hartmut Sadrozinski		
4/19/00	40	Work out a strategy for the use of mechanical samples in the near term.	Gwelen and Eduardo		
4/25/00	43	Investigate localized heat curing as fallback to UV glue	Ossie		
4/25/00	42	Write ladder requirements document.	Eduardo		
4/25/00	41	Complete drawings of the ladder gluing jig and glue dipping apparatus	BJ and John		
4/25/00	44	Measure flatness of mechanical samples.	Ossie		

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**Task ID** 15                                  **Project ID** 5

**Task Description** Redo the layout of the hybrid PC board.

**Lead** Robert Johnson

Open-Date	Action-ID	Action Description	Person-Responsible	Close-Date	How Closed
3/29/00	26	Make a drawing of the hybrid with 7 screw holes, plus 2 by each connector.	BJ	4/3/00	BJ made the drawing and sent to Robert and Gwelen.

3/29/00	28	Check prices for thermal vacuum chambers from commercial vendors.	John Broeder	
3/29/00	29	Take a look at what Peter Michelson has in terms of vacuum equipment that we could use.	Hartmut Sadrozinski	4/5/00 Hartmut looked at the piles of stuff in HEPL. It is not organized, so some effort would be required to use any of it. Peter may be able to supply a technician to put something together for us if we deliver a specification.
3/29/00	27	Search around SLAC for a suitable vacuum chamber.	John Broeder	

**Task ID** 10 **Project ID** 8

**Task Description** Thermal testing of ladder/face-sheet assemblies

**Lead** Gwelen Paliaga

Open-Date	Action-ID	Action Description	Person-Responsible	Close-Date	How Closed
3/22/00	13	Obtain specifications for the required survival temperature range.	Martin Nordby	4/12/00	Operation: -10C to +25C, testing to 10C beyond in both directions. Survival: -20C to +40C, testing to 10C beyond in both directions.
3/29/00	31	Get more information from Lockheed on the survival temperature range.	Martin Nordby	4/12/00	-20C to +40C, with testing to 10C extra in each direction.
4/5/00	9	Send the I vs t Labview program to Gwelen at UCSC	Erik Swensen	4/5/00	The program was put on the web.
4/5/00	10	Find somebody to prototype a lead-C laminate with prepreg carbon sheets between many layers of thin lead foils.	Robert Johnson	4/6/00	Guido, at Trieste, agreed to work on this.

4/5/00	8	Send a partial sample of the Kapton bias circuit used in the BTEM to Eric Ponslet	Gwelen Paliaga	4/5/00	Sample was sent to Eric.
4/5/00	14	Make 3 test ladders: 1. 300um C with Si glued in patches 2. Same but Si glued over full area 3. Add 75um C between Pb and Kapton	Gwelen Paliage		
4/12/00	35	Analyze representative C-Pb sandwiches and summarize the results in a report. Included will be 300um C/3.5% Pb/75um C, since that is what we have materials to construct at present.	Eric Ponslet		
4/12/00	36	Talk to Ed Garwin about making the CTE (and modulus) measurements on C-Pb structures at SLAC.	Eduardo		
4/12/00	37	Send information on the BTEM 75um carbon face sheets to Eric.	Martin Nordby		
4/12/00	39	Put the 38-cm tray drawings on the Hytec web site and make them available to SLAC and UCSC.	Erik Swensen	4/14/00	Erik sent out an email with information on how to access their web page.

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**Task ID** 17 **Project ID** 9

**Task Description** Convert the layout of GTFE64 cells from Cadence to Tanner.

**Lead** Vallon Chen

<b>Open-Date</b>	<b>Action-ID</b>	<b>Action Description</b>	<b>Person-Responsible</b>	<b>Close-Date</b>	<b>How Closed</b>
3/13/00	3	Test the conversion of layouts from Cadence to Tanner	Vallon Chen		

3/13/00	4	Finish the layout of the front-end and digital block test chip and submit to MOSIS.	Vallon Chen
3/27/00	24	Finish the layout and LVS of the analog/digital test chip.	Vallon Chen
4/3/00	16	Review the calibration system design for the new test chip.	Ned Spencer
1/13/00	5	Explain to the ASIC group the design of Vallon's SEU-hard cell.	Vallon Chen
3/13/00	7	Simulate Vallon's rad-hard cell and Rockett cell in Tspice	Ned Spencer
3/13/00	6	Explain the Rockett SEU-hard cell design to the ASIC group.	Ned Spencer
3/27/00	23	Simulate the two SEU hard cells in S-Spice.	Ned Spencer
5/3/00	17	Find publications on NRL laser system for SEU testing and give to Ned.	Hartmut Sadrozinski
3/27/99	22	Try out the Tanner LVS.	Ned Spencer
3/27/00	21	Introduce the planned logic changes into the command decoder schematic and do the logic simulation in Viewsim.	Robert Johnson
4/3/00	15	Use the Tanner place and route first on the unmodified cells and check with LVS.	Ned Spencer
5/3/00	18	Prepare an EDIF schematic for Tanner to try to input into S-Edit	Robert Johnson
3/27/00	25	Start testing the translation of the layout from Cadence to Tanner	Vallon Chen

3/27/00 20 Talk to the Japanese collaborators about holding a heavy ion beam test for latchup and SEU studies in August 00. Hartmut Sadrozinski

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**Task ID** 24 **Project ID** 11

**Task Description** Make noise measurements on the BTEM tower electronics with and without concurrent readout.

**Lead** Wilko Kroeger

<b>Open-Date</b>	<b>Action-ID</b>	<b>Action Description</b>	<b>Person-Responsible</b>	<b>Close-Date</b>	<b>How Closed</b>
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4/5/00	11	Test the noise occupancy in the presence of the ACD power supplies and while using the Perugia test power supply.	Wilko Kroeger		
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4/5/00	12	Measure the TOT width distribution using an oscilloscope	Wilko Kroeger		
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**Task ID** 40 **Project ID** 15

**Task Description** Tower thermal analysis and wall design.

**Lead** Erik Swensen

<b>Open-Date</b>	<b>Action-ID</b>	<b>Action Description</b>	<b>Person-Responsible</b>	<b>Close-Date</b>	<b>How Closed</b>
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3/27/00	19	Review the electronics thermal requirements, to revise the specification for the maximum operational temperature.	Robert Johnson	4/14/00	25C operational upper limit. Hartmut's analysis shows some loss of efficiency only in worst-case conditions: end-of-life and 5X expected radiation dose with this temperature. A lower temperature spec will be too expensive and constraining on the thermal design.
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