GLAST Tracker Issues

Task ID 1 **Project ID** 1

TaskDescription Fix overall Instrument dimensions and fix Tracker SSD size.

Lead Martin Nordby

Issue ID	Issue Description	Resolution	Action ID
10	Is there enough room around the sides for the ACD?		0
11	How wide an interstrip gap can be tolerated with regard to breakdown?		0
12	Is the tracker power reserve sufficient?		0
13	Impact on the PSF and science.		0
14	Width of traces on the fanout circuit and wire bonding issues.		0
15	Number of channels in the Fast-OR and occupancy requirements.		0
16	Capacitance vs strip pitch and width and noise implications.		0

Task ID 4 **Project ID** 2

TaskDescription Finalize the detector mask design.

Lead Takashi Ohsugi

Issue ID	Issue Description	Resolution	Action ID
6	Larger DC pads for probing implants?		0

Issue ID	Issue Description	Resolution	Action ID
7	Two AC pads per strip, one for probing and one for bonding?		0

Task ID 9 **Project ID** 3

TaskDescription Test methods for applying adhesive to the detector edge. Choose the best.

Lead Eduardo

Issue ID	Issue Description	Resolution	Action ID
21	Edge dipping vs automated syringing		0
22	Prevention of drips on the underside of ladders.		0
23	Optimal gluing technique to hold constant gap, bond strength, wetting.		0
24	Spraying vs damming vs dipping.		0
25	Hard epoxy vs soft silicone		0
26	Could encapsulation be eliminated? Concern about conductive particulates.		0
27	Need test pieces for this development work.		0
28	How can we encapsulate the wire bonds from detector to kapton fanout?		0
113	How many, and what type of mechanical sample SSDs should be purchased now?		0
115	Does edge gluing result in too many shorts between detectors. Is this an important issue for our system?		0

Task ID 16 **Project ID** 4

TaskDescription Perfect the method for establishing and controlling the space between detectors and bias circuit.

Lead

Issue ID	Issue Description	Resolution	Action ID
2	Why is the planarity of the BTEM silicon planes so poor? The gluing procedure needs more study.		0
5	Bond thickness for attachment of silicon to Kapton. Should it be increased to 4 mils?		0
17	Is silver-loaded epoxy compatible with aluminum on SSD?		0
18	Does epoxy creep under shear of axial load?		0
19	Can carbon loading be used instead of silver?		0
20	Can only room-temperature cure be used?		0
56	How should detectors be clamped during adhesive curing?		0
58	Improve protection of the tray corners.		0
116	How much silver-loaded epoxy can we tolerate in the tracker volume? Should we use two adhesives, one loaded and one not?		0

Task ID 13 **Project ID** 5

TaskDescription Prototype and test the new corner scheme for the detector-electronics interconnect

Lead Gwelen Paliaga

Issue ID	Issue Description	Resolution	Action ID
1	Should the dimensions of the hybrid corner piece be modified with respect to the current drawings?		0

29	Bonding pad size for the kapton strips should be larger to facilitate wire bonding. If the pitch is large, perhaps the traces can be fanned in.		0
30	Cleaning and preparation of the metal traces prior to wire bonding.		0
31	Gold body vs plating for the traces (the latter will require trimming of traces)		0
52	Standoffs for the kapton readout cables?		0
57	How will the hybrid be aligned to the closeout, especially to ensure a uniform height for the wire bonding.		0
59	Use the connector to program the GTRC address. This will require a 37-pin connector.		0
60	Kapton cables and connectors must move away from the corner.		0
61	Hard encapsulant vs compliant.		0
62	Leave adequate clearance around screw holes.		0
63	Align with pin holes or off of edge?		0
65	Adhesive needs to be removable.		0
66	Take back the 10 mil in space given up at one time with respect to the BTEM design?	YES	0
67	How many screws are needed for the hybrid now?		0
68	A means is needed to facilitate handling of the board once all the parts are on.		0
69	How will the board be clamped down during work?		0

70	Allow room for cover dismounting with risking damage to the components.	0
71	A solder mask MUST be used this time, leaving open solder points and wire bonding points. Be careful to leave open space for wire bonding sufficiently far from the chips.	0
72	Widen traces, where practical, to 8 mils.	0
73	Keep the bonding pattern identical for each chip, as much as possible.	0
74	Layout address pads such that the bond pattern is the same for each chip. This means that the traces and vias must address the chip.	0
75	Increase clearances in areas that had problems with bridging	0
76	Pattern AVDD2 and GND plane such that current flows through a neck to a single ladder.	0
77	Make a small test piece together with the hybrid, for practice bonding and bond testing.	0
78	Replace the inductor/resistor combination with a filter chip.	0
79	Maximize the trace widths at wire bond locations.	0
80	Follow NASA (JPL) guidelines and rules for board layout and coupon production.	0
107	How well will double-sided or transfer tape hold up in the space environment?	0
108	How much pressure is needed to bond the hybrid to the closeout with tape, and can the closeout take the force?	0

Issue ID	Issue Description	Resolution	Action ID
109	Can a commercial company fabricate the right-angle interconnect, rather than us doing it in house?		0
110	Should the right-angle interconnect have a lip sticking out over the tray, up close to the detectors, to give more room for gluing on the Kapton piece?		0
111	Be sure that everybody and all drawings are in agreement that we are NOT removing 10 mils of clearance between hybrid and closeout with respect to the BTEM design.		0
64	What thermal conductivity is needed?		13

Task ID 22 **Project ID** 6

TaskDescription Detailed CAD layout of the Kapton bias circuit

Lead

Issue ID	Issue Description	Resolution	Action ID
4	Keep in mind the need for uniform support of the detectors on glass beads, given that the traces then to be higher than the remainder of the circuit.		0
32	Break the ground plane into 4 separate circuits, one for each ladder, as was already done for the detector bias.		0
33	At least 2 bonding locations for each ground circuit and each bias circuit.		0
34	Need better alignment method for installation onto the tray (trimming with razor blade will not be acceptable with carbon trays).		0
35	Keep the grounding trace on the ladder far end from going off the edge of the tray (this was a problem in the BTEM).		0

Issue ID	Issue Description	Resolution	Action ID
36	NASA (JPL) guidelines and requirements for printed flex circuits.		0

Task ID 27 **Project ID** 7

TaskDescription Detailed layout of each of the 4 flex cables.

Lead

Issue ID	Issue Description	Resolution	Action ID
37	Need 37 pin connectors on each hybrid, to program the GTRC address.		0
38	Must we use Micro-D connectors on the DAQ end of the cable?		0
39	Can a vendor be found to do the full length in one go, or do we need to splice with a connector?		0
40	Do current densities satisfy NASA requirements?		0
41	Current baseline needs 9 layers serviced by each cable. Requires 2 more pins for the Fast-OR.		0
42	Reduce from 2 temperature probes to 1? If not, at least the 2 returns can be combined.		0
43	Is a differential reset signal really needed?		0
44	Add filtering just below the first tracker layer.		0
45	Jumper the analog and digital grounds together just below the first tracker layer and provide a means for tying off the ground there to the shield.		0
46	Need additional shield around the part of the cable that runs past the calorimeter.		0

Task ID 28 **Project ID** 8

TaskDescription Design, prototype, test carbon-tray structure

Lead Hytec

Issue ID	Issue Description	Resolution	Action ID
47	Move kapton cables away from the corners.		0
48	Keep top/bottom dimensional symmetry as much as possible to facilitate fixuring and avoid assembly errors.		0
49	Add top/bottom, left/right indicators to the closeout.		0
50	Do we really need 5 closeout variations (top, bottom, superglast, normal, no lead)?		0
51	Minimize need for tight tolerances.		0
53	Make sure that the kapton readout cables are adequately supported.		0
54	Stagger the tapped hole pattern in the bottom closeout to avoid crossing screw holes.		0
55	Mold ridges in the face sheet for placement of converters?		0
104	What units should be used for dimensioning drawings?		0

Task ID 18 **Project ID** 9

TaskDescription Design and fabricate the front-end and digital block test chip.

Lead Vallon Chen

Issue ID	Issue Description	Resolution	Action ID
103	Is the modified, differential calibration system too much of a risk?		

81	Is 1.3us the appropriate shaping time?	0
82	Should the analog power be brought in from the sides, or jumpered over the top with wire bonds?	0
83	Increase the size of the bonding pads	0
84	Output the FIFO read and write pointers.	0
85	Is a 4-deep FIFO enough?	0
86	Should the back of the chip be gold coated, to get better ground plane contact?	0
87	Differential hard reset signal?	0
88	Change the address for turning on the Fast-OR input bias to be appropriate for the new hybrid layout.	0
89	Add a start bit to the output of the configuration register.	0
105	How can we verify T-Spice without having Hspice to compare with?	0
106	How do we deal with programmable cells in converting from Cadence to Tanner layout?	0
114	What is the cross talk between adjacent channels, and how far is it from threshold?	0
3	Is the Tanner layout editor up to the task of designing the GTFE64 chip?	3

Task ID 39 **Project ID** 10

TaskDescription Write new specifications for the GTRC chip

Lead Robert Johnson

Issue ID	Issue Description	Resolution	Action ID
90	Self bias the data inputs to logic zero.		0
91	Make sure that data can still be sent out with the Fast-OR stuck high.		0
92	Remove the TOT logic?		0
93	Add a bit to the configuration register to disable the Fast-OR input?		0
94	Remove the clock-on command and add a bit to the configuration register to keep the clock on all the time.		0
95	Disable the Fast-OR output during the clock-on transient. What implication does this have for dead time?		0
96	Process the buffer info from front-end chips and record errors.		0
97	Receive a data word with the read event command and report it back in the event trailer or header to verify the GTRC buffer control.		0
98	Differential input for the hard reset?		0
99	Use a command to initiate the token?		0
100	Increase the size of the bonding pads.		0
101	Use an SEU safe configuration register.		0

102	Review size of the buffer (64)	0
112	Should the GTRC be designed to issue to read from GTFE64 chips automatically?	0