Project ID	1	Project Name Tracke	er Layout	
Project Des	scription	Fix the parameters of the overa	ll Tracker layout.	
End Date	Task ID	Task Description	Lead	Notes
5/1/00	2	Fix SSD strip pitch	Hartmut Sadrozinski	This needs sign-off at IPO level.
5/1/00	1	Fix overall Instrument dimensions and fix Tracker SSD size.	Martin Nordby	This needs sign-off at IPO level.
7/1/00	3	Finalize the tracker converter configuration.	Hartmut Sadrozinski	Requires sign-off at IPO level. Affects tower height, tray design, flex cable design.
Project ID	2	Project Name Specif	y and define SSDs	
Project Des	scription	Finalize the SSD design and pro-	epare for production.	
End Date	Task ID	Task Description	Lead	Notes
	47	Review detector specifications	Hartmut Sadrozinski	
	46	Prepare detector specifications	Takashi Ohsugi	
	5	Test ST prototype detectors	Hartmut Sadrozinski	
	6	Detector long-term testing.	Gwelen Paliaga	
6/1/00	4	Finalize the detector mask design.	Takashi Ohsugi	Requires completion of tasks 1 (detector size) and 2 (strip pitch).
Project ID	3	Project Name Ladde	r Assembly	
Project Des	scription	Develop the ladder assembly te equipment.	chniques and production	
End Date	Task ID	Task Description	Lead	Notes
	25	Develop and test a procedure for encapsulation of the ladder wire bonds.		
	9	Test methods for applying adhesive to the detector edge. Choose the best.	Eduardo	
	8	Design, prototype, and test the edge-gluing fixture.	Eduardo	
		Research adhesive for edge		

GLAST Tracker Projects

Project ID	4	Project Name Ladde	er Placement	
Project Des	scription	Develop the techniques and jig onto trays. Includes studies o issues.		
End Date	Task ID	Task Description	Lead	Notes
	11	Research adhesives for attachment of ladders	Ossie Millican	
	16	Perfect the method for establishing and controlling the space between detectors and bias circuit.		
	12	Design and prototype a precision jig for ladder attachment	Gwelen Paliaga	Reduce ladder spacing to 100um
	30	Design storage/work holder fixture for trays.		Begin with the concept developed for the BTEM.
Project ID	5	Project Name Hybri	d PC Board Development	
Project Des	scription	Develop techniques and parts and attachment to the trays.	for assembly of the hybrid	
End Date	Task ID	Task Description	Lead	Notes
	31	Encapsulation or conformal coating method for the hybrid.	Gwelen Paliaga	
	32	Choose an adhesive/spacer material to attach the hybrid to the tray.	Gwelen Paliaga	
	33	Design jigs for storage and work on the hybrids.	Gwelen Paliaga	Start with the BTEM concept.
	34	Design a jig for burn-in of the hybrids.	Gwelen Paliaga	Start with the BTEM design.
	35	Develop a procedure for cleaning of the hybrids before wire bonding.	Gwelen Paliaga	This may be done by the assembly vendor, especially if one vendor does both the surface mount parts and the chips.
	26	Design and prototype the flex circuit to be bonded to the corner piece.	Gwelen Paliaga	
	15	Redo the layout of the hybrid PC board.	Robert Johnson	BJ has a preliminary layout of the new overall dimensions and screw locations.
	42	Test the electronics assembly in vacuum and over the required temperature range.	Gwelen Paliaga	

	13	Prototype and test the new corner scheme for the detector-electronics interconnect	Gwelen Paliaga		
Project ID	6	Project Name Detect	or Bias Circuit		
Project Des	scription	Design and fabricate the bias c	ircuit for the planes of SSD).	
End Date	Task ID	Task Description	Lead	Notes	
	22	Detailed CAD layout of the Kapton bias circuit			
Project ID	7	Project Name Flex R	leadout Cable		
Project Des	scription	Update the design of the tracket the flight instrument.	er flexible readout cables fo	r	
End Date	Task ID	Task Description	Lead	Notes	
	27	Detailed layout of each of the 4 flex cables.			
	45	Research flex circuit vendors and determine whether a splice will be needed in the cable.			
Project ID	8	Project Name Tray M	Mechanical Assembly		
Project Des	scription	Complete the final design and p fiber based trays for the flight i			
End Date	Task ID	Task Description	Lead	Notes	
	10	Thermal testing of ladder/face- sheet assemblies	Gwelen Paliaga		
	29	Detail design of face sheets.	Hytec		
	28	Design, prototype, test carbon- tray structure	Hytec		
Project ID	9	Project Name Front-	end Readout ASIC		
Project Des	Project Description Final design and prototyping of the GTFE64 chip in the process to be used for flight.				
End Date	Task ID	Task Description	Lead	Notes	
		Convert the layout of	Vallon Chen		
	17	GTFE64 cells from Cadence to Tanner.			

20	Design an SEU-hard flip-flop cell for the configuration register.	Ned Spencer	
18	Design and fabricate the front- end and digital block test chip.	Vallon Chen	
36	Update the schematic design of the GTFE64 and simulate in spice and Viewsim.	Ned Spencer	
19	Design and fabricate a test board for the front-end and digital block test chip.	Robert Johnson	
38	Prototype fab and test of the GTFE64 chip in HP0.5um	Wilko Kroeger	
41	Test the ASICs for single- event-latchup and SEU immunity.	Ned Spencer	
44	Test and characterize the HP 0.5um amplifier prototype chip	Masa Hirayama	
55	Design and fab a probe card for GTFE64 testing.		This card should include a GTRC chip close to the probes, plus multilayer layout similar to the hybrid.
57			
37	Do the final GTFE64 layout in the HP0.5um process, using Tanner tools	Vallon Chen	
Project ID 10	Project Name Reado	out Controller ASIC	
Project Description	Final design and prototyping o process to be used for flight.	f the GTRC chip in the	
End Date Task	ID Task Description	Lead	Notes
60	Update the Verilog model of the GTRC and simulate		
39	Write new specifications for the GTRC chip	Robert Johnson	
54	Develop the standard-cell set for the HP 0.5um process (for the GTRC chip layout in Cadence)		
Project ID 11	Project Name Electr	onics Requirements	
Project Description	Complete the specifications an end readout system.	d design of the tracker from	t-
End Date Task	ID Task Description	Lead	Notes

	24	Make noise measurements on the BTEM tower electronics with and without concurrent readout.	Wilko Kroeger	
	59	Write a publication on the front end electronics	Robert Johnson	
	58	Make detailed noise measurements with a GTFE64 chip mounted on a Liz board.	Masa Hirayama	
	61	Measure delays in tracker Fast-OR chain	Wilko Kroeger	
	53	Complete the tracker electronics requirements document.	Robert Johnson	
Project ID	14	Project Name Tracke	er Converters	
Project Des	scription	Procurement of the converter f procedures for mounting them	-	e
End Date	Task ID	Task Description	Lead	Notes
	23	Prototype and test a carbon- lead-carbon sandwich		
	56	Build and test a multi-layer Carbon-Pb laminate for SuperGLAST layers.	Guido Barbiellini	
Project ID	15	Project Name Tracke	er Tower Design	
Project Des	scription	Overall tracker tower mechanic including walls, Vectran cables to grid.		
Project Des		including walls, Vectran cables		Notes
Project Des		including walls, Vectran cables to grid.	, ACD snubbers, interface	Notes
Project Des	Task ID	including walls, Vectran cables to grid. Task Description Tower thermal analysis and	, ACD snubbers, interface Lead Erik Swensen	Notes
Project Des End Date Project ID	Task ID 40 17	including walls, Vectran cables to grid. Task Description Tower thermal analysis and wall design.	, ACD snubbers, interface Lead Erik Swensen onics Review	Notes
Project Des End Date Project ID Project Des	Task ID 40 17 scription	including walls, Vectran cables to grid. Task Description Tower thermal analysis and wall design. Project Name Electro	, ACD snubbers, interface Lead Erik Swensen onics Review	Notes
Project Des End Date Project ID Project Des	Task ID 40 17 scription	including walls, Vectran cables to grid. Task Description Tower thermal analysis and wall design. Project Name Electron Prepare for and hold the electron	, ACD snubbers, interface Lead Erik Swensen onics Review onics design review.	
Project Des End Date Project ID Project Des	Task ID 40 17 scription Task ID	including walls, Vectran cables to grid. Task Description Tower thermal analysis and wall design. Project Name Electro Prepare for and hold the electro Task Description Prepare hierarchal set of	, ACD snubbers, interface Lead Erik Swensen onics Review onics design review. Lead	
Project Des End Date Project ID Project Des	Task ID 40 17 scription Task ID 48	including walls, Vectran cables to grid. Task Description Tower thermal analysis and wall design. Project Name Electron Prepare for and hold the electron Task Description Prepare hierarchal set of block diagrams	, ACD snubbers, interface Lead Erik Swensen onics Review onics design review. Lead Robert Johnson	

	50	Prepare a preliminary interface description	Robert Johnson		
Project ID	20	Project Name	Tracker Web Page		
Project Des	scription	Create and maintain the	e tracker web pages		
End Date	Task ID	Task Description	Lead	Notes	

43 Set up the tracker web page at Masa Hirayama UCSC