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Second Draft

GLAST Tracker
Front-End Electronics Requirements

Table of Contents:

1 Scope

The tracker front-end electronics encompass all electronics mounted on the tracker module and the cables connecting those modules to the data acquisition in the TEM.

2 Testing and Verification

The following tests will verify all of the functionality requirements and specifications and are not repeated for each requirement in the following sections.

2.1 Automated Probing of ICs

All chips shall be tested for complete functionality on the wafer by automated probing.

2.2 Hybrid Testing

Before mounting onto a tray, all hybrid assemblies shall be tested for complete functionality, threshold uniformity, and noise performance, as well as burn-in, by connection to a TEM module.

3 Performance Requirements

3.3 Trigger Noise versus Efficiency:

Noise occupancy for the trigger shall be less than 5×10^{-5} with ≥99% single-hit MIP efficiency at normal incidence.

- Justification: For the simple trigger algorithm envisioned (coincidence of signals made up from the logical OR of all hits in a layer), the noise occupancy must be this low in order to keep the noise L1T rate well below 1 kHz.
- Status: The electronics of the BTEM had noise occupancy well below 10^{-5}, giving a noise L1T rate of only a few Hz. This was with no digital readout in progress. Noise occupancy during digital readout activity is under study.
- Verification: Bench-top threshold scans taken with actual data acquisition modules, both with and without readout digital activity in progress.

3.4 Data-Stream Noise versus Efficiency

Noise occupancy for the data stream shall be less than 5×10^{-4} with ≥99% single-hit MIP efficiency at normal incidence.

- Justification: This is a data volume issue. The quoted level corresponds to about one noise hit per layer. More than that would have a significant impact on the data volume, relative to hits from actual tracks.
- Status: The BTEM tracker more than met this requirement even without any masking of channels.
- Verification: Same as for the trigger noise.

3.5 Threshold Uniformity:

The rms variation of the discriminator thresholds across a single front-end chip shall not exceed 10% (TBR) of the nominal setting.

- Justification: The nominal setting is about 4 times the rms noise, so this requirement keeps the variation to less than half the rms noise level. The goal is to prevents the margin between noise too high (minimum threshold) and efficiency too low (maximum threshold) from being eaten up by threshold variation. With CMOS technology, achieving better than about 10% (some 16 mV in this case) may not be readily feasible.

- Status: Measurements on existing prototypes indicate rms variations across individual chips that are typically less than 10 mV but in some cases as high as 16 mV.
- Verification: by threshold scans on chips mounted on a special printed-circuit test board that provides an LVDS calibration trigger.

3.6 Readout Speed and Dead Time:

Assuming a noise occupancy in the data stream of 10^{-3} and a calorimeter dead time of 20 μs per event, the tracker should have no significant additional impact on the dead time up to a trigger rate of 10 kHz.

- Justification: In other words, the tracker dead time at 10 kHz should be significantly less than 20%. The 20 μs is the deadtime of the calorimeter, and the tracker should not add to that.
- Status: The BTEM tracker has sufficient front-end buffering to avoid any problem with Poisson fluctuations. Bench tests show that the digital-analog coupling is small enough that the trigger can go active again only a few microseconds after the startup of the readout.
- Verification: by simulations using the expected background mix, together with bench tests using the calibration system to inject "data."

4 Functional Requirements

4.1 Signal Processing:

2.1.1 Amplifier Type

The front-end amplifiers shall be charge sensitive with a continuous reset.

- Justification: This is the appropriate choice for silicon-strip detectors and an asynchronous signal.
- Status: The existing GLAST tracker amplifier design is of this type.

2.1.2 Shaper type

The shaping amplifier (2^{nd} stage) shall be CR/RC (single pole).

- Justification: A more complicated shaping function would require more current-carrying nodes in the circuit and hence more power, with only marginal improvement in noise performance.
- Status: The existing design is of this type, although the use of MOSFETs rather than resistors results in a more linear than exponential decay of the pulse, especially for large pulse heights.

2.1.3 Shaping Time Constant

The time constant of the shaping amplifier shall be in the range from 1 to 2 microseconds (TBR).

- Justification: A shorter time constant would result in too much amplifier noise and would also decrease the time available for making a trigger decision. The maximum tolerable value depends on the expected end-of-life detector shot noise. Increasing the time constant would also increase the size of the trigger coincidence window and would also increase the length of the tower trigger dead time following passage of tracks through the tower. (The Fast-OR trigger outputs cannot pulse for a second event until the amplifier outputs from the first event have fallen below threshold.)
- Status: The existing amplifiers have a time constant of around 1.3 to 1.5 μs.
- Verification: by internal picoprobing of representative chips on a test board.

2.1.4 Linearity

TBD

- Justification:
- Status:
- Verification: by bench testing on a special PC board, using an external calibration trigger and the internal calibration DAC.

2.1.5 Digitization Method

Digitization shall be done by means of a single threshold.

- Justification: The GLAST science has no requirement for pulse-height analysis in the tracker, whether for angular resolution, energy resolution, or particle ID. Anything more than a single threshold would be an undue complication and would squander power.
- Status: The BTEM tracker system works well with a single threshold.

2.1.6 Location of Digitization

Digitization of the amplifier outputs shall be done within the front-end chip, with no analog signals output from the chip.

- Justification: Many silicon-strip systems output the analog pulse-height in a multiplexed readout, for digitization elsewhere. This is unnecessary for single-threshold digitization and also tends to result in "common-mode" noise problems, complexity, and higher power.
- Status: The BTEM system does digitization on chip and does not show any evidence of problems from "common-mode" noise or pickup.

2.1.7 Threshold Control

The threshold shall be programmable per chip by a DAC, with range at least from 0 to 1500 mV, with a resolution of no worse than 6 mV around the nominal operating point (≈150 mV).

- Justification: Fanning analog threshold information out to all of the chips could be problematic from a noise point of view and would leave the system vulnerable to chip-to-chip threshold variations. On the other hand, having separate thresholds per channel would be extravagant and unnecessary. The resolution should not be larger than the typical threshold variation within a chip, and the maximum needs to be high enough to allow threshold scans to be done well past the 50% efficiency point for a MIP, in order to understand the amplifier gain.
- Status: The existing prototype chips satisfy this requirement with a 7-bit DAC having 6 bits of resolution and two ranges.
- Verification: testing of representative chips on the bench with a test board.

2.1.8 Recovery

The amplifier output shall fall below the discriminator threshold after no more than about 100 μs in the case of a very large charge deposition, such as from an iron ion.

- Justification: A tracker module cannot retrigger as long as the amplifier outputs remain above threshold, so it is important that highly ionizing particles do not hold the trigger dead for too long a time. The limit specified here is not ideal but seems practical.

- Status: The existing prototypes satisfy this requirement, according to measurements made on the bench by inputting large calibration pulses. Spice simulations do not reproduce the observed behavior but predict much longer saturation.
- Verification: by measuring the response to large calibration pulses on a test board.

*4.2 **Control**:*

2.1.1 Remote Command

It shall be possible to configure the electronics by remote commands. This includes all such items as threshold settings and masks.

- Justification: self-evident.
- Status: The existing chips can be remotely configured.

2.1.2 Configuration Default

The chips shall power up into a reasonable default configuration.

- Justification: This is primarily of importance to facilitate initial testing of the chips.
- Status: Each bit of the configuration register of the existing chips has a power-on default.
- Verification: The default can be checked in chip testing by exercising the read-back feature (Item 2.1.3).

2.1.3 Configuration Read-back

It shall be possible to verify by read-back that the desired bits were in fact written into the chip configuration registers.

- Justification: Defects in a chip could prevent the configuration from shifting in properly without that otherwise being evident to the operator.
- Status: In the existing prototype the current contents of the register shifts out as the new contents are shifted in. This was verified in the chip testing, but the existing DAQ does not pick it up. A start bit needs to be added to the output to allow the DAQ to pick it up easily.

2.1.4 Control Protocol

Run-time and calibration control shall be by chip-addressed serial command strings, except for the trigger input for the data latch, which may be a dedicated line.

- Justification: This requirement is important for minimizing the number of signal lines, which is important for minimizing failure points and cable mass. A dedicated line may be preferred for the data latch in order to keep to the required trigger latency.
- Status: The BTEM system has a dedicated trigger line and uses serial strings with chip addresses for all other commands. The GTRC readout controller chips are controlled from the DAQ and they in turn generate the control signals for the GTFE64 front-end chips.

4.3 Software Reset

It shall be possible to reset individual chips by serial command.

- Justification: self evident.
- Status: exists in the actual prototypes.

4.4 Hardware Reset

There shall be a separate hard reset line, either differential or else referenced to the front-end electronics ground, that will reset the whole system if pulsed.

- Justification: A hardware reset is necessary when the chips get into an unresponsive state, for whatever reason. It is not desirable to have to cycle the power to recover them.
- Status: The existing prototypes have a hardware reset, which is single-ended CMOS. There was a pair of LVDS driver and receiver chips used on the TEM board to reference to the front-end ground and isolate from the TEM-board ground.

4.5 Inputs to the Trigger Logic

Each tracker layer shall output asynchronously a logical OR of the state of its discriminator outputs (the "Fast-OR"), to be used as input to the trigger logic.

- Justification: The tracker must self trigger.
- Status: This is fully implemented in the BTEM system.

4.6 Trigger Mask

It shall be possible to mask individual channels from the Fast-OR, under external control, independently of the mask for the data stream.

- Justification: In case of a large number of anomalous noisy channels, masking them from the trigger would have less impact on the science than removing them from the data stream.
- Status: This is implemented in the BTEM system.

5 Calibration

5.1 Charge Injection by Command

It shall be possible to inject charge into the amplifiers by serial command with amplitude controlled by an on-chip DAC.

- Justification: This is needed mainly for functionality testing (too noisy for detailed, quantitative performance measurements) during production, I&T, and on orbit. The on-chip DAC is important to avoid fanning out an external DC level to a million channels.
- Status: This is implemented in the BTEM system.

5.2 Charge Injection by External Trigger

It shall be possible to initiate a calibration pulse by means of a quiet, external LVDS signal, for bench testing only.

- Justification: This is necessary for doing detailed, quantitative noise measurements from threshold curves. However, it is only for testing the chip design and, therefore, does not need to be implemented on the flight-instrument hybrid. Special test boards will be used to exercise chips in this manner.
- Status: This is implemented in the GTFE64 chip used in the BTEM system, and a test PC board for making threshold scans in this manner is in hand.

5.3 Pulse Height Range and Resolution

The internal calibration system shall have a pulse-height range at least from 0 to 50 fC with a resolution no worse than 0.25 fC.

- Justification: 50 fC corresponds to about 10 MIPs, which is sufficiently far above the signals of interest (1 to 2 MIPs). Heavy ions can give much more, but their effect on the amps can be studied on the bench by external charge injection. 0.25 fC corresponds roughly to the expected noise sigma.

- Status: The GTFE64 chip used in the BTEM satisfies this requirement, except that the resolution is closer to 0.275 fC.
- Verification: by bench testing of prototype chips.

5.4 Selection of Channels for Calibration

The front-end chip shall include a programmable mask to select any set of individual channels for pulsing.

- Justification: This flexibility is needed for noise studies of individual channels, for crosstalk studies, and for simulations of varying degrees of occupancy in data.
- Status: The GTFE64 chip used in the BTEM includes this feature.

6 Testing and Monitoring

6.1 Temperature Monitoring

The temperature shall be monitored on at least 8 locations distributed roughly uniformly over the tower height, including the top and bottom trays, and uniformly on all four sides of the tower.

- Justification: We need to see the temperature gradient in the tower, but the temperature of every single hybrid is not necessary, since all hybrid on a side are closely coupled thermally. Some redundancy on each side is desired.
- Status: the BTEM tower has two monitors per cable, for a total of 16.

7 Bias Voltage

7.1 Insulation

All traces, leads, and wire bonds, with the exception of the traces under the detectors on the bias circuit, shall be insulated or encapsulated.

- Justification: It is critical for these conductors not to be shorted by debris. Also, there may be some danger of electrical discharge in vacuum.
- Status: In the BTEM tower the wire bonds from the hybrid to the bias circuit were not encapsulated, and the solder leads on the connectors were not encapsulated. Otherwise the conductors were insulated.
- Verification: visual.

7.2 Isolation of Tower Circuits

It shall be possible during operations to switch off the bias supply to any individual side of a tower.

- Justification: In case of a short circuit in one set of cables and hybrids, it is desirable not to lose the entire tower.
- Status: In the BTEM the whole tower was operated from a single supply, but the conductors were separate for each tower side.

7.3 Isolation of Ladder Circuits

The bias circuit for each ladder shall be separate and isolated from the bus by a resistor of no less than 100 kΩ and no more than 200 kΩ.

- Justification: In case of a short in one of the circuits, the supply should only have to supply at most an additional ~1 mA of current in order to keep alive. The voltage drop for functional ladders would not be more than about 10 V in the worst case toward end-of-life. This separation also facilitates testing and trouble shooting during assembly and prevents noise from propagating from one ladder to the next.
- Status: In the BTEM design this criterion is satisfied, using 100 kΩ resistors.

- Verification: check each tray with an ohmmeter before mounting the ladders.

8 Power Dissipation

Including contingency, the power consumption of the front-end electronics must not exceed 250 W (TBR) of already conditioned power, including reserves. This figure does *not* include power needed to drive signals and clock from the DAQ to the front-end electronics.

- Justification: This corresponds to the allocation in our proposal.
- Status: The corresponding power consumption in the BTEM was 210 μW/ch, which would yield a total of 217 W for the proposal baseline design.
- Verification: bench-top power measurements on individual hybrids, with readout at the maximum trigger rate.

9 Power, Grounding, and Shielding:

9.1 Separation of Analog and Digital Grounds

Digital and analog grounds shall be kept separate in the front-end electronics and only tied together, and tied to the shield (the tracker module mechanical structure), at the point where the cables exit the tracker.

- Justification: The isolation is necessary for keeping digital noise out of the amplifiers. The tracker shield is the best ground reference for the tracker module as a whole. Keeping the grounds separate to the TEM would introduce potentially problematic ground loops between the 8 readout cables.
- Status: This grounding scheme was implemented in the BTEM tracker module and worked well, with no evidence of any detrimental effects from noise pickup.
- Verification: check the resistance between the grounds with an ohmmeter for each completed hybrid and regularly during tray and tower assembly.

9.2 Separation of Analog and Digital Supplies

Digital and analog power shall be derived from separate supplies and kept separate everywhere.

- Justification: This is essential for isolation of the analog system from digital noise.
- Status: This was implemented in the BTEM.
- Verification: check the separation of the busses with an ohmmeter.

9.3 Substrate Connections on the Front-End Chips

On the mixed-mode front-end IC chips, only the analog ground shall be connected to the substrate, while the digital ground return takes place in metal traces that are not tied to the substrate.

- Justification: If this were not done, then the analog and digital grounds would be connected by a fairly low resistance, causing too much digital feedthrough to the amps. This procedure has been used before, such as on the BaBar Atom chip. The danger is an increased susceptibility to latch-up.
- Status: This was done on the 3rd and final prototype of the BTEM front-end chip, which showed significantly less digital-analog coupling compared with the earlier prototypes.
- Verification: by LVS in the CAD tools.

9.4 Digital-Analog Coupling

Digital-analog isolation shall be sufficient that digital activity during a readout cycle (not including a possible clock-turn-on transient) does not induce above-threshold signals into the amplifiers, assuming the normal operational threshold.

- Justification: This is essential in order that the front-end buffering can be used, which in turn is necessary for achieving low dead time at the high rates foreseen. The clock turn-on transient is not such as problem, as the trigger can be held dead for this short time.
- Status: Preliminary measurements on the BTEM module indicate that this requirement is satisfied at the threshold we ran for the duration of the beam test, even during the clock-on transient.
- Verification: on the bench at the tray level check the trigger output rate versus threshold during the time of readout of a previous trigger.

9.5 Shielding of Cables in the Calorimeter Region

The cables between tracker and TEM shall be shielded between the base of the tracker and the TEM enclosure.

- Justification: The tracker digital noise should be isolated from the calorimeter front-end electronics and possible calorimeter noise should be isolated from the track analog supplies and ground.
- Status: In the BTEM the Kapton cables did not extend very much past the tracker base, but the twist-pair cables going to the VME crates were fully shielded.

9.6 Separate Grounding of Detector Ladders

The ground on the bias circuit under the detectors shall be separate for each ladder, with separate connections to the hybrid.

- Justification: This is a precaution to limit spurious current paths.
- Status: in the BTEM tower the ground plane in the bias circuit was not divided.
- Verification: on each tray, using an ohmmeter before ladder attachment.

9.7 Digital and Analog Ground Connection on the Hybrid

There shall be on each hybrid a point where digital and analog ground may be connected via a surface-mount resistor.

- Justification: This is a precaution, in case we find during development that latch-up safety or an unforeseen noise issue forces us to couple the grounds together on the hybrid.
- Status: This feature is included in the BTEM hybrids, but no such resistor was installed.

10 Reliability

10.1 Redundancy of Chip Readout Paths in a Layer

Failure of a single amplifier chip shall not result in the loss of data from the other chips in the layer.

- Justification: In a system in which the chips are read out serially, one after another, there is a danger that a single bad chip will destroy the readout path for all chips.
- Status: The BTEM design has dual readout paths, which satisfies this requirement.

10.2 Redundancy of Readout Paths from each Layer

Failure of the digital readout of a single layer shall not result in the loss of data from the other layers.

- Justification: In a system in which the layers are read out serially, one after another, there is a danger that a single bad layer will destroy the readout of all layers.
- Status: The BTEM design has two cables for each layer, giving two independent readout paths.

10.3 Redundancy in Power Paths

An open failure of a single readout/power cable shall not result in the loss of data.

- Justification: In a design in which the data from several layers are multiplexed onto a single cable, there is a danger of losing a large amount of functionality from a single fault.
- Status: The BTEM design has two cables for each layer, with independent readout paths. The power and ground paths, however, are not independent, so a short circuit in one cable will affect the other.

10.4 Loss of Functionality in the Case of a Power Short

Shorting of power connections in a cable shall not result in the loss of more than ¼ of the layers in a single tower.

- Justification: Catastrophic loss from a short circuit in a cable can be minimized by keeping the four sides of the tower separate.
- Status: The cables on the different sides of the BTEM are independent as far as the tracker is concerned, so the issue is how they get connected in the TEM.
- Verification: use an ohmmeter to check that the power and ground really are separate for the four tower sides.

10.5 Safety from Power Shorts in a Single Layer

A power short within a layer shall not result in the loss of data from other layers (i.e. each layer shall be separately fused).

- Justification: It would be better to lose one layer by blowing out a fuse on the hybrid than to short out the power of all 9 hybrids on the side of a tower.
- Status: The BTEM hybrids have fuses for all power inputs except for the detector bias, which is somewhat protected by 100 kΩ series resistors on each hybrid.
- Verification: bench tests of prototypes to check that the fuses blow at a safe level.

11 Radiation Tolerance

11.1 Radiation Hardness:

Test samples of the tracker readout electronics shall be demonstrated to withstand 10 kRad (TBR) of ionizing radiation (with the dose accumulated under power and with an active clock) with no loss of functionality and while still satisfying the noise and threshold-matching specifications when connected to complete detector ladders irradiated to the same level.

- Justification: This is about 10 times the expected dose, yet commercial CMOS processes easily satisfy this requirement.
- Status: Early prototypes of the BTEM readout chip were tested up to 20 kRad without any serious detrimental effects.
- Verification: irradiation in the ^{60}Co source at UCSC.

11.2 Single-Event Latchup Immunity

The two CMOS ASICs must be immune to single-event latchup to a level of at least 20 MeV-cm^2/g LET (TBR).

- Justification: In the NASA GLAST IRD document this is the level above which the predicted curve plummets to negligible values in the non-solar-flaring case.
- Status: Published tests of the HP 0.5um process show that it is latch-up hard to 63 MeV-cm^2/g without any modifications to the design rules. Nevertheless, we have to be concerned about or own layout and about possible detrimental effects of isolating the digital ground return from the substrate.
- Verification: testing in a heavy ion beam.

11.3 Single-Event Upset Immunity

The configuration registers of the ASICs must be immune to single-event upset to a level of at least 3 pC (TBR).

- Justification: Occassional bit errors in the data path will only add a little to the stochastic noise, but a bit error in the configuration register (such as a DAC setting) might remain undetected for many hours, spoiling large amounts of data.
- Status: We have simple memory cell designs that appear, in simulation, easily to exceed this requirement.
- Verification: testing in a heavy ion beam.

12 Safety

13 Cooling

13.4 Coupling of Hybrids to Closeouts

A thermal gasket or adhesive shall lie between the hybrid and the closeout to ensure good thermal coupling in vacuum.

- Justification: Mounting with screws without a gasket would likely give unreliable thermal contact and an unacceptably large temperature drop.
- Status: In the BTEM tracker only screws were used for mounting of hybrids, and the backing, insulating plate between hybrid and closeout was G10, which is too stiff to serve as a thermal gasket.
- Verification: thermal-vac testing of prototypes and qualification units.

13.5 Current Density in Cables

The current density in the conductors of the cables shall comply with the guidelines in the JPL Handbook D-8208.

- Justification: Currents exceeding these guidelines might cause excessive heating of the cable.
- Status: The design of the BTEM cables yields current densities at least 10 times lower than the guideline maximum.
- Verification: measurement of the currents in a prototype system.

13.6 Cooling of Cables

The length of flex cables that passes past the calorimeter shall be clamped securely to the wall of the grid.

- Justification: This is the only section of cable in which heat might have to flow a significant distance before coupling into the mechanical structure (more than a few cm).
- Status: In the BTEM design this was not an issue.
- Verification: visual.

14 Mechanical Constraints

14.7 Proximity to Detectors:

Amplifier inputs must be as close as possible to the detector strips.

- Justification: Good noise performance requires that the signal-current loop be as short as possible.
- Status: In the BTEM design the signal passes through 1 wire bond, a 4 mm Au plated Cu trace, and a 2nd wire bond before reaching the amplifier. The return current passes into a ground place, through a capacitor to the bias plane and back through 2 wire bonds and a 4 mm trace to the bias circuit that makes back contact with the detectors.

14.8 Minimization of Dead Space

The dead space between tracker towers must be minimized.

- Justification: Dead space between towers degrades the PSF of conversion tracks that pass from one tower to another, especially in the tails of the PSF.
- Status: In our design the front-end electronics to be located on the sides of the trays, not in the plane of the detectors, resulting in only a 13.4 mm gap from active area of one tower to that of the next.

14.9 Material in the Bias Circuit

The average number of radiation lengths of material in the bias circuit under the detectors shall be small compared to that of the silicon (0.4%).

- Justification: This is important for the PSF at low energy.
- Status: The estimated thickness of the BTEM circuit is 0.13% of a radiation length.
- Verification: measurement of the mass of prototypes.

14.10 Material in the Hybrid

The average number of radiation lengths of material in the loaded PC board shall not exceed about 2%.

- Justification: This is important for the PSF of low-energy photons that cross tower boundaries. 2% is similar to the thickness of a converter foil.
- Status: The average thickness of the BTEM PC board is 1.4% of a radiation length.
- Verification: measurement of the mass of prototypes.

14.11 Modularity of the Electronics Assembly

The front-end readout electronics for a single tracker layer shall be on a single board that is attached by screws to the tray and removable, if necessary for replacement or repairs, up to the time that the final wire bonds are encapsulated.

- Justification: This will greatly facilitate tray assembly and testing.
- Status: In the BTEM the boards had to be glued to a kapton-circuit tongue on the tray, after which point they could not be removed for repairs. This was the most difficult part of the tray assembly.
- Verification: test the removal and reattachment of several hybrids.

14.12 Encapsulation of Hybrids

Front-end electronics boards shall be conformal coated after testing and burn-in including complete coverage of the IC chips and wire bonds, including wire bonds to the flex circuit.

- Justification: This is important, in order to prevent damage to the hybrids between when they are tested and when they are mounted on finished trays. It also prevents damage during assembly and cabling of the tower and attachment of walls.
- Status: This was done on the BTEM tower using Silguard, a soft silicone-based encapsulant.
- Verification: visual inspection.

14.13 Encapsulation of Solder Pins of Connectors

Connector solder pins on the PC boards and flex circuits shall be encapsulated after soldering and testing.

- Justification: This is important in order to strengthen the attachment of connectors to cables and to prevent short circuits during handling and from particulates during flight.
- Status: This was not done on the BTEM tower.
- Verification: visual inspection.

15 Interfaces with Other Systems

15.14 Communication Protocol:

Communication between the front-end chips and the DAQ shall be accomplished via serial lines.

- Justification: This minimizes the number of wires and reduces the number of failure points.
- Status: The BTEM design satisfies this requirement.

15.15 Multiplexing

The number of lines going to the DAQ shall be minimized, via simple multiplexing, while still satisfying the redundancy requirements.

- Justification: This minimizes the number of wires, but increases the damage from a single failure. This can be alleviated by having redundant lines.
- Status: The BTEM design multiplexes the outputs of all layers on a side of a tower onto two redundant cables.

15.16 Signaling:

All digital signals sent onto the circuit board between chips and between the front-end electronics and the DAQ shall be LVDS or pseudo-LVDS. As the only possible exception to this requirement, signals going from one chip to the next via wire bonds or very short traces with no fanout could be simple differential CMOS. (Here, pseudo-LVDS means low-voltage differential signaling which is not necessarily in compliance with all details of the LVDS standard, such as common-mode range, and not necessarily terminated at the line impedance in the case of short distances.)

- Justification: LVDS is important for minimizing digital noise feedthrough to the front-end amplifiers.
- Status: The BTEM used LVDS everywhere, except for the passing of data from one front-end chip to the next (and from front-end chip to the controller chip), in which case differential CMOS was used.

16 Parts

16.17 Layout Rules

PC board and flex circuit layout shall be done in compliance with the JPL Handbook D-8208 (TBR).

- Status: This was not followed in the case of the BTEM, and there are several violations already evident.

16.18 Connectors on the Hybrids

Mil-spec/space-qualified nano connectors with plastic body and captive jackscrews shall be used on the front-end electronics boards.

- Status: The Nanonics connectors used in the BTEM satisfy this requirement.

16.19 Connectors for the DAQ Interface

Mil-spec/space-qualified Micro-D connectors with metal body and captive jackscrews on the DAQ ends of the cables (TBR).

- Justification: This is what the DAQ group prefers.
- Status: In the BTEM a PC board is used to make the transition from Nanonics to Micro-D. Putting the Micro-D on the flex cable may be problematic and needs to be investigated.

16.20 Passive Components on Hybrids and Cables

All passive components are standard surface mount chips selected according to ?? (TBD).

- Status: The BTEM used standard commercial surface-mount parts.