Experimental Determination of the Allowable Stress Limits of Rigidly Bonded Silicon Wafers for the GLAST Detector Design

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Abstract

This report summarizes thermal tests done to determine the mechanical performance of silicon wafers in a worst-case scenario: bonded to a thick block of aluminum with a high modulus adhesive. The results show that the silicon wafers successfully survived conditions beyond those expected for GLAST, and that failures in previous testing are a result of something other than CTE mismatch.

Summary

The detector design for the Gamma Ray Large Area Space Telescope (GLAST) requires thin, 400 μm silicon wafers to be adhesively bonded to substrates possessing significantly higher coefficients of thermal expansion (CTE), and in some cases, higher thickness and stiffness. In orbit, it is expected that the detector will be subjected to temperatures in the range of +50 ^{o}C to –30 ^{o}C. This temperature range is large enough that mechanical failure of the silicon detectors resulting from CTE mismatch is a concern. Previous testing[1] has shown that thermal cycling of the complete detector tray design may cause the silicon detectors to break. These tests aim to better define the design space for the GLAST detector.

Test Setup

This test represents a worst-case scenario for the silicon wafers. A thin (~100 μm) bondline of space qualified, high modulus epoxy (GE 2216) was used to bond the silicon to an aluminum substrate. It can be shown[2] that stresses resulting from CTE mismatch are transferred most effectively with thin layers of high modulus adhesives. 12.7 mm thick blocks of 6061 –T6 aluminum tooling plate were used as the substrate in the sandwich as shown in Figure 1 (not to scale).

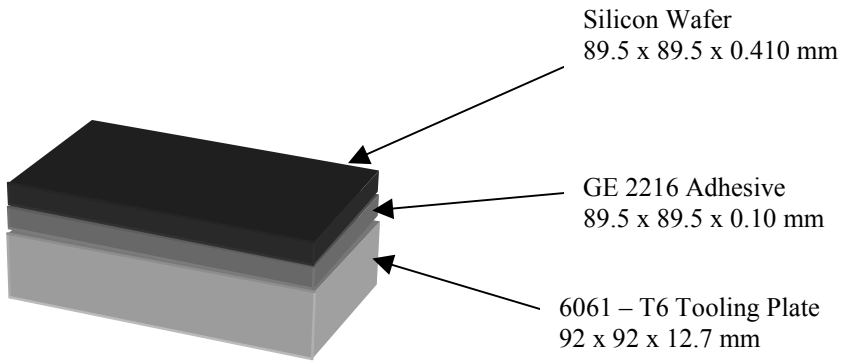


Figure 1. Schematic of the Sandwich Configuration.

Aluminum was chosen because it is readily available and has a much higher CTE (23.6 ppm/ ^{o}C) than silicon (2.5 ppm/ ^{o}C). The aluminum's thickness was chosen to be significantly higher than that of the silicon so that the stiffness of the substrate could be considered semi-infinite in the depth direction. Hence, it is safe to assume there will be no out of plane bending or "taco" effect resulting from the silicon influencing the expansion of the aluminum, and that all effective expansion and contraction is in plane with the silicon.

The silicon wafers used were ground to 410 μm thick and the edges were laser cut. Narrow strips (~1.5 mm wide) of scotch tape were layered and used as shims to achieve

the 100 μm thick adhesive layer. The GE adhesive was allowed to cure at room temperature for three days before the strain gages were applied.

The strain gages used for this testing were Vishay CEA-06-250UW-350, lot # R-A58AD814. The gages were applied in accordance to Vishay Instruction Bulletin B-137-16. The gages were mounted in the center of each silicon coupon because the largest normal stresses were predicted to be there[2]. Two sandwich coupons (as described above) were built and instrumented, and three reference samples were instrumented as well.

All data acquisition was done with a Vishay System 5000 Scanner equipped with a single strain gage card and a single thermocouple card. All thermocouples used were Type T and were mounted to the surface of each test coupon close to the strain gage. A Cincinnati Sub-Zero dual stage environmental chamber was used to cycle the coupons through the desired temperature range.

Testing

Each thermal cycling test used two samples instrumented with a single strain gage and a single thermocouple: a sandwich sample and a silicon wafer reference sample. The reference sample was cycled along with the sandwich so that the thermal output of the strain gage/silicon wafer interface could be subtracted from the response of the sandwich sample, yielding only the thermal strain transferred to the silicon from the aluminum through the adhesive layer.

The first temperature excursions were done at temperatures above ambient (25 ^{o}C). This was done for two reasons: the elevated temperature will aid in any final curing of the GE adhesive and the failure of the silicon was expected to occur at low temperatures, where the ΔT from ambient is the greatest.

The first excursions were to 40 ^{o}C and 50 ^{o}C. This was repeated several times and the temperature ramp rate was varied and the output of each thermocouple was monitored for thermal lag between the samples (the sandwich lagging behind the smaller reference sample). The rate of 1 ^{o}C/min proved slow enough that thermal lag was negligible and that test times for large temperature excursions were practical. Previous testing of the tray assembly, done by Hytec, used ramp rates of 2 ^{o}C/min and 15 ^{o}C/min. These values are relatively high compared to the rate used in this testing, as well as the expected value for GLAST, which is 5 ^{o}C/hr.

The samples were then cycled to the following temperatures below ambient, returning to room temperature after reaching each maximum: 10 ^{o}C, 0 ^{o}C, -10 ^{o}C, -20 ^{o}C, -30 ^{o}C, -40 ^{o}C, -50 ^{o}C, -60 ^{o}C, -70 ^{o}C (sample #2 only). The tests were run to temperatures lower than those expected in flight to gain insight on the ability of the silicon to withstand very high stresses in this configuration. The samples were soaked at each successive extreme for 20 – 30 minutes before returning to room temperature. The sandwich coupon was visually inspected between each excursion for failure or cracks of any sort.

The reduced data was then saved in MS Excel format and the analysis was done in that program.

Results

Neither sandwich sample failed in any manner. This was confirmed both visually and by the strain gage data. The resulting strain at the end of each soak period for both samples is shown below.

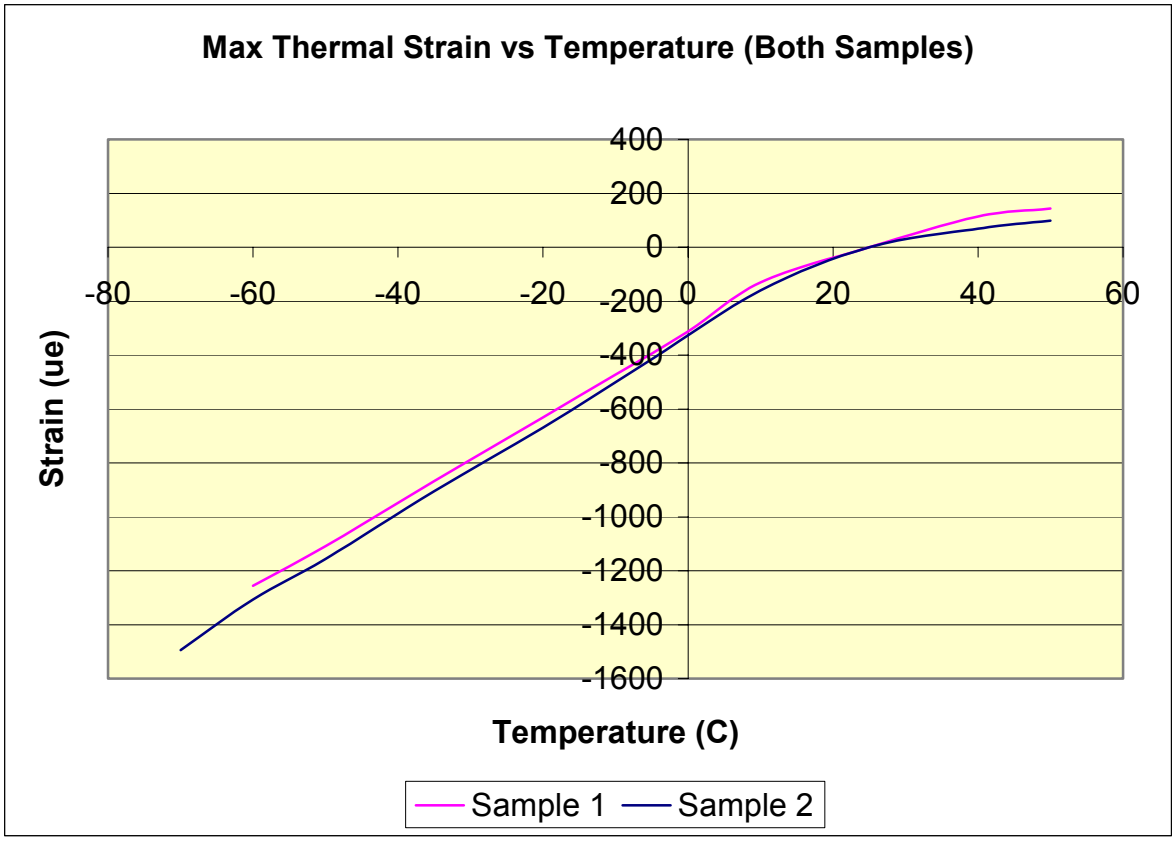


Figure 2. Strain Values After Soak for Both Sandwich Samples.

Figure 2 shows good agreement between the two sandwich samples. The largest discrepancy, seen at 40 ^{o}C, was due to a near instantaneous relaxation attributed to strain relief left over from the curing of the GE adhesive. The values in Figure 2 were obtained by subtracting the output from the reference sample from the output of the strain gage on the sandwich sample. Hence, Figure 2 is a plot of the thermal strain induced on the silicon by the aluminum, through the adhesive layer, as a result of the CTE mismatch between the silicon and the aluminum.

Next, the modulus of elasticity of silicon was determined as a function of temperature (see Appendix 1) and the corresponding values for stress were calculated from the strain data using the following relation:

$$\sigma = E(T)\varepsilon \quad (1)$$

where:
σ = Normal Stress in Silicon (MPa)
E(T) = Modulus of Elasticity as a Function of Temperature (MPa)
ε = Measured Strain in Silicon ($\mu\varepsilon$)

The resulting plot is shown below in Figure 3.

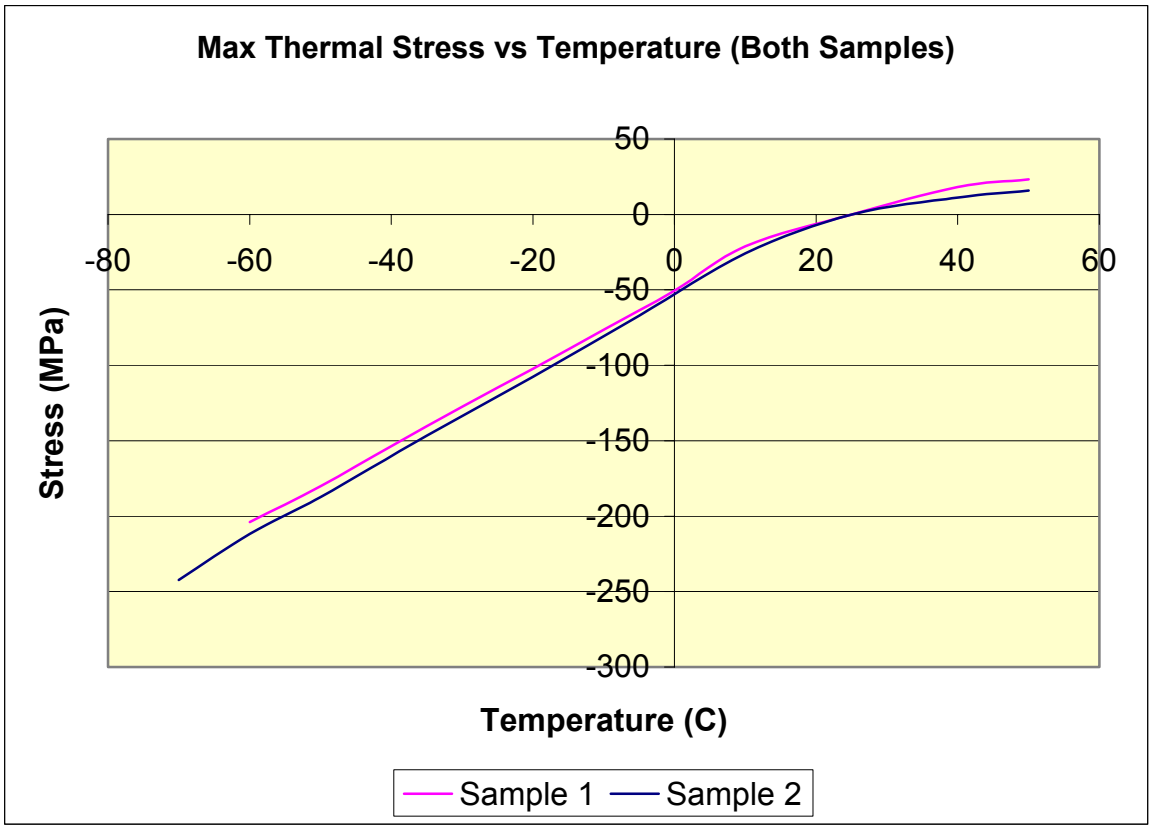


Figure 3. Stress Values After Soak for Both Sandwich Samples.

To check the validity of these results, a spreadsheet calculation[2] was used to calculate the stresses in the silicon under the influence of the aluminum block. The adhesive was considered a high modulus epoxy per Ref 2 and 100 µm thick, and the following parameters were entered into the spreadsheet for the aluminum:

E = modulus of elasticity = 69 GPa
T = thickness = 1.27e-2 m
α = CTE = 23.6 ppm/ ^{o}C

The spreadsheet results were then superimposed on the values from Figure 3.

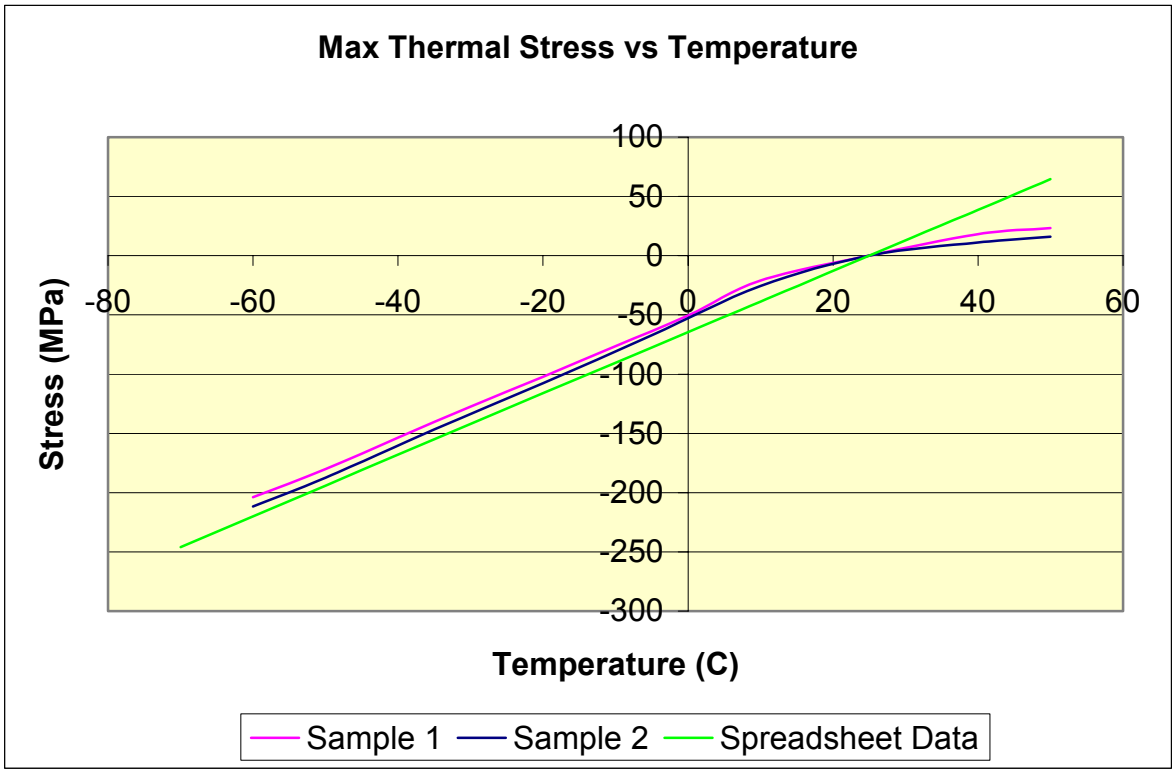


Figure 4. Comparison of Experimental and Theoretical Stress Values.

Figure 4 shows an excellent agreement between the predicted and measured values of stress in the silicon. This serves as one form of verification of the validity of the test data. Another form of verification used to validate the test data is outlined in Vishay Technical Note 504[3]. In short, this note describes how to use the calibration data provided for strain gages of a particular foil lot (the batch of conducting material the gage wires are made from) for tests where the strain gages are mounted on substrates with a CTE other than that of the gage. The calibration curve, provided on the Engineering Data Sheet that comes with the gages, shows the thermal output of the gages as a function of temperature when the gages are instrumented on a material whose CTE exactly matches that of the gage (in this case, the gage CTE = 10.8 ppm/ ^{o}C). When the substrate has different thermal properties than the gage, the following correction[3] is used to rotate the calibration curve about the zero point at room temperature.

$$\varepsilon_{TIO(2.5)}(t) = \varepsilon_{TIO(10.8)}(t) + (2.5 - 10.8)\Delta T \qquad (2)$$

where:

$\varepsilon_{TIO(2.5)}(t)$ = corrected thermal output for the silicon substrate, CTE = 2.5 ppm/ ^{o}C

$\varepsilon_{TIO(10.8)}(t)$ = provided thermal output for the silicon substrate, CTE = 10.8 ppm/ ^{o}C

ΔT = Temperature change from ambient (^{o}C)

The thermal output is always zero at room temperature by definition, yet the shape of the curve remains similar but rotated either clockwise for a substrate with a lower CTE or counterclockwise for a substrate with a higher CTE. The corrected thermal output curve is plotted with the original curve in Figure 5. Also, the experimental data obtained from the thermal testing is shown and exhibits a close match to the expected corrected output. (Note: the experimental data in Figure 5 is from the reference sample only).

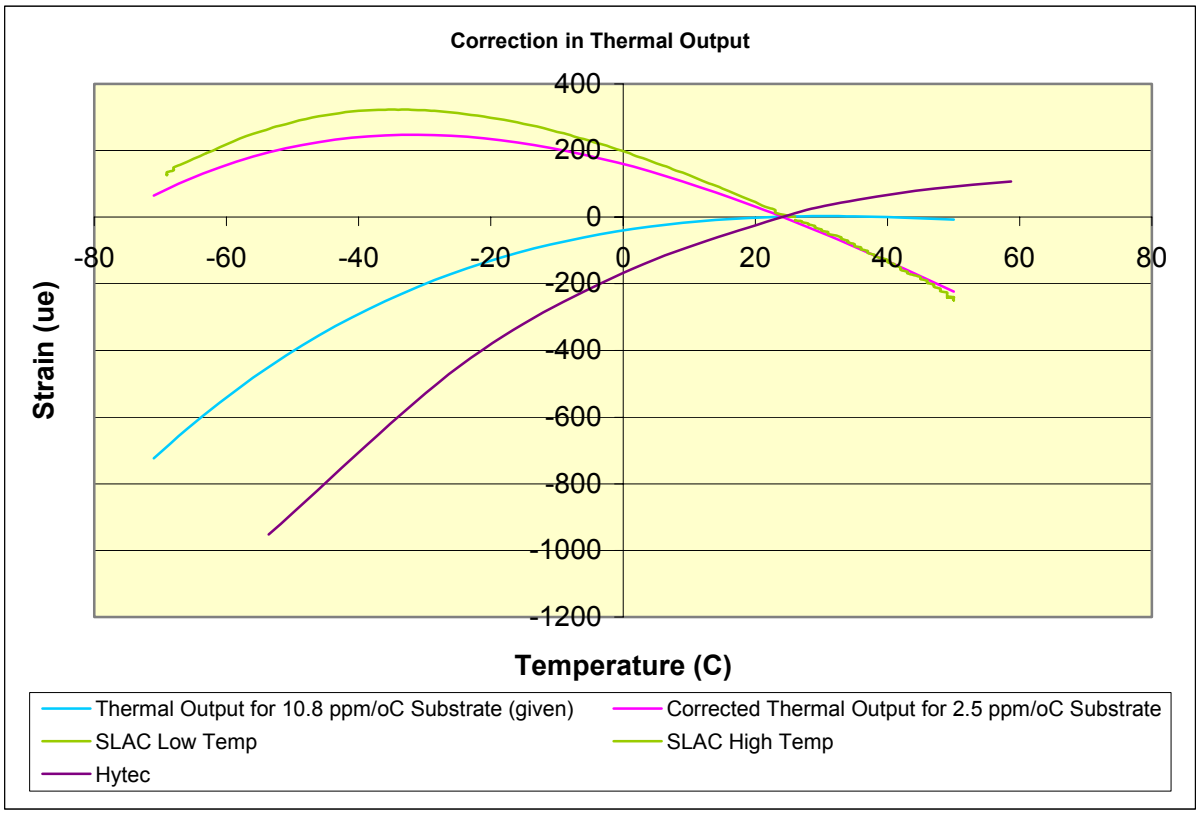


Figure 5. Comparison of Theoretically Determined and Measured Thermal Output.

The curves SLAC Low Temp and SLAC High Temp (both green) represent experimental data from the temperature regions below and above ambient, respectively. In other words, the closer the green line is to the pink line, the better the data matches what is predicted. The largest difference is at ~ -40 ^{o}C, where the percent difference is 27%. Upon consulting Vishay, this magnitude of error is common and this data can be considered legitimate. Unfortunately, there is no published specification for the closeness of fit for this relation. This is because of the large number of uncertainties involved with applying the gages, setting up the data acquisition, methods of thermal compensation, etc…

The Hytec curve is from their data[1] used to determine the CTE of silicon over the temperature range of interest in GLAST. This test was done as a validation of their test method, and the CTE relation obtained from their testing matched well with textbook data[1]. As can be seen in Figure 5, there is a large discrepancy in the Hytec data when compared to the expected corrected output. I spoke to Erik Swensen of Hytec about this

issue, and he said they may have used gages with CTE = 0 ppm/ ^{o}C. To this date, there has been no confirmation from Hytec on the CTE of the gages they used.

Discussion

The thermal strains induced in this testing far exceed those expected for the silicon detectors on GLAST. To illustrate this, spreadsheet calculations were done for the two candidate converter materials, tungsten and lead, for both thicknesses, 2.5% Radiation Length (RL) and 25% RL. Also, three types of adhesive were used in this comparison: a relatively compliant silicone, a relatively rigid epoxy, and a candidate electrically conductive candidate adhesive, Nusil CV-1500. The normal stress in the silicon was calculated for the above configurations at -60 ^{o}C (ΔT = -85 ^{o}C), and then compared to the stress predicted in the sample sandwich at the same condition. Figure 6 shows this comparison.

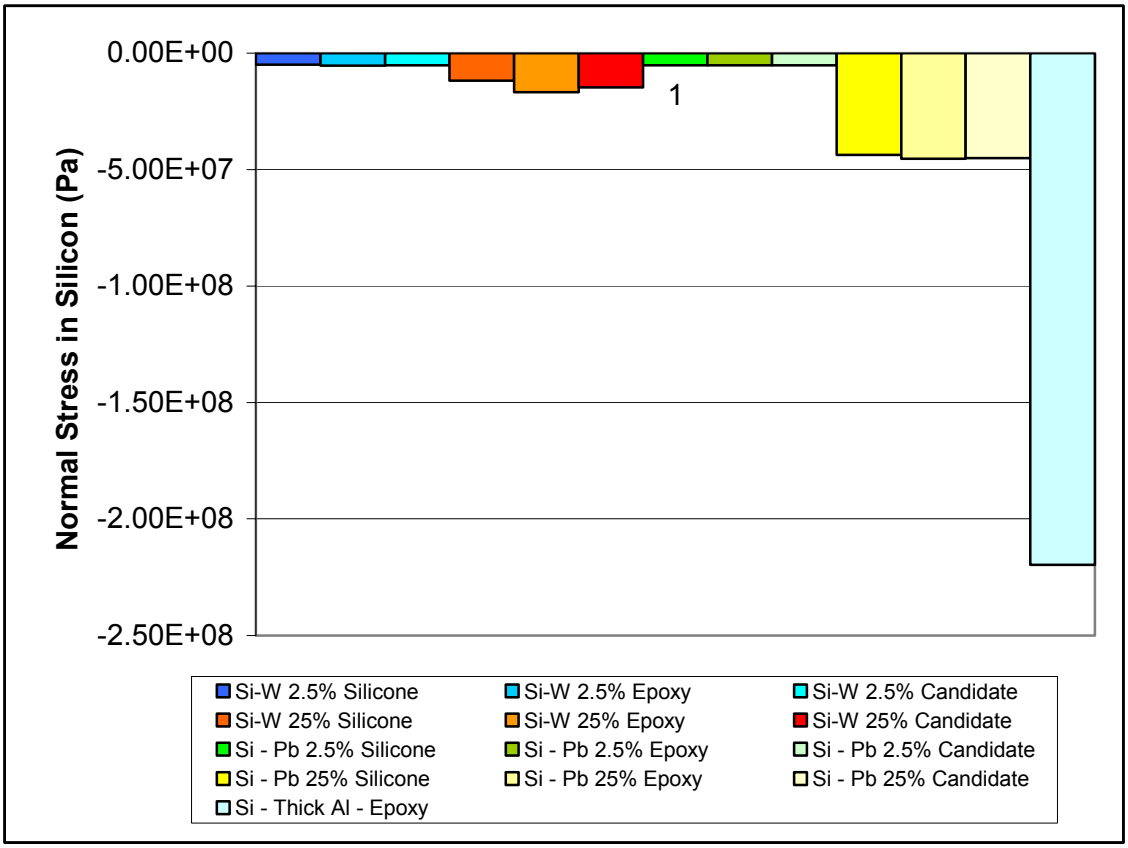


Figure 6. Comparison of Silicon Normal Stress in Various Fight Configurations and in Test Configuration Under Identical Environmental Conditions.

Figure 6 clearly shows how the stresses induced in the silicon from the testing far exceed those expected in orbit, regardless of the configuration.

Next it was desired to compare the compressive strain levels achieved with the aluminum substrate to the maximum compressive strain that would occur if the semi-infinite

substrate were lead, the candidate converter material with the highest CTE. This strain level can be determined from the following equation:

$$\varepsilon = \alpha \Delta T \quad (3)$$

Where:
ε = Strain in Pb (ppm)
α = Linear CTE of Pb = 29 ppm/ ^{o}C
ΔT = Change in Temperature = -55 ^{o}C (@ -30 ^{o}C)

Using the above stated values in (3), ε = -1595 $\mu\varepsilon$ (note: 1 $\mu\varepsilon$ = 1 ppm). Knowing that the CTE for the Al is 23.6 ppm/ ^{o}C, the equivalent temperature change can be determined for the Al to produce -1595 $\mu\varepsilon$. This temperature change is - 67.6 ^{o}C, and from ambient this corresponds to a temperature of - 42.6 ^{o}C. As previously shown, both sandwich samples were tested to - 60 ^{o}C. Therefore, the use of Al instead of Pb is adequately accounted for, and with significant margin.

Due to the large temperature excursions involved in the testing and analysis described in this report, the assumption that material properties are constant functions of temperature is not always valid. Due to the limited time available for testing and analysis, not all teperature dependant properties have been considered. The primary areas where these assumptions may effect the results are in the spreadsheet calculations used to predict the stress in the silicon. Additionally, a generic value for the shear modulus of the adhesive, G = 655 MPa, was used. This value does not necessarily correspond to the GE 2216 adhesive used, but is a representative value for epoxys provided by Hytec[2]. An approximate value was used because the manufacturer does not supply a value for this property.

Conclusion

Sandwich samples were constructed that include worst-case scenario parameters for the silicon detector tiles on GLAST. These samples were driven far beyond the stress limits expected in the GLAST mission and did not fail. The samples tested previously by Hytec that failed used a non-symmetrical gluing pattern that may have caused unnecessary bending in the silicon detectors. Therefore, a more symmetrical gluing pattern is recommended to reduce bending of the silicon.

Recommendations

These tests eliminated any significant bending in the silicon due to the continuous attachment of the wafer to the Al substrate. The sparse and unsymmetrical gluing pattern used to bond the detectors that Hytec tested most likely resulted in significant bending and even torsion of the wafer, resulting in failure.

Further thermal testing, using the same strain gage techniques employed herein, should be performed on a wafer bonded to a substrate more representative of the flight configuration using a symmetrical adhesive pattern of dots that are relatively close together. This adhesive would preferably be a rigid epoxy similar to the GE 2216. A rigid epoxy is desirable because it can be compressed down to much thinner bondlines than a silicone adhesive, hence reducing the overall mass of the detector assembly. Also, the survivability of the silicon under high thermal stresses has been demonstrated and hence the superior strain transfer characteristics of the epoxy are not an issue. The substrate should include the kapton layer bonded to the most promising converter material.

Next, a series of tests using live silicon strip detectors should be planned to characterize the relationship of leakage current to strain and temperature.

Due to the high number of variables involved in the proposed attachment procedure for the silicon detectors (e.g. adhesive coverage, residual stresses from room temperature cure, etc…), it is advisable to thermally cycle all detector assemblies intended for flight. This process will both relieve residual stresses between at the silicon/adhesive interface and serve as a thermal qualification of the hardware.

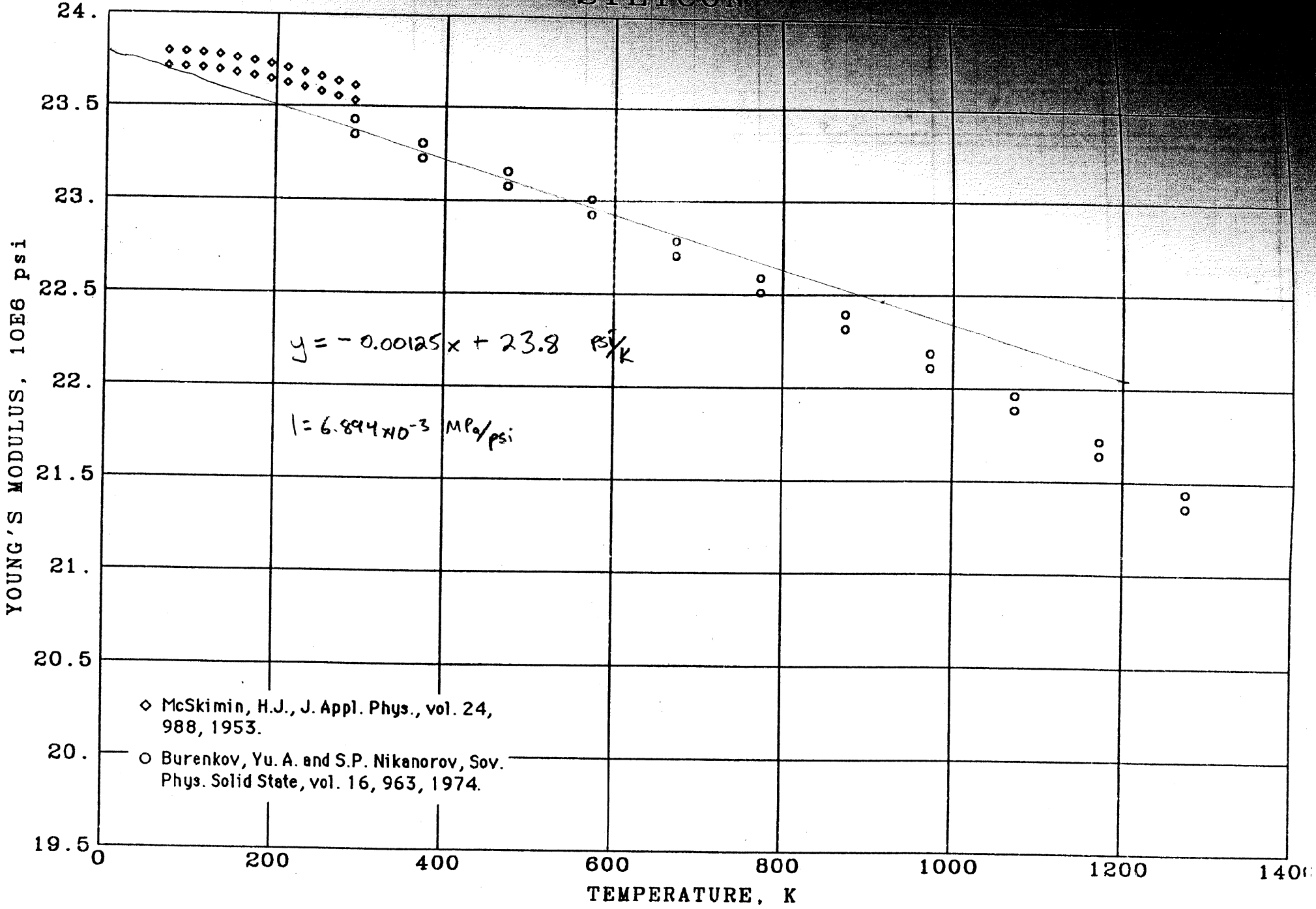
References

1. "GLAST Prototype Tray and Ladder Thermal Test Report", Mike Steinzig, Erik Swensen, Steve Ney, Hytec Technical Note HTN-102050-012

2. "Investigation of Compliant Layer in SuperGLAST CTE Mismatch Problem", Steve Ney, Erik Swensen, Eric Ponslet, Hytec Technical Note HTN-102050-018

3. "Strain Gage Temperature Effects", Measurements Group Technical Note 504, http://www.measurementsgroup.com/guide/tn/tn504/504i.htm

SILICON



Source: "Materials Handbook for Hybrid Microelectronics", Joseph Allen King, 1988