Glast Tracker Electronics Meeting 05/03/00

Assembled by G. Haller, SLAC

1. Attendees:

UCSC: R. Johnson, H. Sadrozinski, W Kroeger, N. Spencer
SLAC: D. Nelson, J. Olsen, D. Freytag, G. Haller, JJ Russell, T. Waite
SU Campus: R. Williamson, J. Wallace, B. Bumala, D. Lauben, S. Williams

2. Summary

2.1. Technology for Custom Chips

The HP 0.5 um process is still the target. Robert mentioned that there is a paper (Osborne, et al) reporting that the latch-up threshold was found to be higher than required by NASA. There is a possibility of investigating the sensitivity in a beam in Japan in July, but the question is whether the electronics effort for that can be supported. It was also mentioned that one should investigate further SEU/SEL testing via NRL. Presently the TKR project relies completely on the HP process suitibility, so it is very important to prove soon that the process can be used. The issue came up if the process can be used, why do other front-end systems target a rad-hard process?

In order to improve the digital/analog cross-talk, the analog/digital ground were separated on the FE chip. There is however the concern that will (considerably?) increase the latch-up problem. This needs to be addressed.

2.2. Custom Chips

FE chip: a modified version of the analog part of the FE chip was submitted last week in the HP 0.5 um process. The present plan is to submit the next complete FE chip by the end of this year. The amplifier circuits will undergo further review/improvements to obtain the best possible phase-margin, process parameter insensitivity, neighbor channel crosstalk etc. One digital modification will be to include consistency checking/monitoring bits. Each FE chip should write a write-buffer number into the buffer used for the L1 accept. In addition the buffer number read-out at Read-Event time should be returned. This results in 4 or 6 bits per FE chip, depending whether there are 4 or 8 FE buffers. Those bits can be compared and stripped by the controller chip and a single error-bit per controller set if the FE buffer numbers don't match the numbers the controller chip expects.

Robert mentioned that he has access to an SEU resistant memory cell design which should be laid-out/fabricated for possibly use in the configuration registers.

Controller chip: the present version needs some modifications. The TKR group voiced the interest to remove the TOT circuit from the controller chip and move it to the TEM. That circuit is the most complicated part in the controller chip design. That however requires additional circuitry on the TEM, J. Wallace will investigate the consequences in case one decides to move the circuit.

LVDS compliancy: presently the controller chip does not comply with LVDS standard in order to save power (200 ohm termination). This however can affect the noise margin, etc. Robert will report the required increase in power if the interface is made LVDS compliant. This is the preferred solution if the impact is small. Alternatively test with the non-compliant circuit are required.

The CRC added on the controller chip should be checked and removed by the TEM to reduce the data-rate off the TEM. The CRC information from the controller chip has not yet been looked-at. For the test-beam the function was turned off and no data is available. It was proposed that the TKR/TEM should be run with the CRC enabled to investigate the bit-error rate. D. Lauben will take the initiative.

Additional modification in the controller chip are being investigated to make the TKR system and the CAL/ACD systems more uniform as seen by the DAQ. Details are being worked on.

Robert mentioned that the present controller chip design is available in VERILOG. He will give a copy to D. Nelson.

2.3. Number of buffers and data-rate

It was reported that 4 buffers seem to be sufficient as opposed to the present 8-buffer system. This simulation however assumes that there is no buffer use due to "back-up" of events due to data-rate limitations off the TEM to the processors. The J. Wallace/D. Lauben will investigate further.

D. Lauben showed some preliminary results of simulations of the data-rate off the TEM.

JJ Russell is working on the preferred data-format for the software. A proposal is expected within a week.

2.4. TOT/dead-time/dynamic range

Presently the dynamic range of the TOT circuit is 25 MIPS. The dead-time of a tower can be 100 usec for large signals. Apparently the TOT is only used for ground-based two-track seperation. It was mentioned that a 20-30 usec range would be sufficient, which maps into a 4-5 MIPs dynamic range. In order to make progress advise of Steve Ritz is required:

Is the TOT really required on each event? (TOT is up to 33% of the TKR data rate)

What is the dynamic range/TOT range required?

This question should be answered in the next 6 weeks.

There is a risk of the use of a hard-reset to limit the TOT (cross-talk/ circuit complication), so it should be avoided.

B. Bumala showed TOT results from the beam-test show i.e. distributions as a function of MIPS. There were some questions which require a meeting between Bob and Eduardo. In the test-beam noisy channels were not masked off which will affect the TOT measurement. They will investigate further.

2.5. Latency of trigger signals

Robert showed some plots showing typical latencies of the layer-or of 550 ns to 700 ns. There is a discrepancy to the numbers measured by J. Wallace (100-150ns) which need to be found.

Wilko reported that the smallest latency measured via charge-injection was 260 ns.

The question of how late the TKR can receive the TRG ACK signal after the event time came up. The TKR group stated that 2 usec is fine to still get the required efficiency. (The test-beam was operated around 2 usec). W. Kroeger will make more tests.

2.6. Self-triggering

Robert reported that the likely cause of the self-triggering problem is the turn-on of the 20 MHz clock to the FE chips for read-out of the shift-registers. This may be due to a sudden, dramatic increase in digital activity causing an increase in current flowing from DVDD to DGND. This will raise slightly the potential of the ground system. In order to prove the cause, tests with a continuos clock should be undertaken. This is possible via a bit set in the controller chip, although the controller chip turns the clock automatically off after read-out and has to be turned on again via a command. The cause of the self-triggering problem must be found and fixed.

2.7. Power supplies

UCSC received a Perugia-made (in coorperation with CAEN) power-supply. It comprises 120V/5V DC-DC + filtering + linear regulation. It can be used with or without the linear regulation. Apparently it was used for AMS and has 65-70% efficiency. There are no test results yet with the TKR electronics. The weight and power rating should be determined.

The question came up what the noise requirement are for the supplies. This is a very important parameter which can limit the efficiency. It was proposed to connect several styles of power-supplies to the TKR and measure when the performance degrades. Alternatively a variable noise source can be added at the supply. Measurements are needed.

The DC operating range of the circuits should be measured as well as the AC sensitivity (ripple and short-term voltage change due to current change)

The TKR group is concerned about the low 13% power margin. The AO PS efficiency of 84% seem very high in view of the noise performance required. The power margins of the whole instrument need further evaluation.

2.8. Cable/grounding

UCSC plans on shielding the kapton cable on both sides. Presently the shield, analog ground and digital ground are connected at the base of the TKR.

A grounding and shielding plan for the TKR has to be provided. Robert has asked M. Nordby on the possibility of electrically isolating the GRID and the TKR.

The IR drop on the kapton cable needs to be measured in order to determine whether it is acceptable. Changes of voltage as a function of instantaneous current increase and the effect on the circuit is the issue.

2.9. Balloon Flight

The plan for the balloon flight is to fly the test-beam TKR electronics. This is independent on at what date in 2001 the flight is scheduled.

Robert is considering removing the super-glast layers, tbd.