GLAST Silicon Microstrip Tracker Electronics

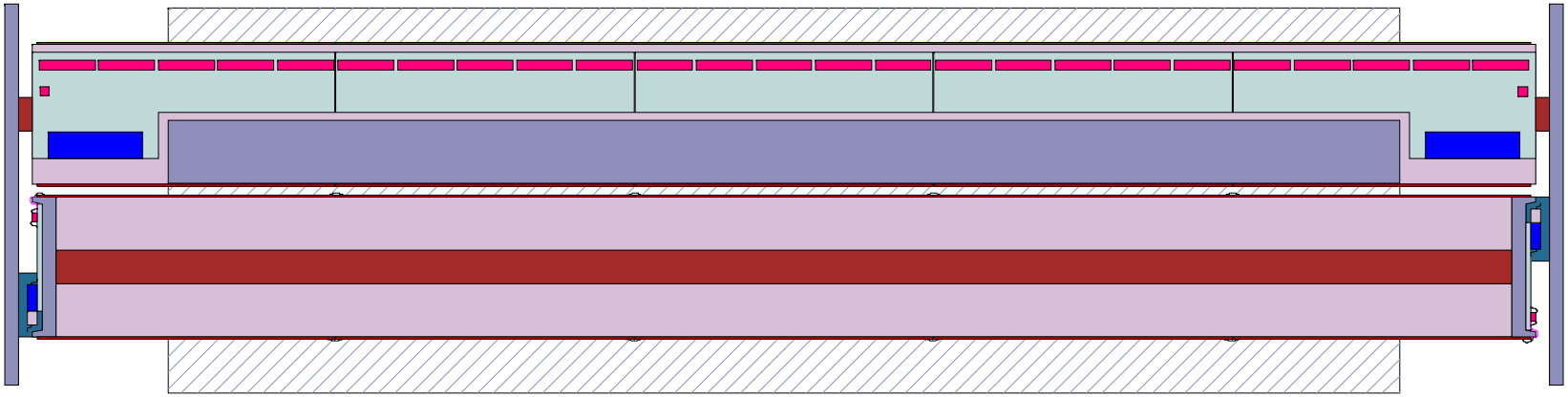
Front-End DAQ Status

Goals

- Redundancy
- Minimize cabling and interconnections
- Sparse readout
- Low power
- Minimal digital feedback into amplifiers

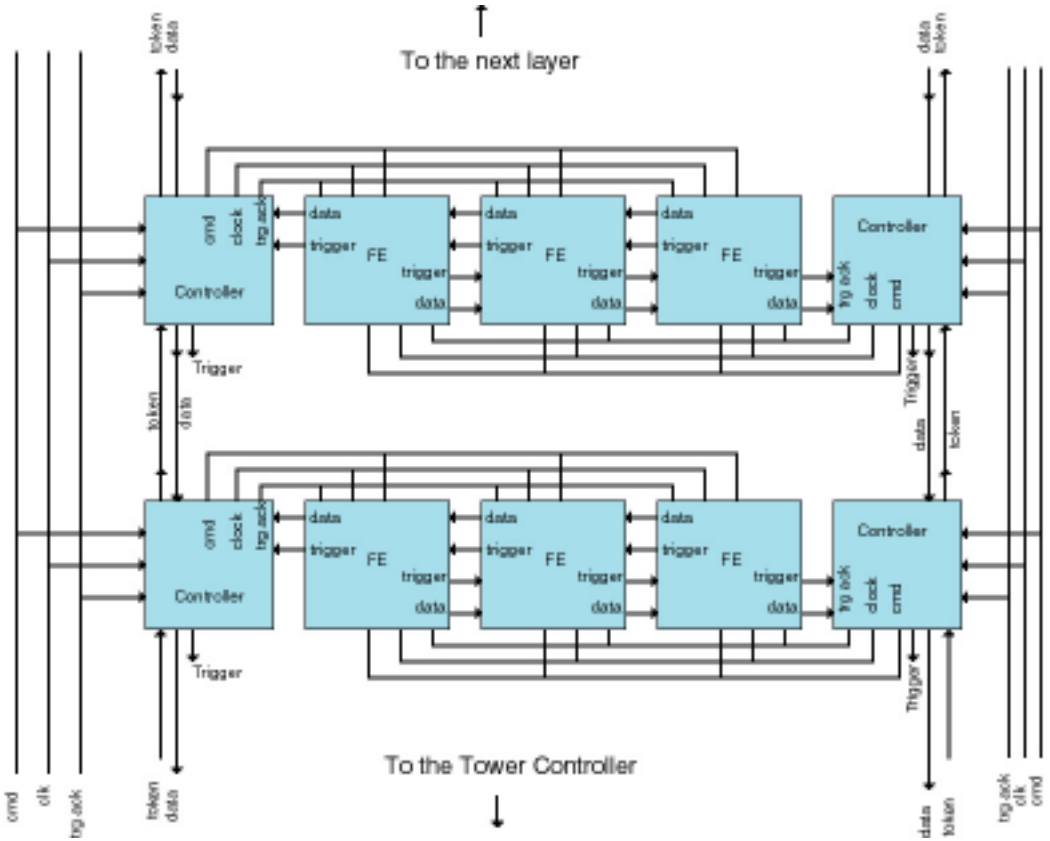
Assumptions

- 16 layers per tower side (or up to 31)
- 25 readout chips per layer
- 64-channel readout chips
- Data truncation at 64 hits per layer



Readout Architecture

Only 3 of 25 readout chips per layer are shown here.



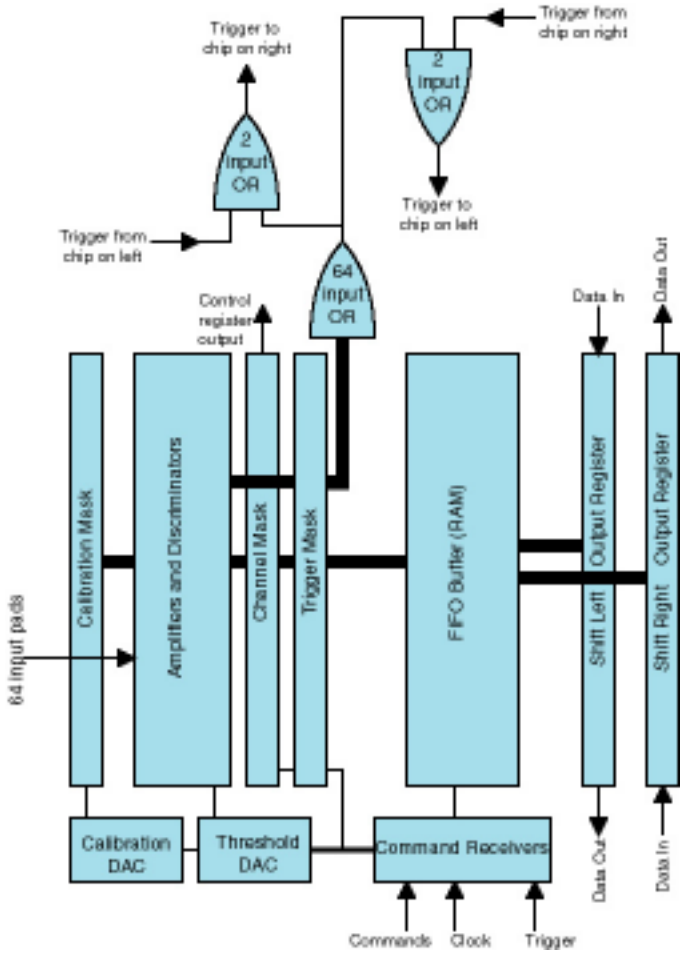
- Redundant controller chip at both ends of the readout chain in each layer.
- Either controller can program any of the 25 readout chips to shift data and trigger signals in its direction.
- Data are passed down a long shift register from chip to chip.
- Empty chips send only a single bit; chips with hits send 65 bits.
- Trigger outputs form an up-to-1600 fold logical OR.
- Data are read from the controller chips serially in a token-controlled daisy chain.
- Trigger *and* trigger acknowledge signals have a separate transmission line per side per layer.

Signal Transmission

- Signal transmission must take into account power and noise. The front-end amplifiers *must* operate during digital clocking and data transmission, but the power budget is only about 80 mW per layer.
  - Chip-to-chip data: 3V differential CMOS
  - Chip-to-chip trigger: low-voltage differential
  - Controller chip to front-end chips: low-voltage-swing differential switched current
  - Controller chip to controller chip and to/from tower controller: not yet designed but must be differential.
- Designed for 20 MHz clock, but with considerable margin.
- Except for chip-to-chip data and, possibly, controller-to-controller, comparators are needed to receive the signals. This uses some DC power but is essential for preventing pickup by the front-end amplifiers.

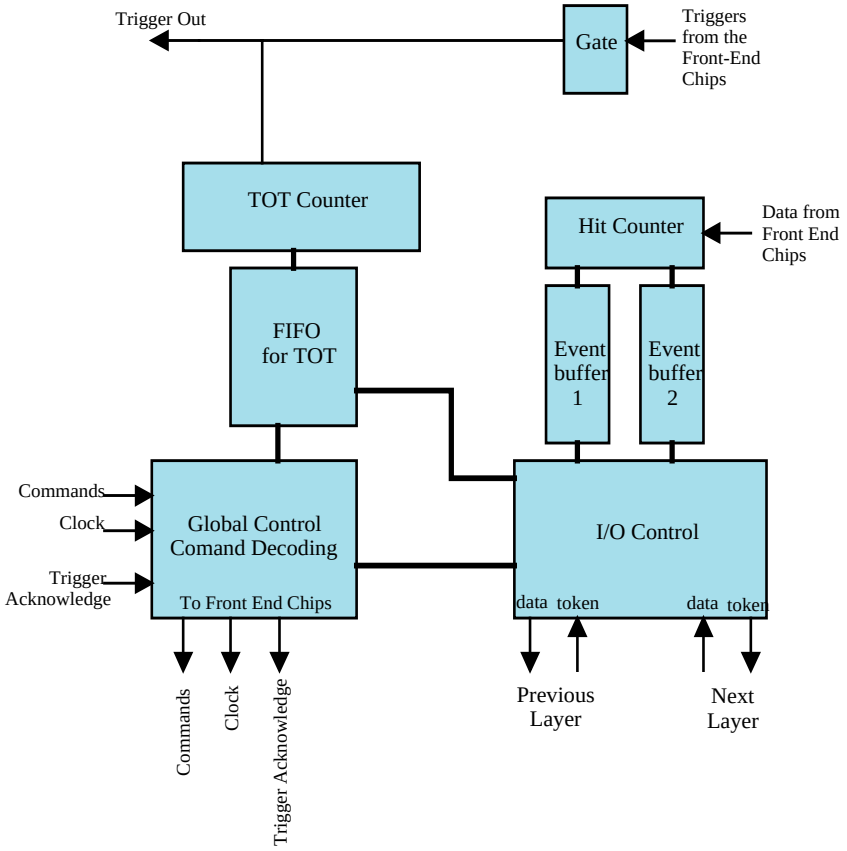
Front-End Readout Chip

- 207-bit control register
  - 64-bit calibration mask
  - 64-bit trigger mask
  - 64-bit data mask
  - 7-bit calibration DAC
  - 7-bit threshold DAC
  - 1-bit left *vs.* right control
- 7 addressable serial commands
  - load control register
  - read event
  - end read event
  - clear event
  - calibration strobe
  - reset chip
  - reset FIFO



Readout Controller Chip

- 10-bit control register
  - Number of chips to read out
  - Calculate an 11-bit check-sum?
  - Require x-y coincidence?
  - Require a trigger from this layer?
- 8 addressable serial commands
  - load control register
  - clear event
  - read event
  - load front-end chip control register
  - turn on the front-end chip clock
  - calibration strobe
  - send reset to front-end chips
  - reset
- Format: *saaaaacccddd…*



Data Format and Protocol

- Each controller chip sends a variable-length packet after receiving the token. An empty packet (header only) is sent if there are no hits.
- There may be arbitrary spaces between packets.
- The token can come before the controller chip is ready *but* the tower controller has to manage the buffers in the front-end (8) and the controller chips (2) by counting read commands and tokens sent versus events returned.
- Packet format (Start bit plus 11-bit words):
  - Start bit—a single 1.
  - Layer address (5 bits), followed by number of hits *n* (6 bits).
  - Control code (2 bits), followed by time-over-threshold (9 bits).
    - Control bit 1: does the packet contain data or control register output?
    - Control bit 2: was the readout terminated early (truncated)?
  - Sequence of *n* hits, each with an 11-bit address for the hit channel in the layer.
  - 11-bit check-sum (optional).

DAQ Synopsis

- Trigger pulse generated by one or more front-end channels.
- Controller chip begins counting the ToT. Stops after 1.6 μs if no trigger acknowledge arrives.
- Within 1.3 μs a trigger acknowledge is received and front-end chips latch data into FIFO.
- Up to 8 more triggers can be handled before beginning a readout.
- Read-event command is sent and the first event is moved from the FIFO to the data register.
- The data are clocked into the controller chip, which builds a list of hits.
  - Token-controlled readout of the previous event from the controller chip's buffers can proceed at the same time, as can acquisition of new data by the amplifiers.
  - If the controllers receive another read-event command before the data are clocked out, then the readout is truncated and clocking out of the new event begins.
- Tower controller starts a token going up the tower to read the data packets from the controller chips.

Cabling

- Two kapton flex-circuit cables on each side of the tower (8 cables per tower).
- 51-pin single-row 25-mil pitch Nanonics connector at the tower controller end.
- 25-pin connector on each end hybrid.
- Multilayered cable provides shielding and controlled impedance.
- All digital signal lines are differential side-by-side traces.
- 11 traces are bussed to all layers:
  - Analog power and ground, digital power and ground.
  - Detector bias.
  - Clock and commands.
- 32 traces go to just a single layer each:
  - Temperature monitoring.
  - Trigger output and trigger acknowledge input.
- 8 traces are daisy chained from layer to layer:
  - Token passing up the tower.
  - Data flowing down the tower.

Status

- Front-end readout chip: final layout details and verification (simulation, lvs, drc) are in progress. Test DACs in November. Submit prototype Dec. 10.
- Controller chip: HDL and state diagrams are well in progress. Logic design will be done by automated synthesis. Layout will be mostly done with DoD designed standard cells by automatic place and route. Submit Jan 20, 1998.
- Hybrids: 30 of the central hybrids have been fabricated. The end hybrids are completely designed but await fabrication pending possible connector change.
- Kapton detector interconnect: submit for fabrication this week.
- Kapton flex cables: completely designed but await fabrication pending a final decision on the connectors. Some rework of the design is very likely.
- Detectors: first batch due to arrive in December, 1997.

- A DAQ system will be needed for testing all of this hardware on the time scale of June 1998!