ASIC Development for the GLAST Tracker

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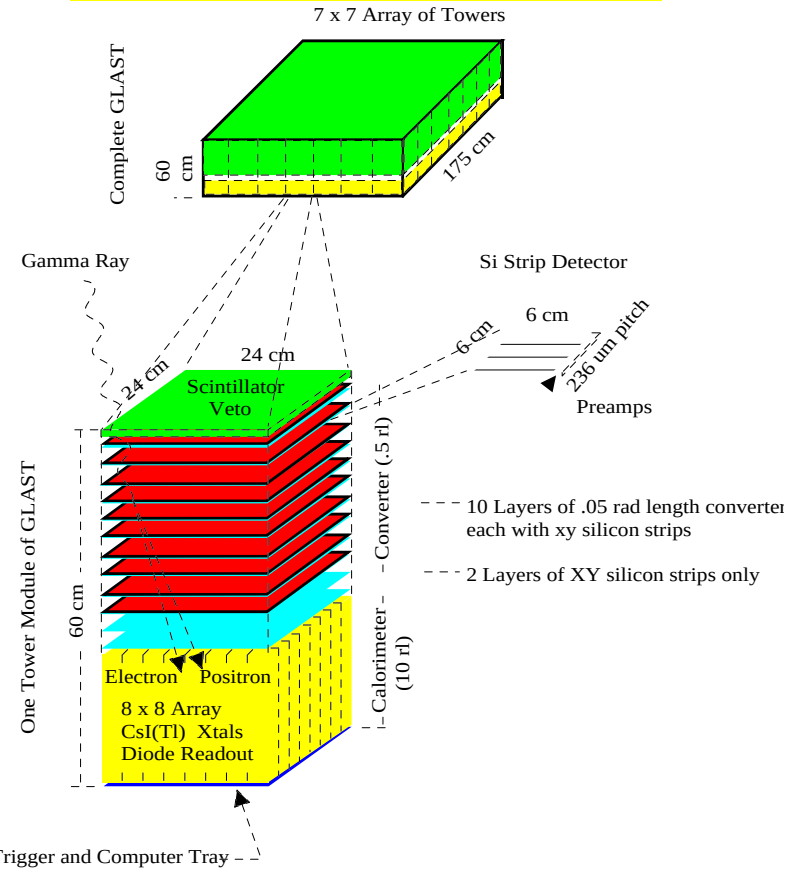
The GLAST Instrument Concept

An assembly of identical modules, each with a veto shield, a silicon-strip tracker, and a calorimeter.

The current tracker baseline design calls for 32 cm square detector planes, each with a 5×5 array of 6.4-cm detectors.

GLAST conceptual design. (The current baseline design is for a 5×5 array of 32-cm square towers, each with 16 x,y layers.)



Electronics Requirements

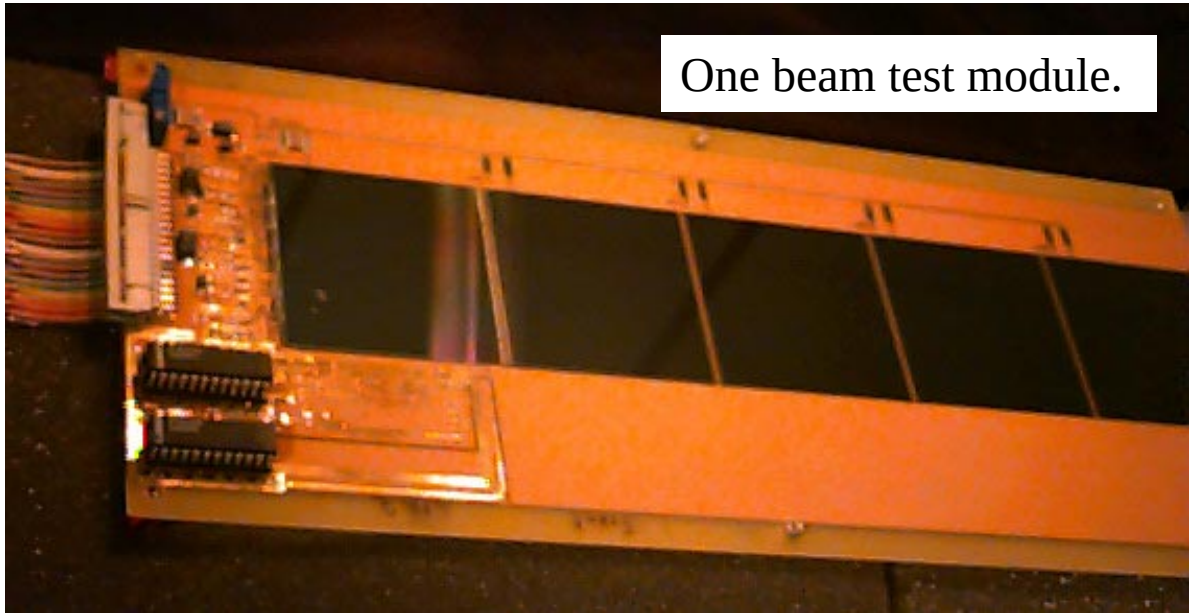
Challenge: 1.3 million readout channels operating with high reliability in a space environment.

- Power less than ≈250 μW/channel, including amplifiers and digital readout.
- Low noise occupancy (<0.05%) and good threshold uniformity.
  - Expected detector loading is about 1.2 pF/cm × 32 cm = 38 pF.
  - Detector thickness is 400 μm, for about 5.3 fC/MIP.
  - AC coupled detectors, with 194 μm pitch.
- Microsecond peaking time for the amplifiers.
- Sufficient redundancy to be immune to single-point failures.
- Self triggering.
- Radiation hard to 10 kRad with latch-up immunity.
- <1% dead-time at a 10 kHz trigger rate.
- Sparse readout and data formatting close to the front end.

Analog Channel

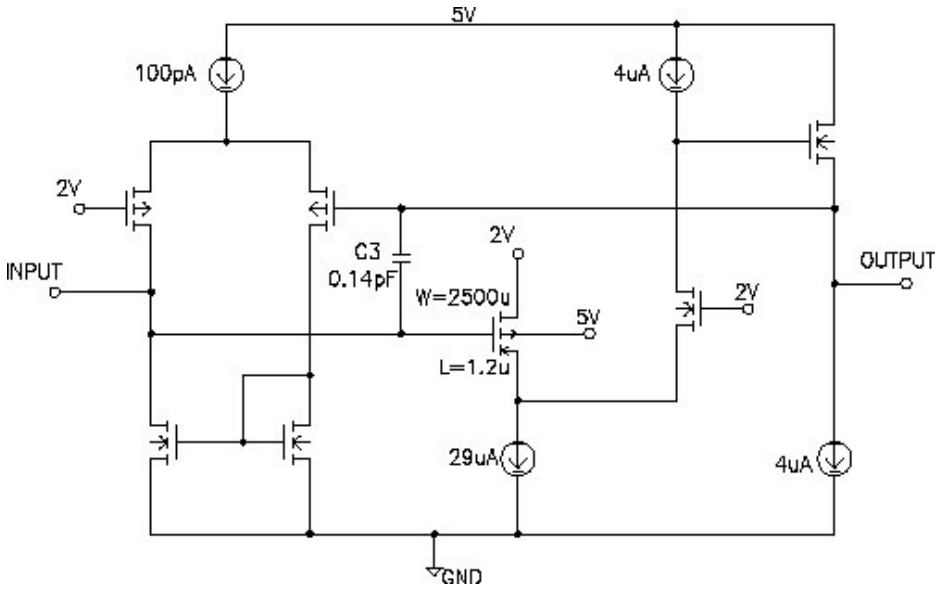
- A first 16-channel prototype was fabricated and tested one year ago.
- Later, a 32-channel version was produced for the recent beam test at SLAC.
  - Slightly reduced peaking time (1.3 μs, down from 1.6 μs).
  - Slightly reduced gain (125 mV/fC, down from 150 mV/fC).
  - OR gates for trigger output, rather than open drains.
- Extensive bench-top noise measurements have been done on several 16-channel chips.
- 71 32-channel chips were run successfully in the beam, but the data analysis has only begun.

HP CMOS26G process
(0.8 μm, 3-metal, N-well)


One beam test module.

Preamplifier Design

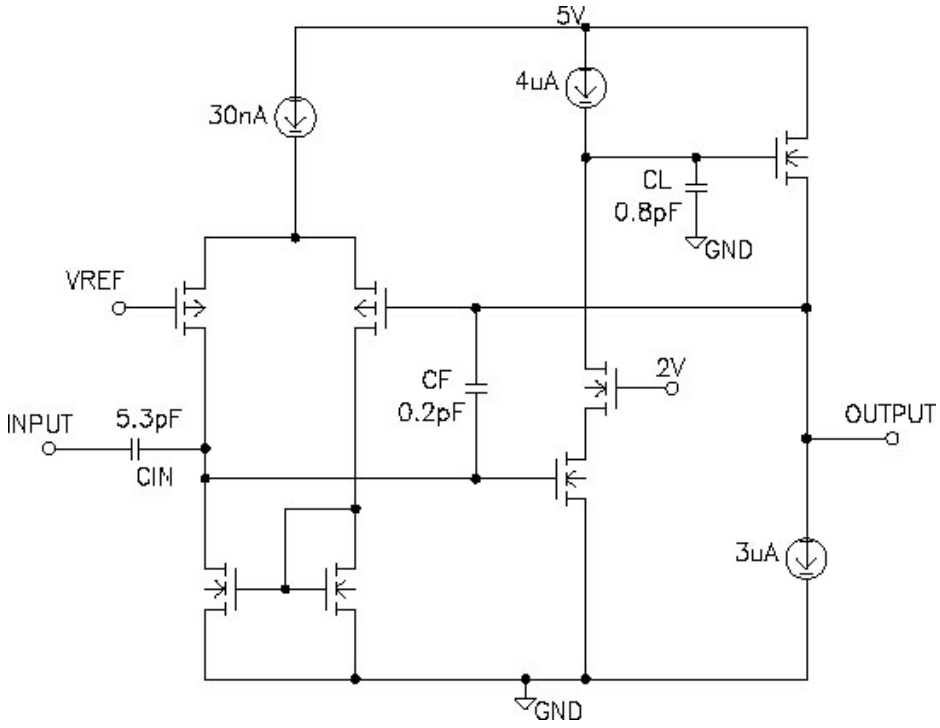
- Standard folded cascode amplifier with 2V bias for the front end, to save power.
- ≈25 μA bias current set by an external resistor.
- Slow differential amplifier stabilizes the bias point and provides a continuous reset.
- Input impedance ≈5 kΩ gives ≈200 ns time constant with GLAST 38 pF detector load.
- Open loop gain: 64 dB at 0 Hz
- Power: ≈90 μW



Preamplifier schematic.

Shaping Amplifier Design

- AC coupling from the preamplifier.
- Conventional cascode amplifier with capacitive feedback.
- Slow differential amplifier in the feedback provides the "differentiation" function *and* stabilizes the output bias point. (Ref.: I. Kipnis, LBNL)
- Open loop gain: 62 dB at 0 Hz
- Voltage gain: ≈26
- Peaking time: ≈1.3 μs
- Pulse shape: reset current source makes a tail that is more linear than exponential, except at the lowest pulse heights.
- Power: ≈35 μW

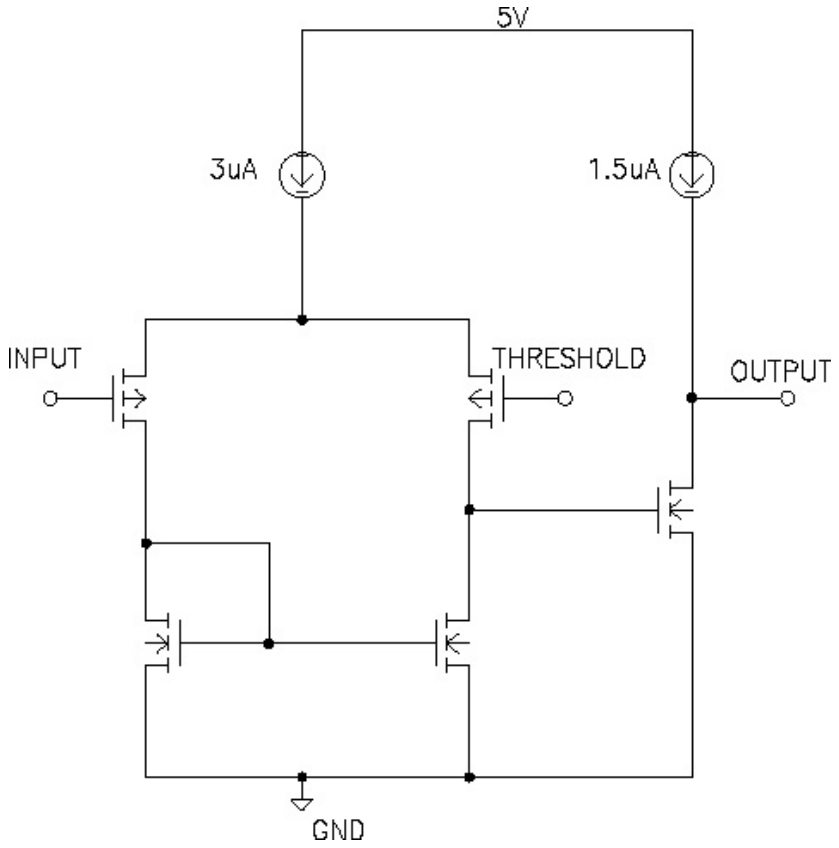


Shaping Amplifier Schematic

Comparator Design

Old Design

- 16-channel & 32-channel prototypes actually had NFET inputs. We need to go to PFET inputs (as shown here) to accommodate better the bias level at the shaper output.
- Conventional two-stage comparator, with DC coupling from the shaper output.
- No current in the second stage in the quiescent state (with no input signals).
- Only 17μW of quiescent power.

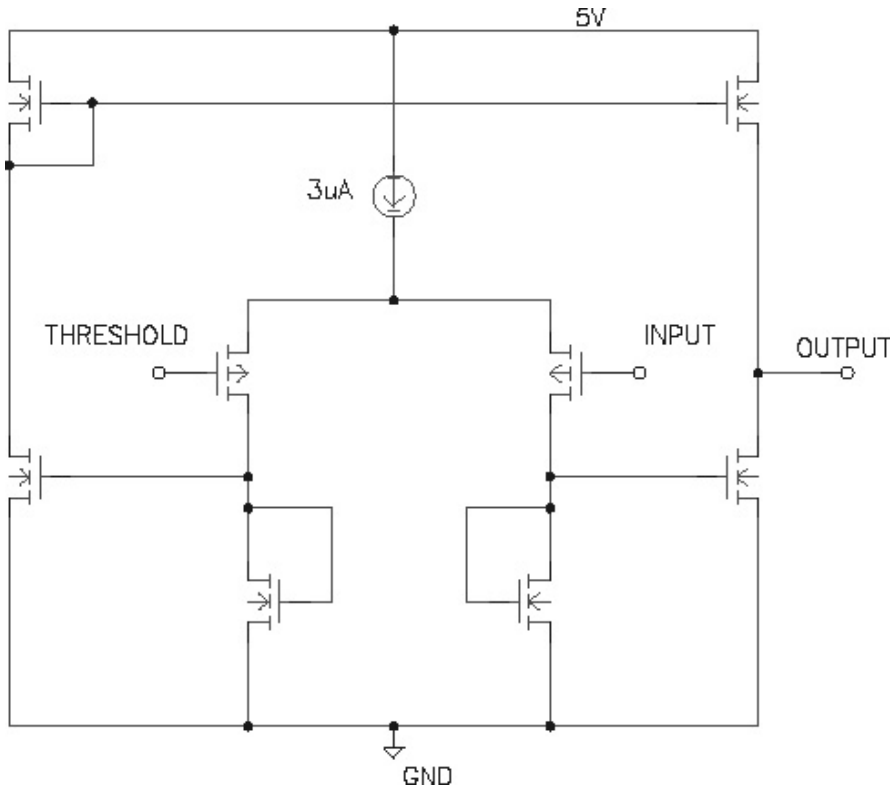


"Old" Comparator Schematic

Comparator Design

New Design

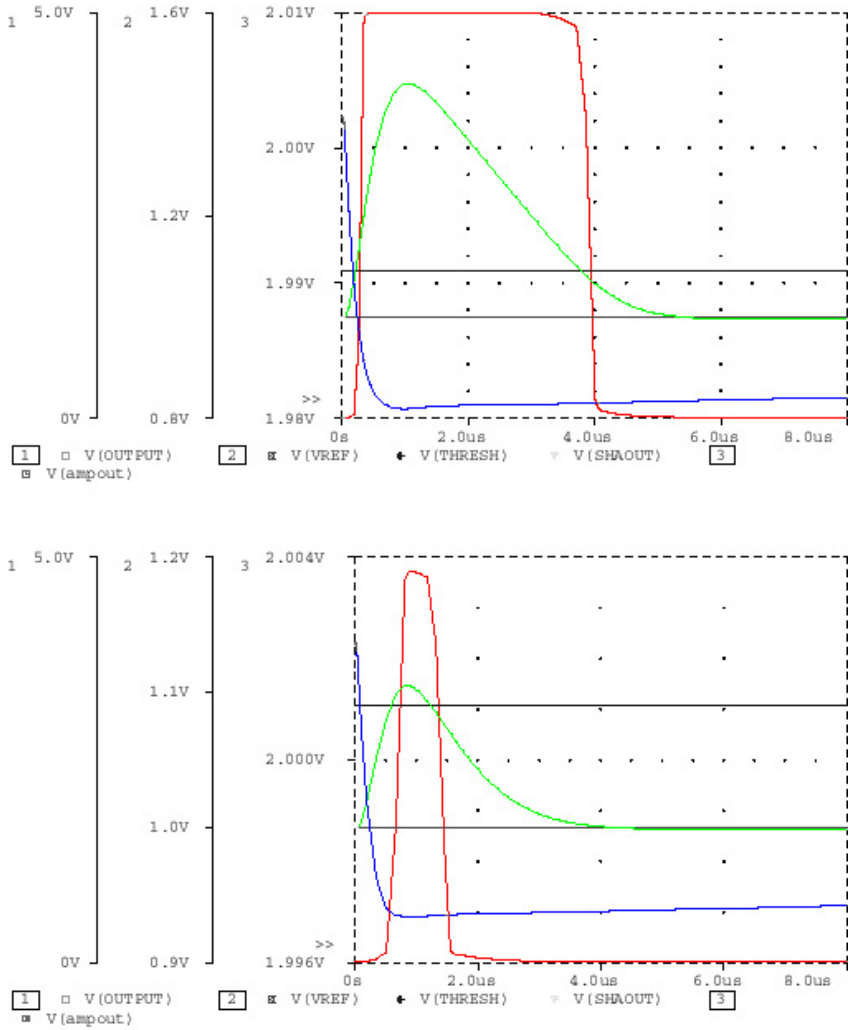
- Pavel preferred the symmetric design shown here, and this is what is in the layout at this time.
- Advantage: no coupling of the large output swing into the common bias network.
- Disadvantage: turn-on transition is not as abrupt as in the old design:
  - Old: $\Delta Q<0.04$ fC at preamp input produces a change at the comparator output from 0 to 5V.
  - New: $\Delta Q\approx0.28$ fC is needed to swing the output from 0 to 5V.
- I would like to change the comparators in at least 1/2 of the channels back to the old, proven design.



Analog Channel Signal Shapes

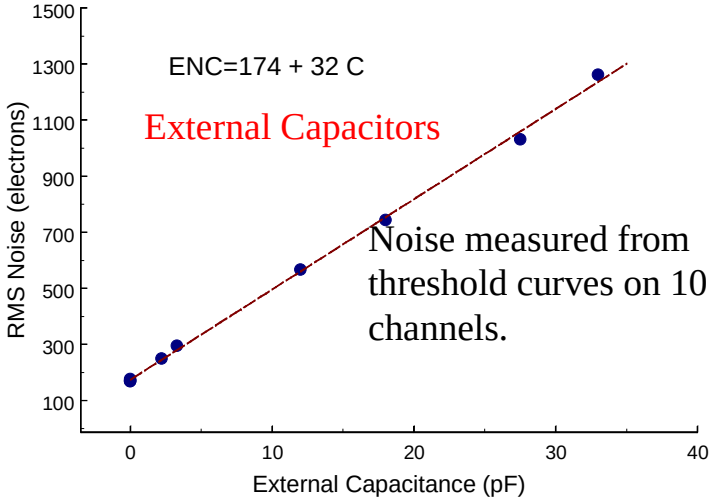
Spice Simulations

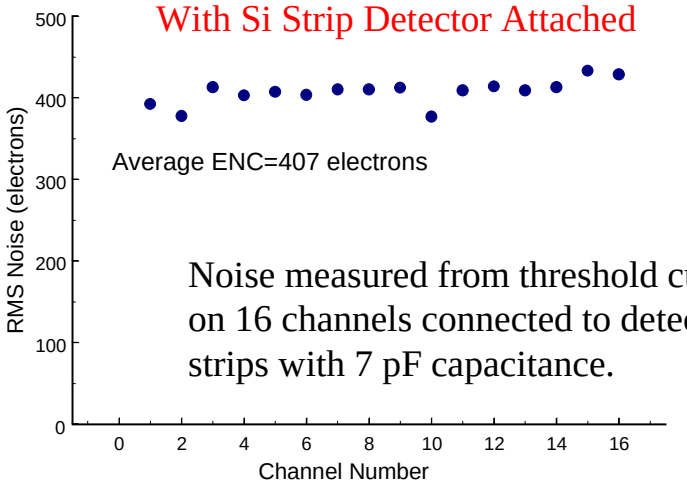
- Top: preamp, shaper, and comparator outputs for a 4 fC input charge.
- Bottom: 1 fC input charge.
- In both cases, the shaper baseline and the threshold (90 mV) are shown by solid black horizontal lines.



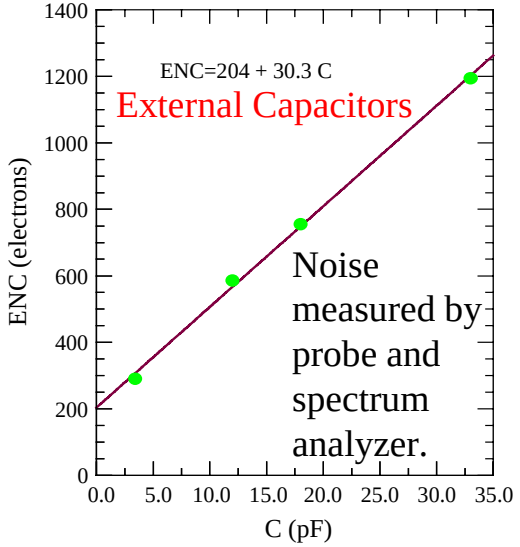
Analog Channel Performance

- Gain (shaper output): ≈150 mV/fC in 16-ch chip, ≈125 mV/fC in 32-ch chip.
- Peaking time:
  - ≈1.6 μs in 16-ch chip,
  - ≈1.3-μs in 32-ch chip.
- Power consumption, including bias circuitry: 150 μW/channel
- Noise: ENC=174 + 32×C electrons, with C in pF, measured by several methods, as shown here, for the 16-ch chip.



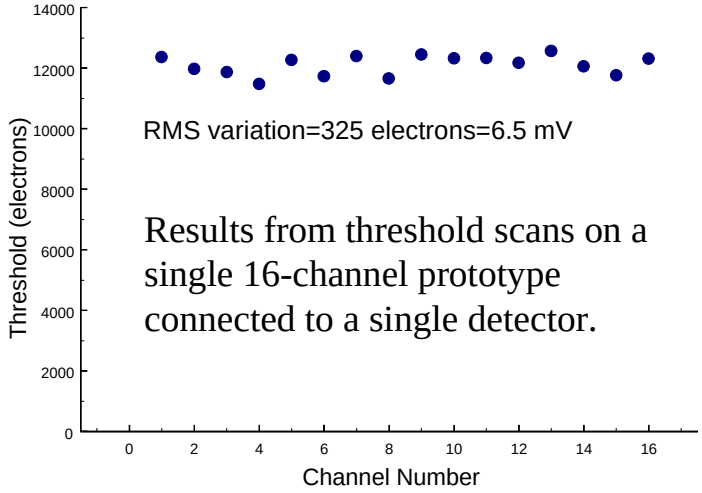


Channel 14 Noise

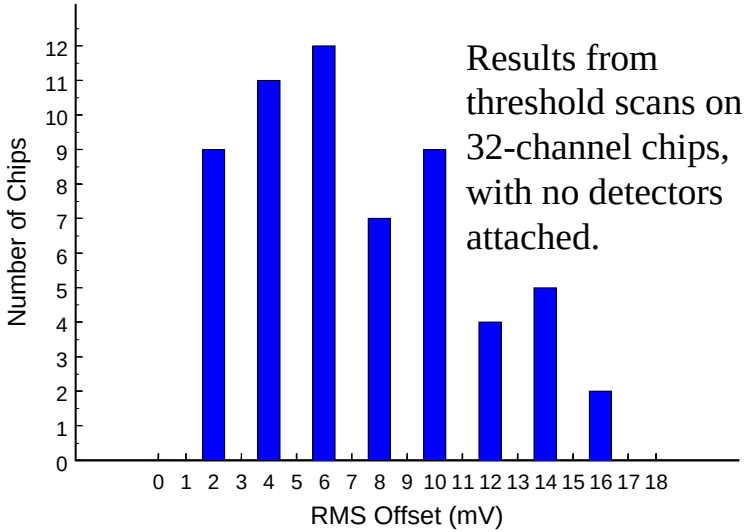


Threshold Matching

- Threshold matching from channel to channel across a given chip depends primarily on the transistor pairs in the shaper feedback.
- Most chips meet the desired upper limit of about 15 mV rms threshold variation (compared with the ≈32 mV rms noise level).
- Work is in progress to try to improve this figure further in the next prototypes.
- We plan always to have the capability to set the threshold independently for each readout chip, so chip-to-chip variations won't matter.



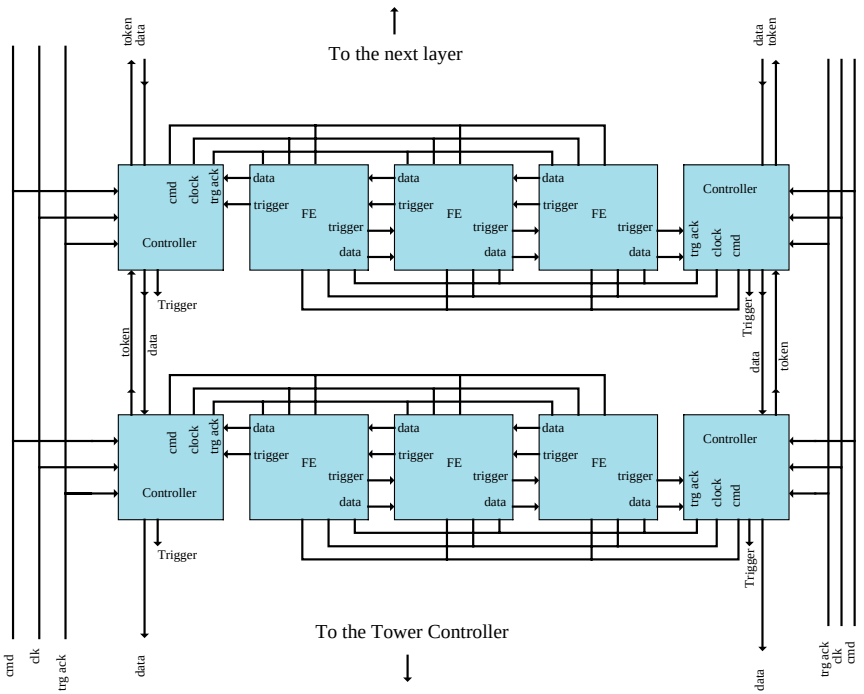
Results from threshold scans on a single 16-channel prototype connected to a single detector.



Results from threshold scans on 59 32-channel chips, with no detectors attached.

Readout Architecture

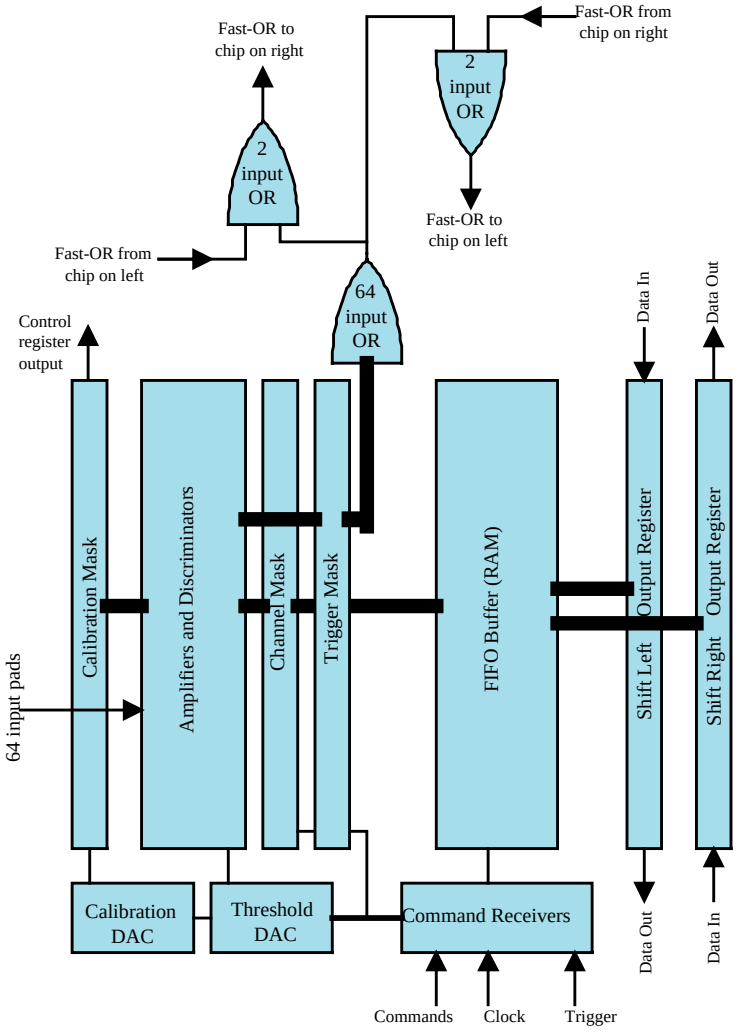
- 25 64-channel readout chips handle a single detector layer.
- Data can shift out left or right, or in both directions, with a readout-controller chip at each end of the chain. (20 MHz clock frequency.)
- Trigger-output (Fast-OR) signals also move left or right, or in both directions.
- Either readout controller chip can reprogram the readout direction of any of the front-end readout chips, so a single dead chip can be bypassed without losing data from any other chips.
- The readout controller chips pass data down the tower in a token-controlled protocol.



Simplified block diagram of the readout of a GLAST tower, showing only 2 of 16 layers and only 3 of 25 readout chips on each layer.

Front-End Readout Chip (GTFE64)

- The 64-channel chip currently being designed has the following additional features:
  - Calibration mask, to select any subset of channels to be pulsed.
  - Two 7 bit DACs, for setting calibration and threshold levels.
  - Separate masks for data and trigger output (Fast-OR).
  - 8-deep FIFO event buffer.
  - Dual redundant serial command decoders.
  - Dual redundant output shift registers and trigger outputs.
  - Bypasses to avoid clocking out data from empty chips.
  - External communication via low-voltage-swing differential signals.



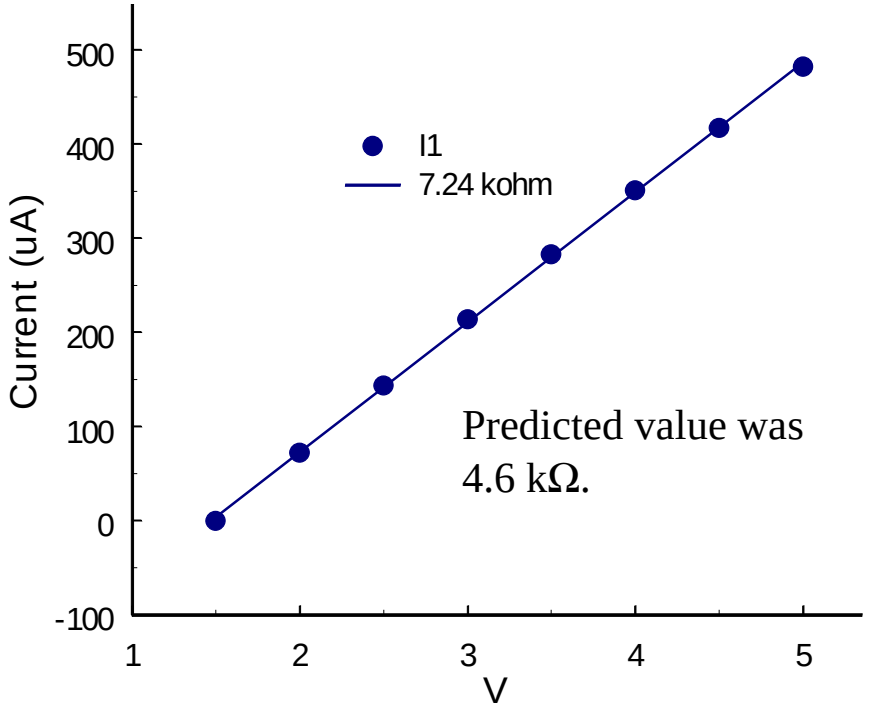
Resistors

Resistors are used in several places in the design:

- The DACs
- Drivers and receivers (to reduce dependency of the power consumption on the supply voltage)

However, the CMOS26G process has no really good way for making even moderately large resistors. Therefore, we have resorted to using N-well structures for that purpose.

We made a test chip that includes some structures for testing the method that we employ to make large resistors in this process (N-wells).

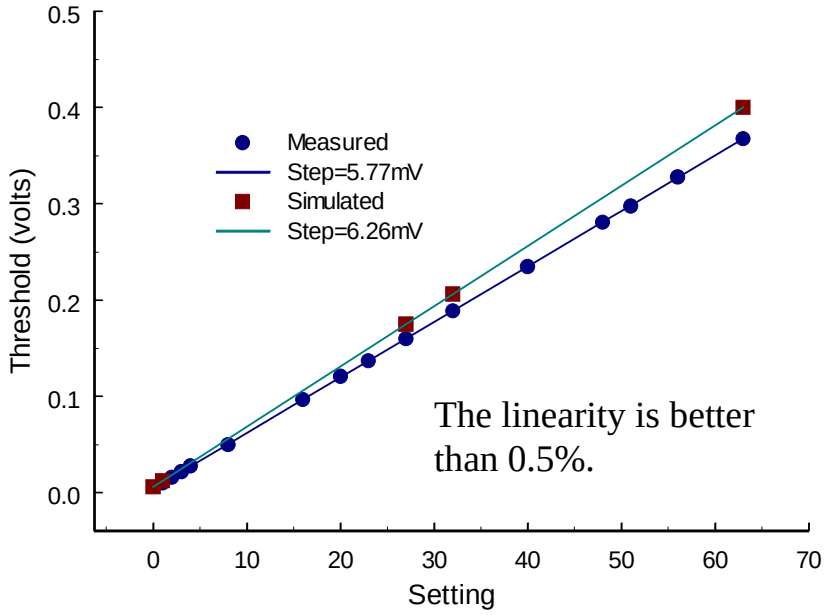


The resistance is nearly a factor of two higher than what we anticipated.

This is being corrected accordingly in the layout.

Threshold and Calibration DACs

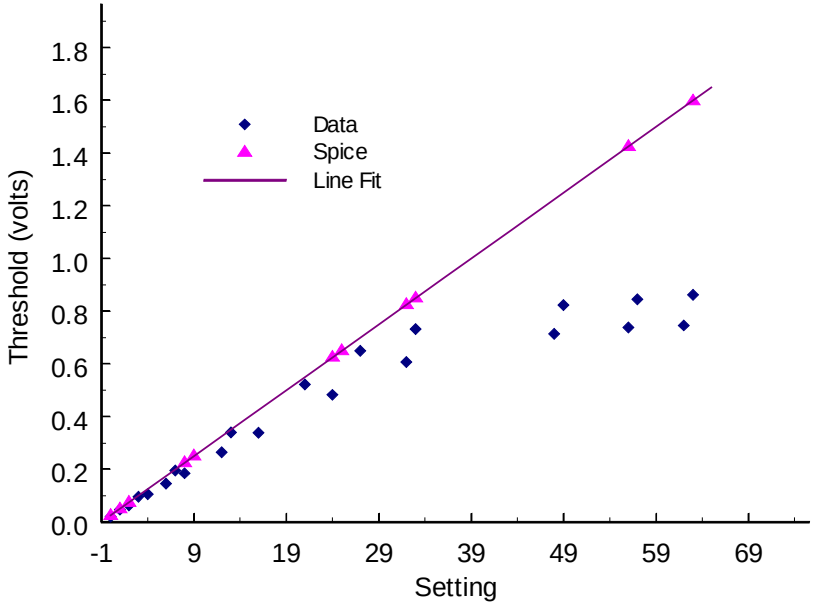
- 6-bit linear DAC with 2 ranges.
  - Threshold DAC:
    - 6 mV/step (≈0.05 fC).
    - or 24 mV/step (up to ≈12 fC).
  - Calibration DAC (same voltage steps into a 42 fF calibration capacitor):
    - 0.25 fC/step in low range.
    - 1 fC/step in high range (up to about 12 MIPs).
- Functions by adding currents, the total of which are converted to a voltage by a resistor (N-well structure).
- A reference current is derived from the 2V supply and a resistor (the two resistor values cancel to 1st order).
- A test chip with this DAC was received just last week from MOSIS.



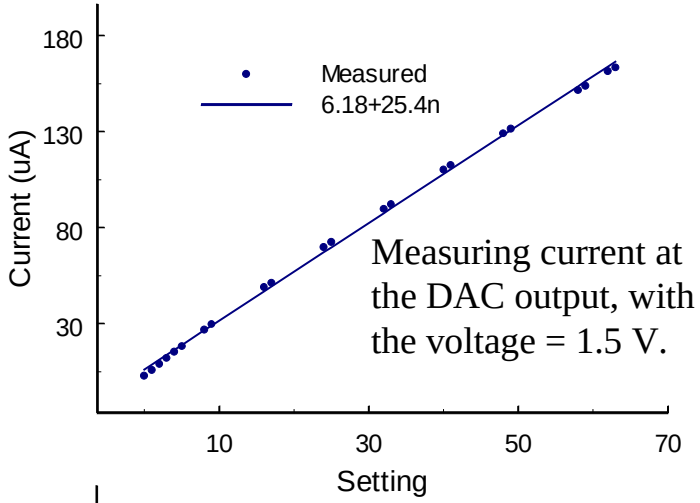
Measurement of the DAC performance in the low range, compared with a Spice simulation of the circuit. The slope is close to expectations despite the error in the resistor values.

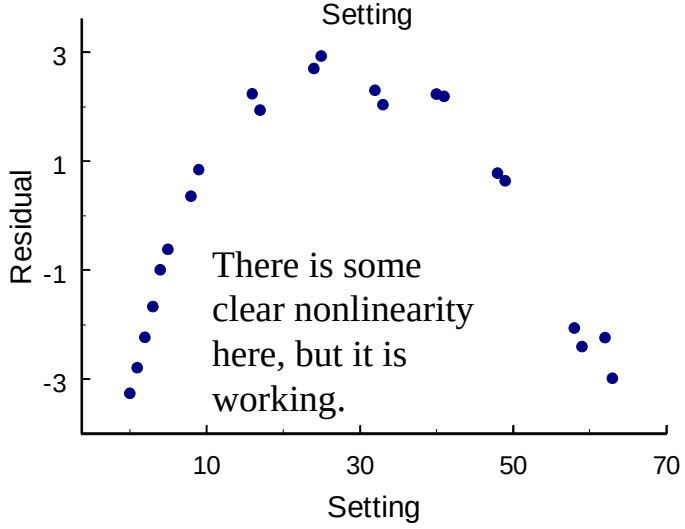
Threshold and Calibration DACs

Even though the DAC low range works perfectly well, the high range does not.



However, the high range is OK if the voltage is held constant and the current is measured, as on the right ⇒

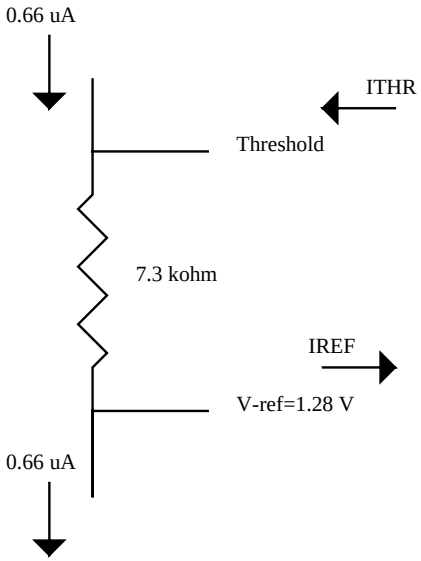


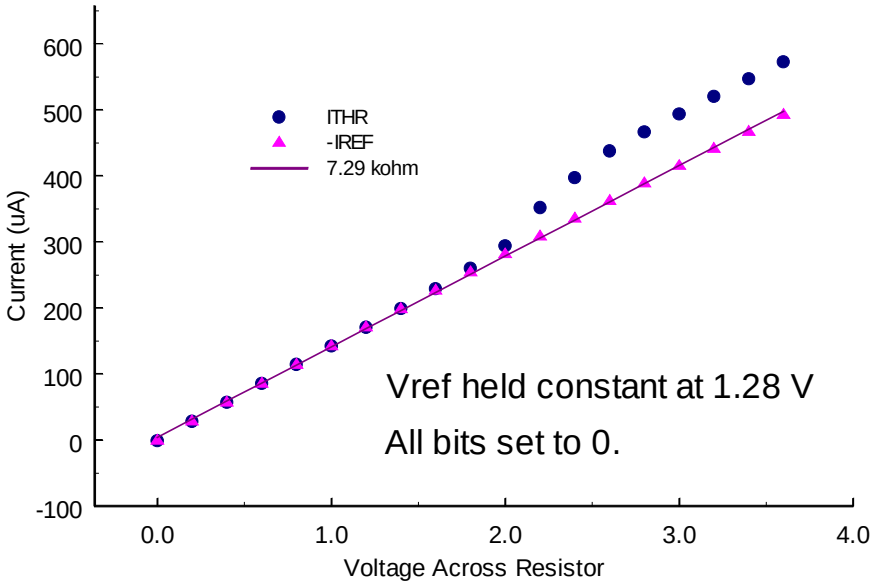


Threshold and Calibration DACs

It appears that current is flowing out of the threshold output node by some means other than through the resistor when the voltage gets above about 2.6 V.

This mystery is being investigated.





With V-ref held constant, V-threshold is scanned from V-ref up to 5 V. Above a certain point there is more current flowing into the threshold node than is flowing out the opposite end of the resistor.

Command Decoder

The front-end chip is controlled by serial command strings delivered to either of 2 redundant command decoders. Either decoder can load the control register at any time, but all other commands are accepted only if the decoder is selected by a bit in the control register.

- Command format:
  - Start bit.
  - 3-bit command code.
  - 5-bit chip address or 1F (for all chips).
  - N-bits of data (load control register).
- Commands:
  - 000: no-op.
  - 001: load control register.
  - 010: read-event.
  - 011: calibration strobe.
  - 100: clear first event from FIFO.
  - 101: reset chip (FIFO + cntrl. reg.).
  - 110: reset FIFO.
  - 111: end-read-event.

Control is by synchronous logic, with an 11-bit state machine. The logic design was done by hand, using a schematic, but the layout was made using DoD CMOSX standard cells and Cadence automatic place-and-route.

The complete design was simulated in Spice, as well as in digital simulators (Viewsim and Verilog).

Drivers and Receivers

- Controller chip to Readout Chips (clock, commands, trigger):
  - Differential current drive, with 1 kΩ termination on the hybrid between the two lines.
  - Maximum load is estimated to be 50 pF.
  - Voltage swing is 0.7 V. Peak current is 12 mA.
  - Rise time is 5.4 ns (compared with 50ns clock period).
  - Receiver power consumption is about 150 μW each, with 5 operating at any given time on each chip.
- Data (chip-to-adjacent-chip):
  - 3V differential CMOS.
  - Simplifies implementation of the 1600-element shift register across 25 chips.
  - Experience with the 32-channel chips suggests that this should not be a problem for these very short distances.
- Fast-OR output (chip-to-adjacent-chip):
  - Small-voltage-swing differential.
  - Local charge storage provides current for the fast edge; the charge is *slowly* replenished from VDD and GND.
  - Therefore, in normal operation, with intermittent triggers, no spikes are introduced into the supplies.
  - Only one set of the redundant drivers and receivers is turned on at a given time, so save power.
- Controller chip to and from adjacent layers and to and from the tower readout electronics:
  - Some form of low-voltage-swing differential transmission will be used.
  - Probably it will be similar to the communication from controller chips to readout chips, but it has not yet been studied and designed.

GTFE64 Simulations

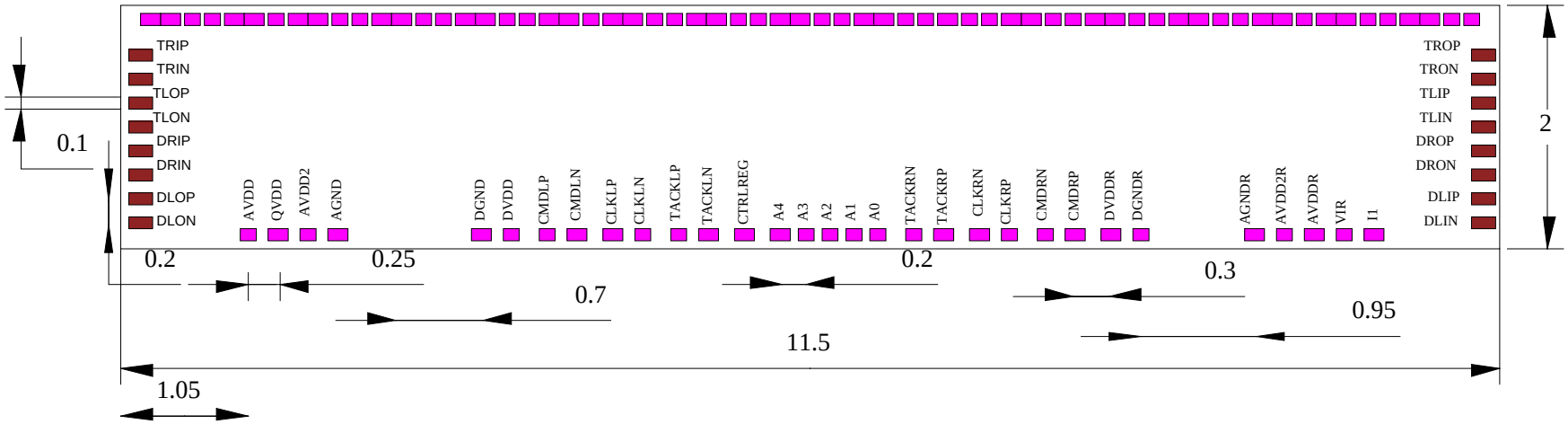
- All of the subcircuits designed by Pavel were simulated thoroughly by him in SPICE (memory, shift registers, drivers, receivers, DACs, *etc*.).
- The complete analog channel has been thoroughly simulated in SPICE (using BSIM models).
- An 8-channel model of the complete output stage (FIFO plus shift registers) was simulated in SPICE (including additional load to account for the missing 56 channels).
- The command decoder was simulated in SPICE as a single unit, as well as in Verilog, using the CMOSX standard-cell Verilog models.
- Logic simulations have been carried out on the complete chip and on a set of three chips connected together:
  - each primitive cell was simulated in SPICE and analog timing diagrams were made.
  - A VHDL model was written for each cell and then executed to produce a digital timing diagram.
  - Delays were introduced into the VHDL models to give a good match between the digital and analog timing diagrams.
  - Dummy VHDL models were made for the analog components for which a digital simulation is meaningless (such as the DACs).
  - The entire schematic was then simulated at 20 MHz and 40 MHz by Viewsim, using Viewsim built-in models for the logic gates and inverters (with nominal 0.5 ns delays).

Layout and Verification

- All layout but that for the command decoder has been drawn manually using the Mentor Graphics IC-Station and MOSIS SCMOS design rules. This includes all I/O pads, with ESD protection. This has all passed LVS and DRC within Mentor Graphics.
- The command decoder layout was done by automatic place-and-route in Cadence using CMOSX design rules.
- The Mentor layout has been transferred into Cadence by way of GDS2, and the two command decoders will be inserted and connected within Cadence. The final LVS and DRC will be done in Cadence before submission, after transferring the schematics from Power-View to Cadence (using EDIF).
- Test-pads have been, or are being, added as follows:
  - Reset pad, to force a reset of the command decoder, if necessary.
  - External calibration pulse input, in case the internal system doesn't work or is insufficient for testing.
  - All analog channel bias points.
  - All preamp and shaper outputs.
  - All receiver CMOS outputs and driver CMOS inputs.
  - DAC outputs.
  - All clock and control outputs from the command decoders.

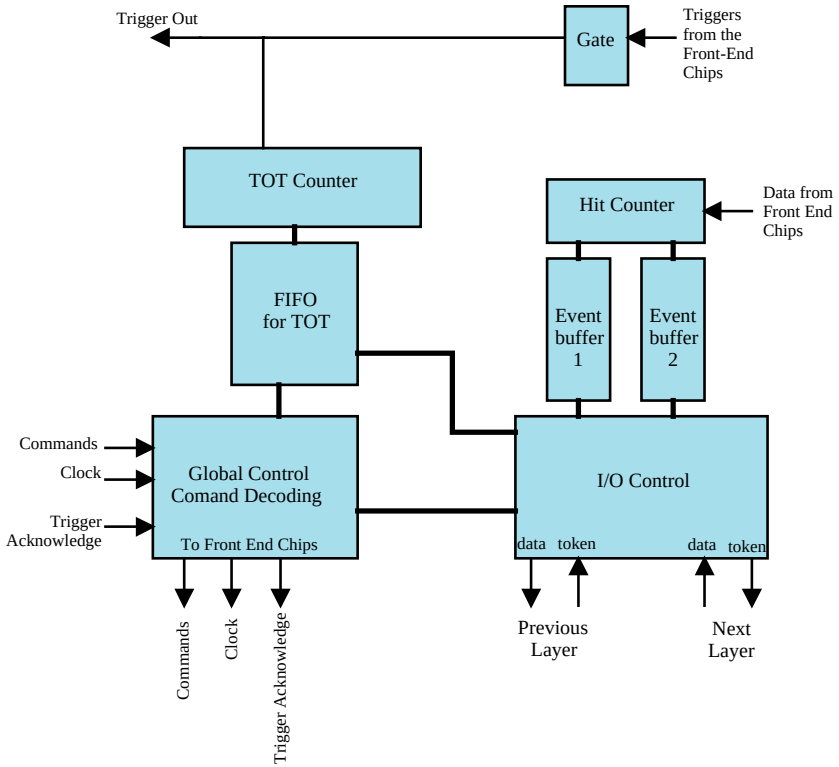
Layout

- The chip is designed to match the 195 micron detector strip pitch.
- Analog power and ground pads are doubled, with one of each at each end of the chip.
- Analog power must pass over the chip-to-chip digital signals. One of the metal layers is used as a shield between them where they cross.
- Analog and digital circuitry are separated by a well structure, but both analog and digital grounds are tied solidly everywhere to the substrate, to avoid latch-up problems.



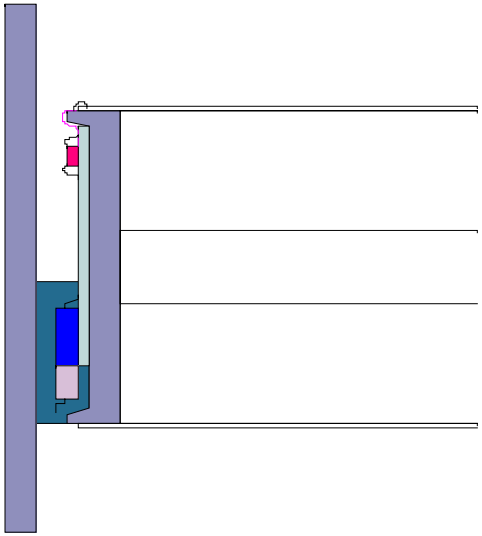
Readout Controller Chip (GTRC)

- Control initialization, calibration, and readout of the front-end readout chips.
- Sparse readout—build list of hit-strip addresses.
- Calculate the time-over-threshold of the prompt trigger output.
- Build events and coordinate the readout with neighboring layers via a serial data line and a token.
- External communication via low-voltage-swing differential lines.
- Currently being designed for the HP 0.8 μm process using the CMOSX standard cells. The logic design is synthesized from Verilog code.



Simplified block diagram of the readout controller chip.

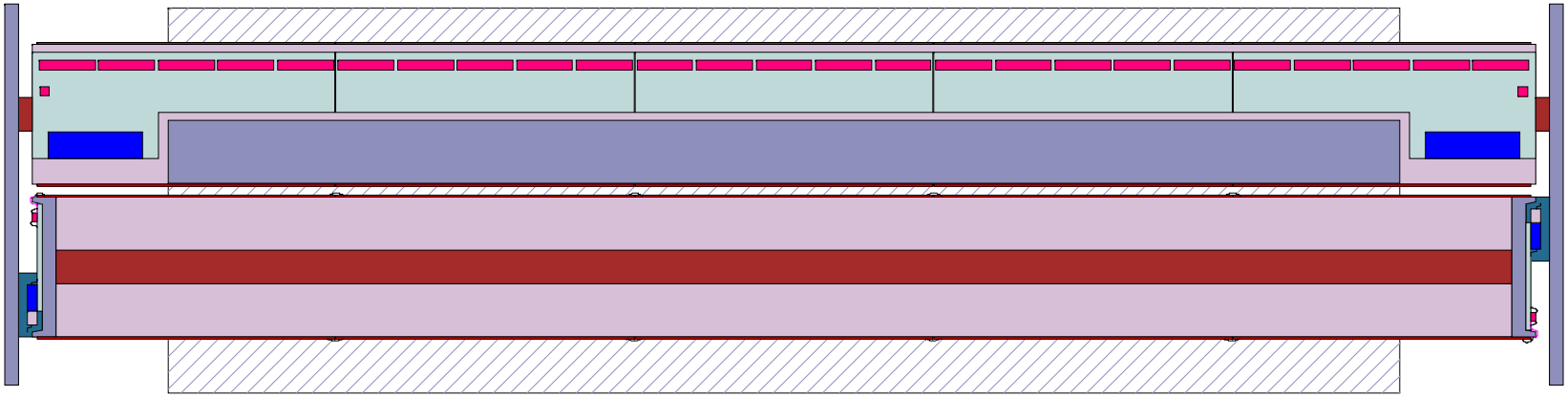
Hybrids



To minimize dead area, the hybrid circuits holding the readout chips and controller chips must be mounted on the sides of the detector trays.

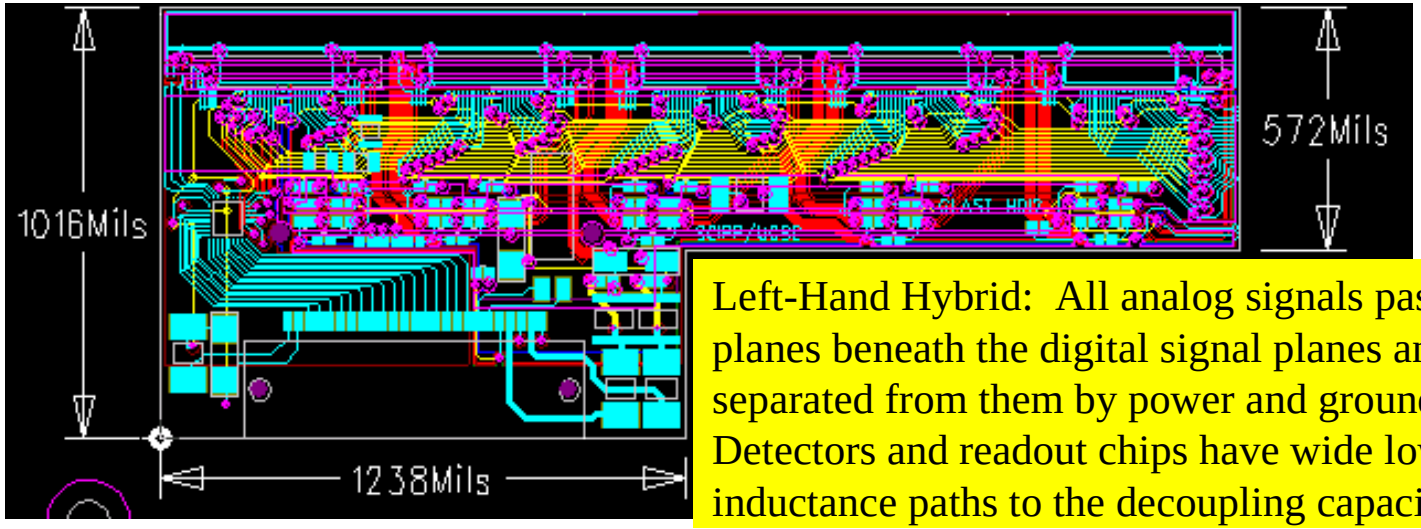
A Kapton flex circuit brings the signals around the corner of the tray.

The hybrid is divided into 5 pieces, each the width of one detector wafer and each holding 5 readout chips. They are connected by wire bonds. The two end pieces each hold a controller chip and connector.



Hybrids

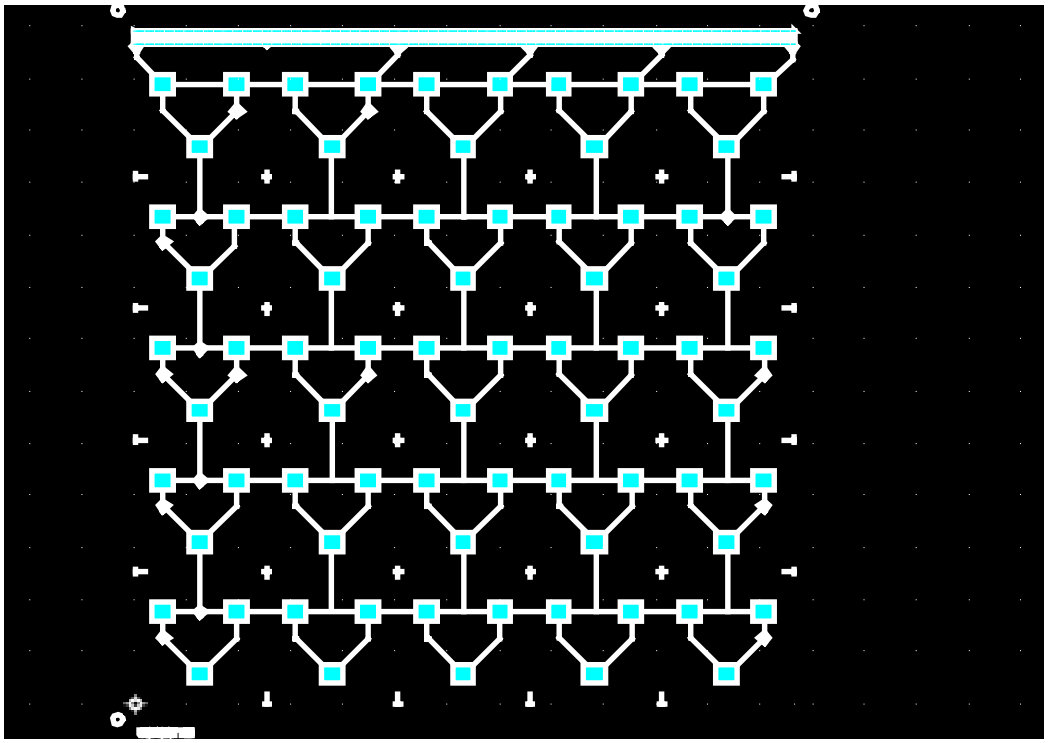
- The hybrid circuits include
  - bypass capacitors for each readout chip and the detector bias,
  - resistors to set the front-end bias current, and termination resistors for the digital signal lines.
  - Power supply filtering and fuses.
  - Temperature monitors.
- Eight layers are used in the layout, including entire planes for power, ground, analog 2V, and detector bias. The central type has already been fabricated.



Left-Hand Hybrid: All analog signals pass along planes beneath the digital signal planes and are separated from them by power and ground planes. Detectors and readout chips have wide low-inductance paths to the decoupling capacitors.

Flex-Circuit Detector Interconnect

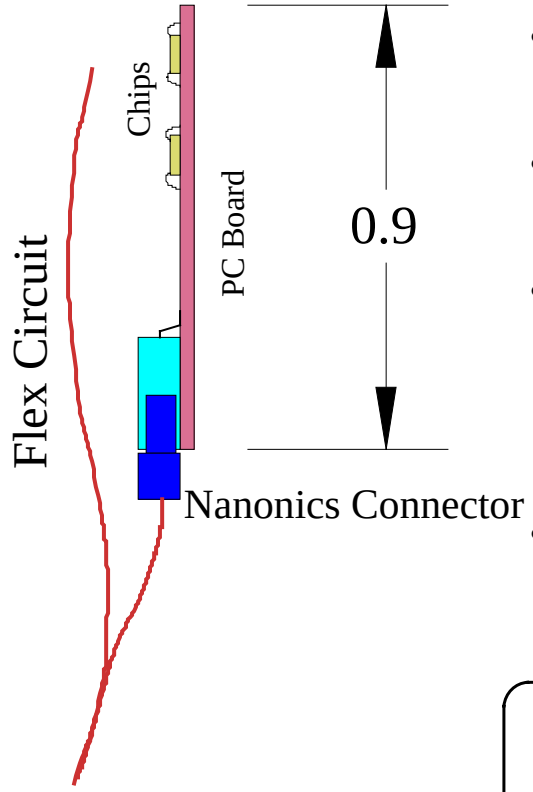
- Top layer of conductors for bias (120 V), ground, and signals.
- Bottom layer is a shield plane to isolate detectors from the trays.
- 3 pads to supply bias to the backs of each of 25 detectors.
- 5 traces to bond to the bias-voltage strips to each of the 5 hybrid circuits.
- 6 traces to bring the ground of the hybrids around the tray corner to the detectors.
- 1600 traces to bring the signals from the detectors around the tray corner to the readout chips.
- Alignment mark at the corner of each detector.



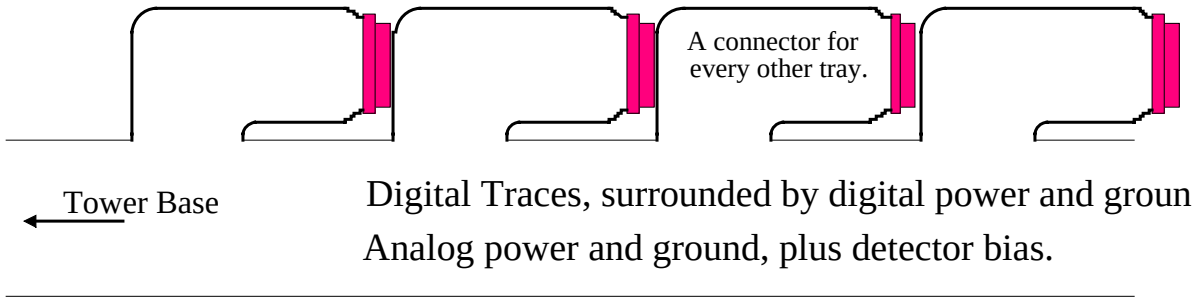
Status:

- Manufacture of 5 prototype pieces is in progress.
- 3-week turn-around.

Cabling and Connectors



- The connectors must lie flat on the hybrid to minimize dead space at the tower edge.
- Nanonics space-qualified 25-pin “Dualobe” 25-mil pitch connectors appear to fit the requirements well.
- The cable must include connections from layer to adjacent layer, as well as from each layer to the tower base. A Kapton circuit provides the best flexibility in design and allows us to build in shielding.
- The design concept shown below will give good access to the connectors and is manufacturable.



Conclusion

- The near-term goal is to have all electronics and detectors necessary to begin assembly of an engineering prototype tower next autumn.
  - Submit GTFE64 chip for 1st prototype production by December 10, 1997. Begin testing in February, 1998.
  - Submit GTRC chip for 1st prototype production in January or February, 1998.
  - Produce at least 10 wafers of GTFE64 chips in July, 1998.
  - Test 1st full readout section in summer 1998.
- Final loose ends of the GTFE64 layout and verification must be tied up *soon.*
- Controller-chip simulations must be carried out together with the readout-chip digital model.
- I/O design of the controller chip must be finalized and layout done.
- Controller chip layout and verification must be done.
- End hybrid design needs to be prototyped, after some possible modifications (more termination resistors?).
- Cables need to be prototyped.
- More interfacing to DAQ at Stanford and mechanical work at SLAC.
- Lots of testing!