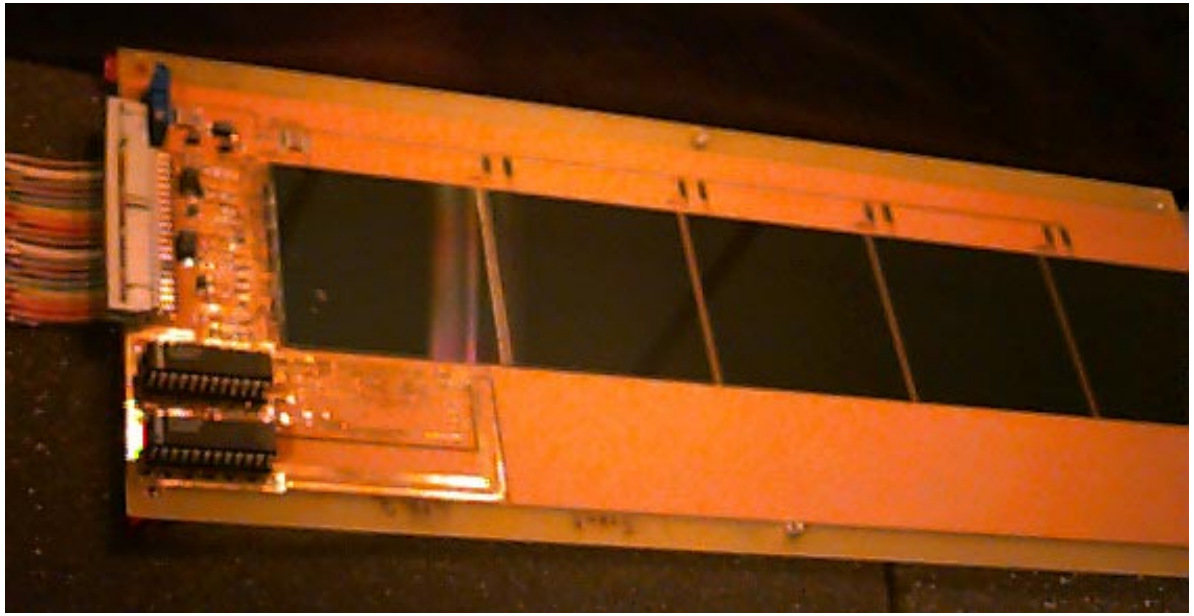
GLAST Silicon Microstrip Tracker Electronics

Robert P. Johnson
Santa Cruz Institute for Particle Physics
University of California at Santa Cruz

- Requirements.
- Status.
- Design Overview
- Readout ASIC development.
- Hybrid circuits.
- Kapton interconnects.
- Cables.
- Planning



November 6, 1997

Electronics Requirements

- Power less than 300 μW/channel, including amplifiers and digital readout.
- Low noise occupancy (<0.05%) and good threshold uniformity.
- Microsecond peaking time for the amplifiers.
- Self triggering.
- Radiation hard to 10 kRad with latch-up immunity.
- <1% dead-time at a 1 kHz trigger rate.
- Sparse readout and data formatting close to the front end.
- Sufficient redundancy to be immune to single-point failures.

Status of UCSC Readout Electronics

- 16-channel amplifier-discriminator chip designed, fabricated, and tested. Meets basic noise and power requirements.
- Improved 32-channel version fabricated for the beam test.
- Fabricated complete tracker and readout for the highly successful SLAC beam test. Included 12 planes, each with 6 32-channel chips.
- Design of the 64-channel readout ASIC chip with complete digital functionality is nearly finished and will be submitted in December.
- Design of a readout controller ASIC is in progress and well advanced.
- Three different hybrid circuits for mounting the readout and controller chips have been designed and one has been fabricated.
- Kapton interconnect for mounting the detectors has been designed and prototypes are currently being fabricated.
- Preliminary design has been made of the cabling.

Facilities and Manpower at UCSC

Facilities & Equipment

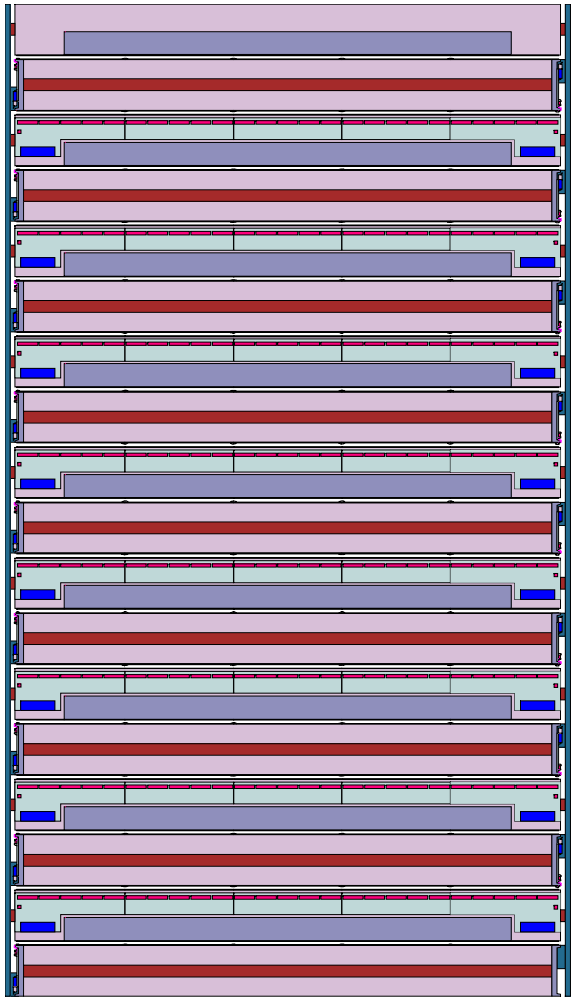
- About 2000 square feet of new space recently allocated to ***this project***.
- $200k new funds from NSF + UCSC for automated wire bonder and probe station.
- 2 manual wire bonders and 3 probe stations with associated microscopes.
- Numerous pieces of electronics test equipment: semiconductor parameter analyzers, logic analyzers, spectrum analyzers, precision LCR meters, pulsers, digital scopes, HV source-measure units, VME DAQ systems, *etc.*
- Radioactive sources, including a large Co-60 source for radiation damage studies.

People Working on GLAST at UCSC at this time.

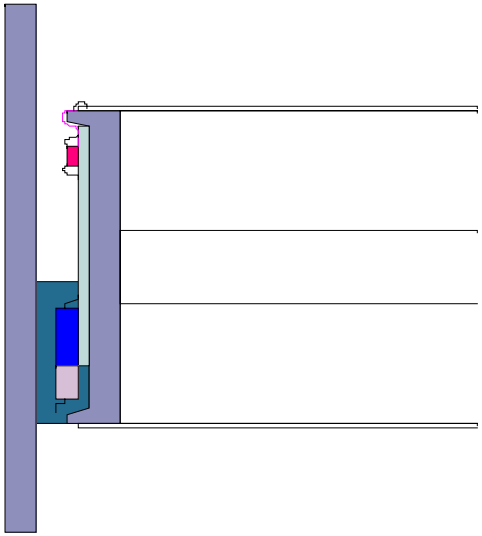
- 3 senior physicists (Atwood, Johnson, & Sadrozinski)
- 3 postdoctoral physicists
- 2 graduate students
- 2 electronics engineers
- 1 PC board designer
- 2 electronics technicians
- 1 machinist

Tracker Design Overview

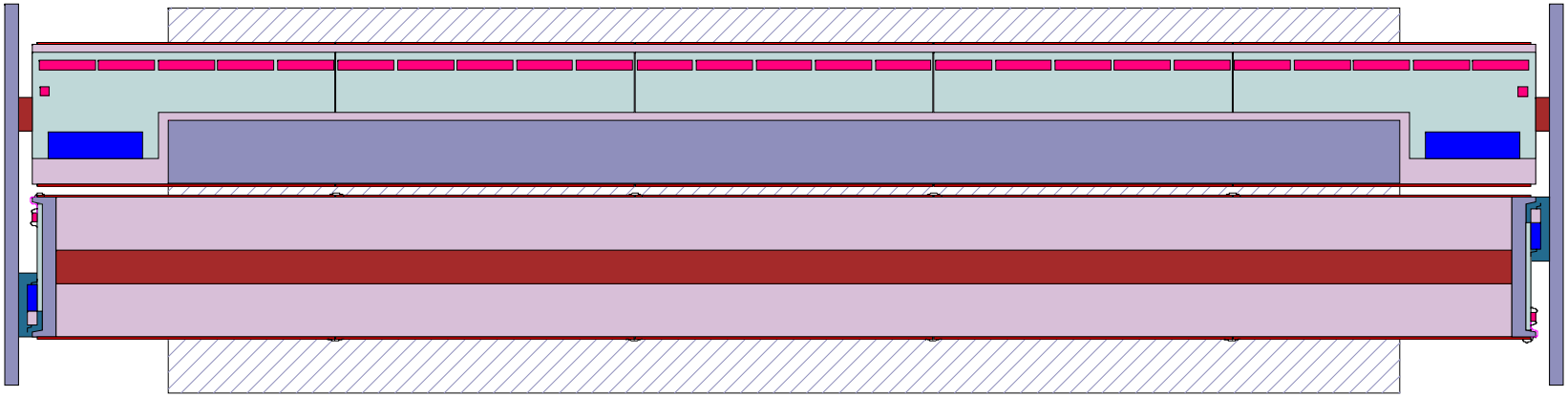
- 17 thick, stiff “trays.”
- Detectors on top and bottom.
- Radiator foils beneath detectors on the bottoms of top 14 trays.
- Electronics on the sides.
- 90° rotation from one tray to the next for stereo view.
- Minimal gap between trays, to keep detectors close to radiator foils.
- Be walls for support and heat conduction.



Tracker Design Overview



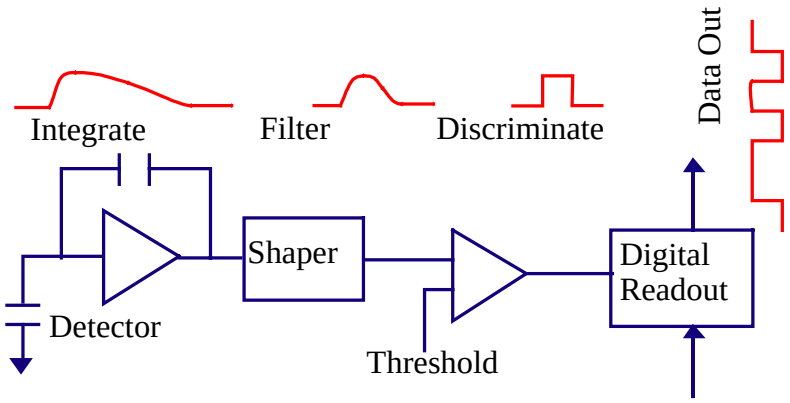
- Walls leave the corners open for access to cables and connectors.
- Kapton flex circuits bring the signals around the corner from the detectors to the readout chips.



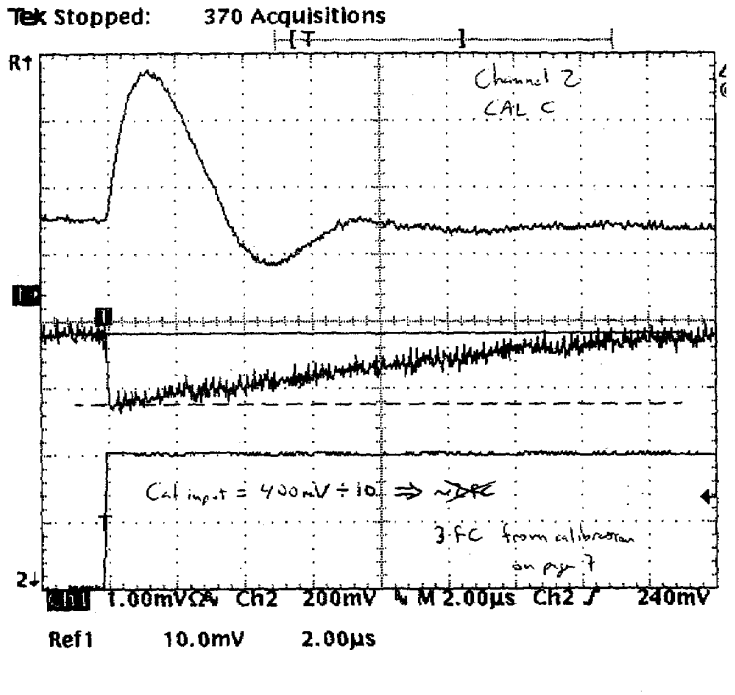
Readout ASIC Development

16-Channel Prototype Chip

- 16 sets of preamp, shaper, and comparator.
- Simple mask and shift register for readout.
- Prompt trigger output (OR of all channels)

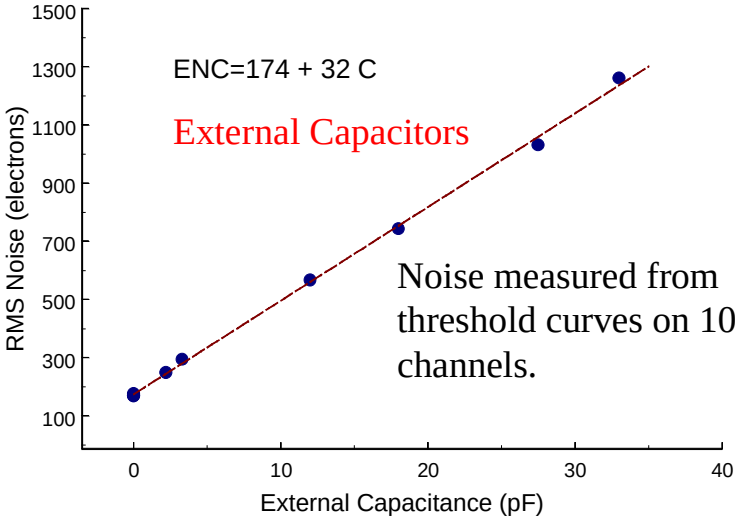


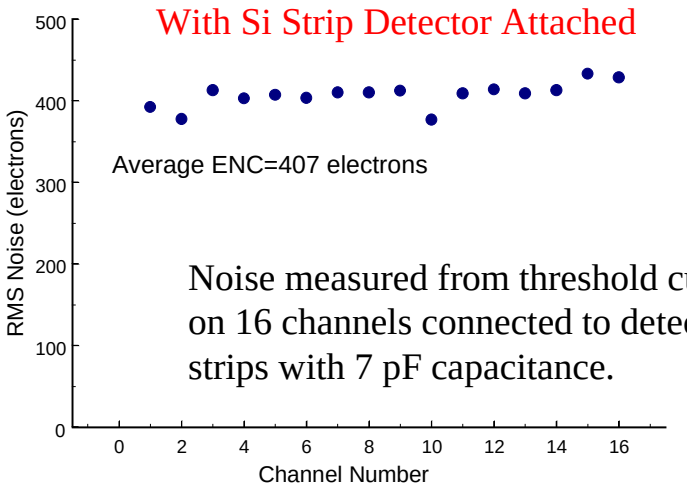
Scope traces of the shaper and preamp outputs (from probe).

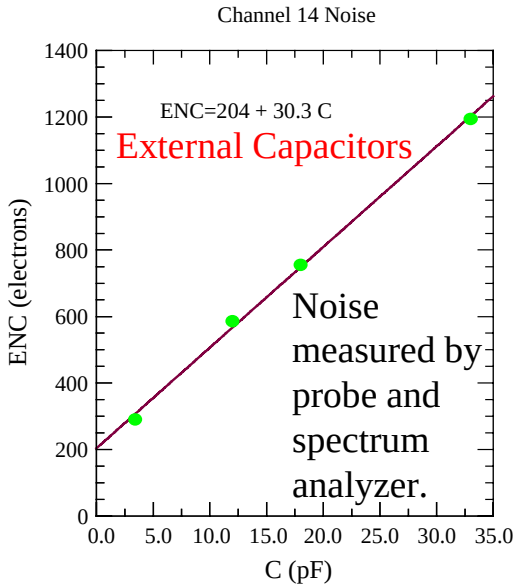


Measured Amplifier Performance

- Gain (shaper output): ≈125 mV/fC
- Peaking time: ≈1.3 μ s
- Power consumption, including bias circuitry: 150 μW/channel
- Noise: ENC=204 + 30.3×C electrons, with C in pF, measured by several methods, as shown here.

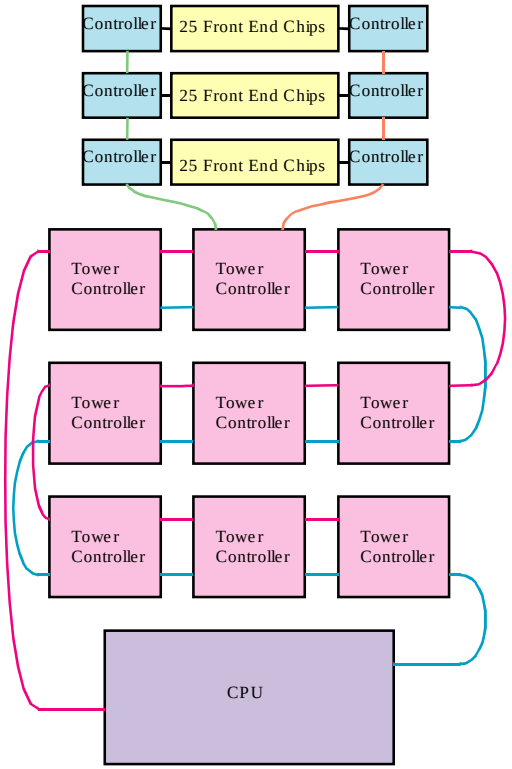


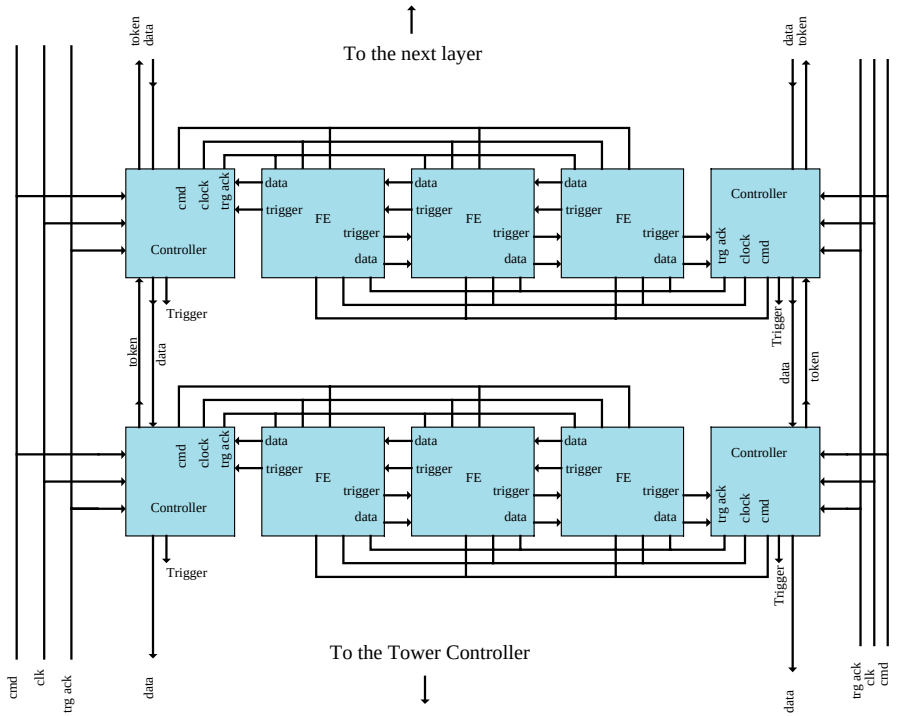




Readout System Design

- Serial data transmission.
- Redundant data paths.





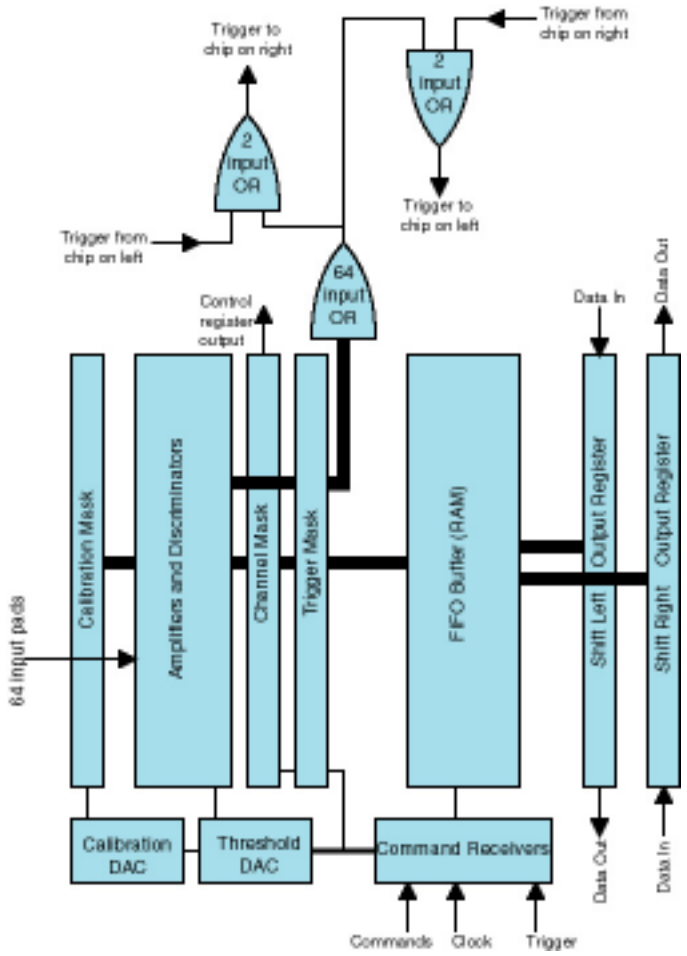
- 25-readout-chip daisy chain per layer
- 2 redundant readout controller chips per layer.

64-Channel Readout Chip

- Calibration mask to select any set of channels to pulse.
- 7-bit DACs for calibration and threshold levels.
- Separate data and trigger masks.
- 8-deep FIFO event buffer.
- Redundant command decoders and output registers—each chip can be controlled by either controller.

Status:

- Schematic-level design complete.
- Mask design nearly complete.
- Simulation and other final verification steps in progress.

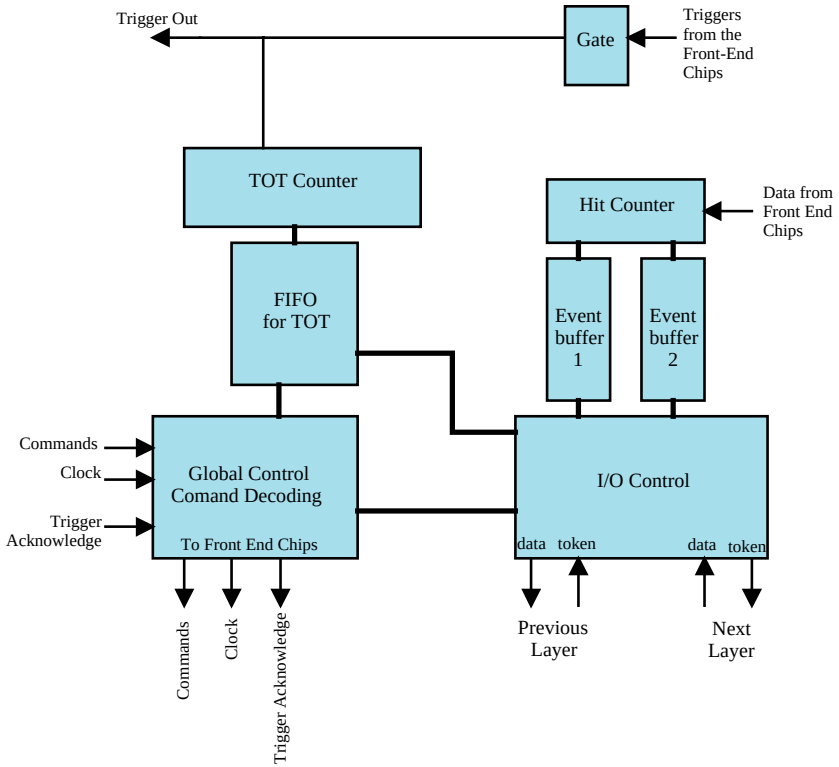


Readout Controller Chip

- Control initialization, calibration, and readout of the front-end readout chips.
- Sparse readout—build list of hit-strip addresses.
- Calculate the time-over-threshold of the prompt trigger output.
- Build events and coordinate the readout with neighboring layers via a serial data line and a token.

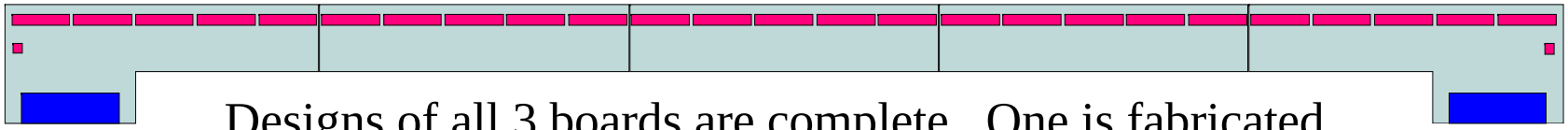
Status:

- Detailed state diagrams and logic description are nearly complete.
- Gate-level design will be done by automated synthesis.
- Layout will be done mostly using standard cells and automatic place and route.

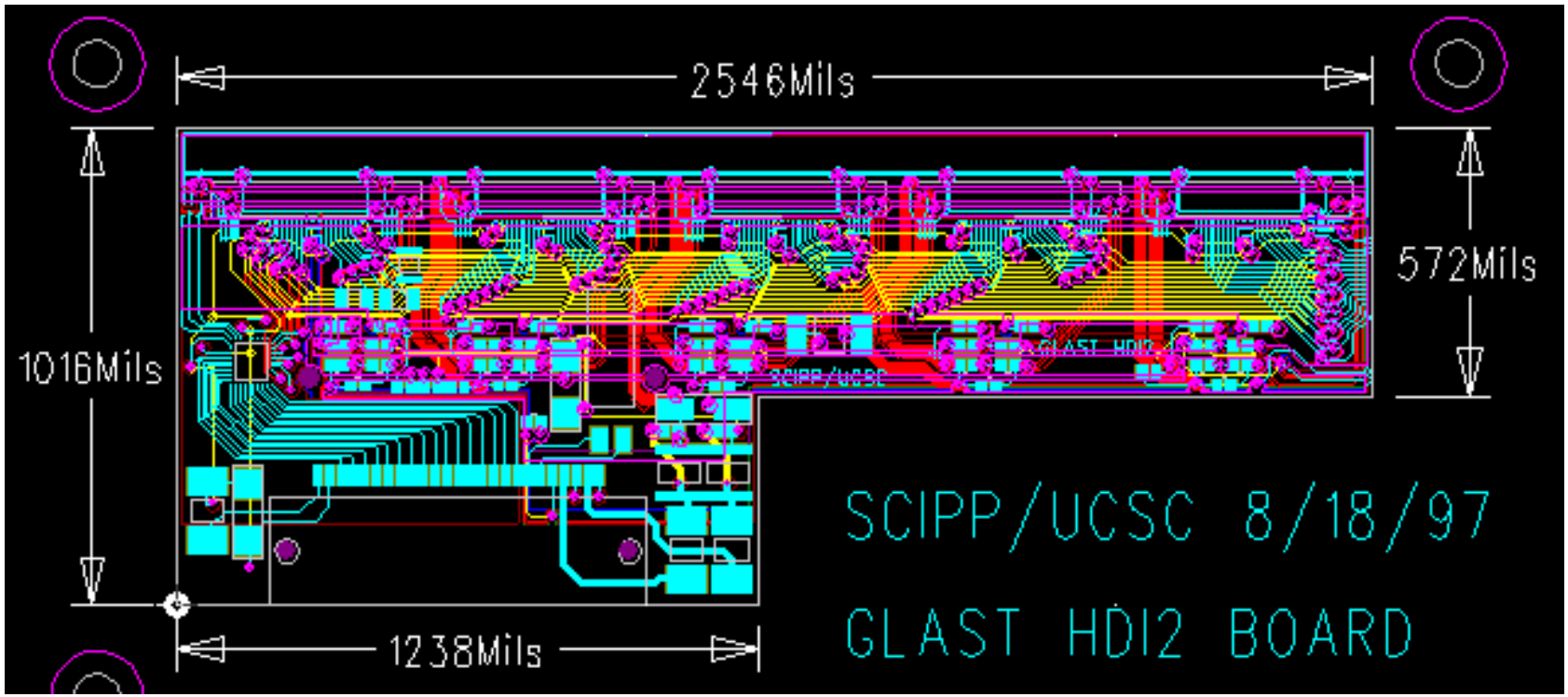


Hybrid Circuits

Three 8-Layer Printed Circuit Boards

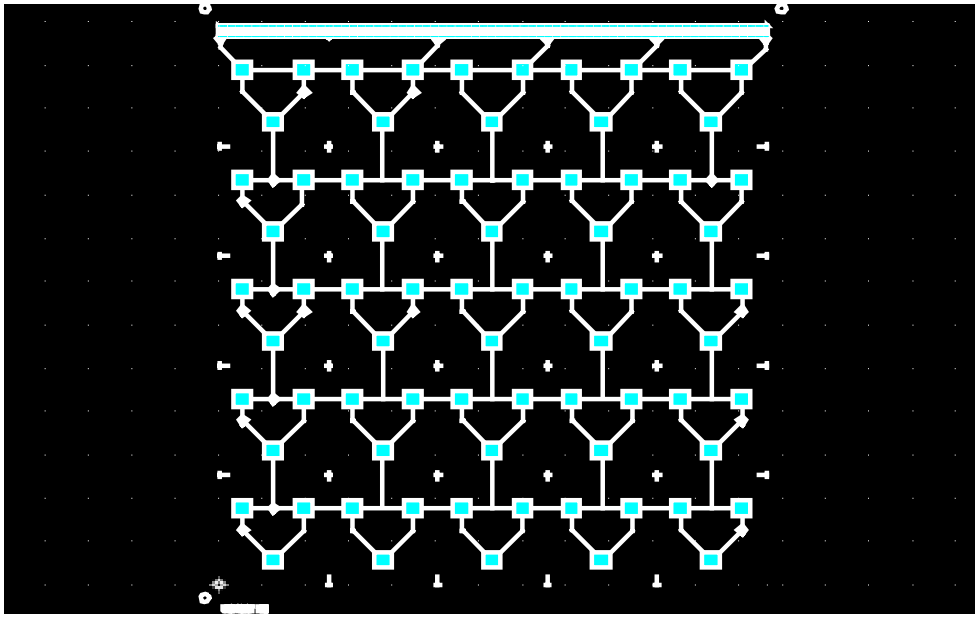


Designs of all 3 boards are complete. One is fabricated.



Kapton Flex Interconnect

- Top layer of conductors for bias (120 V), ground, and signals.
- Bottom layer is a shield plane to isolate detectors from the trays.
- 3 pads to supply bias to the backs of each of 25 detectors.
- 5 traces to bond to the bias-voltage strips to each of the 5 hybrid circuits.
- 6 traces to bring the ground of the hybrids around the tray corner to the detectors.
- 1600 traces to bring the signals from the detectors around the tray corner to the readout chips.
- Alignment mark at the corner of each detector.

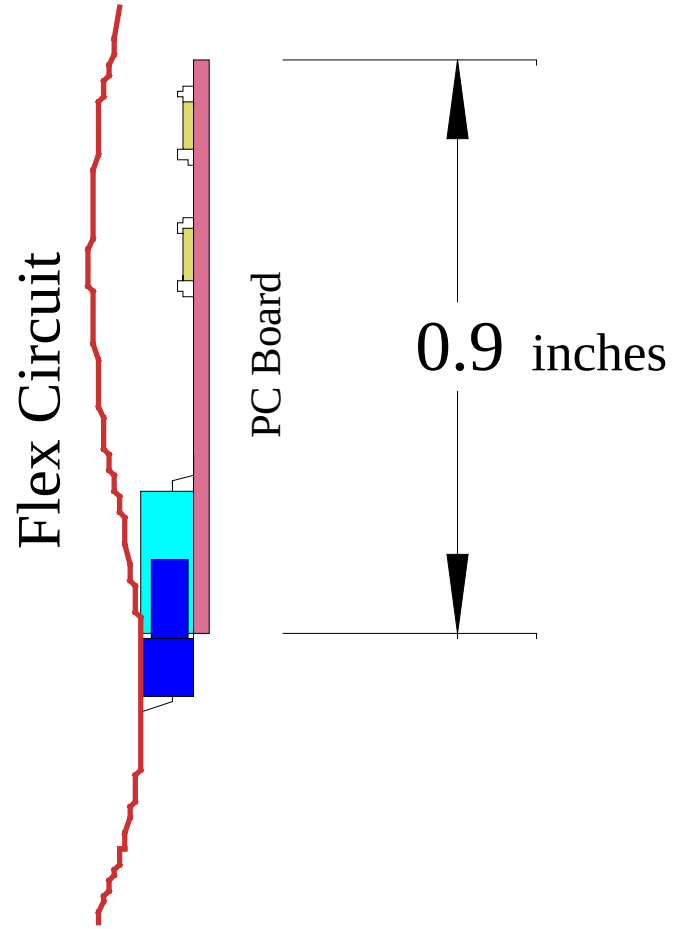


Status:

- Manufacture of 5 prototype pieces is in progress.
- 3-week turn-around.

Connectors and Cabling

- The major difficulty is the small clearance required at the tray edges.
- The mounting scheme shown here minimizes the dead space between the detectors and the tower wall but complicates access to the connectors.
- A vendor of suitable space-qualified miniature connectors has been identified and samples obtained.
- We have made a design of a Kapton flex-circuit cable, but we are reevaluating how it will attach to the connectors.



Electronics Development in 1998⇒2000

- Prototype tower critical path: ASIC development.
  - December 1997: submit 64-channel readout chip prototype.
  - January 1998: submit readout-controller chip prototype.
  - February 1998: begin prototype testing.
  - July 1998: begin production of the ASICs; complete in September.
- Kapton interconnect: test assembly methods using prototypes. Iterate the design and fabricate >32 pieces for the prototype tower.
- Flex cables and connectors: fabricate prototypes and test them during Winter/Spring 1998. Iterations may be needed even beyond the first prototype tower.
- Amplifier improvements: study beam test results and make further measurements in our lab. This will lead to important incremental improvements in the analog performance.
- Process change: the HP 0.8μm process that we are using will be discontinued in early 1999. We will have to investigate other processes to find one suitable for the analog electronics of the readout chip. Then the design will have to be redone.
- Space qualification: the ASICs will have to be tested for radiation damage and latch-up resistance. All parts will have to undergo environmental testing.