GLAST Silicon-Strip Tracker Development Work at U.C. Santa Cruz

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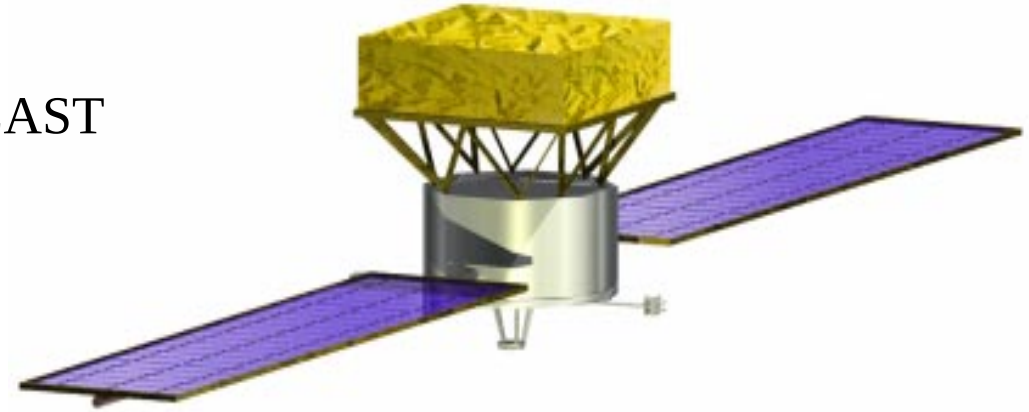
- UCSC Responsibilities in GLAST
- UCSC GLAST Personnel
- Schedule for this Afternoon
- GLAST Tracker Electronics



UCSC Responsibilities in GLAST

- Silicon-Strip Tracker subsystem manager: R. Johnson
- Silicon-strip detector specifications, acquisition, testing: H. Sadrozinski
- Tracker readout electronics:
  - System design.
  - ASIC design, prototyping, and testing.
  - Printed circuit board design and prototyping.
  - Kapton flex circuit and flex cable design and prototyping.
  - Production and testing of components for the prototype tower.
  - Electronics assembly, testing, and QC.
  - Interfacing with the DAQ system being developed at Stanford.
- Prototype tower assembly
  - Detector and IC wire bonding.
  - Potting of wire bonds on the detector ladders.
  - Integration of the electronics onto the trays.
- Software development for simulation and track reconstruction

GLAST Personnel at UCSC

- Ph.D. Physicists:
  - W. Atwood (SLAC)
  - D. Dorfan
  - R. Johnson
  - H. Sadrozinski
  - J.A. Hernando
  - M. Hirayama
  - W. Kröger
- Electronics Engineering
  - V. Chen; ASIC design
  - N. Spencer; analog/system design
  - S. Kashiguine; PC board & flex-circuit design, testing
- Electronics Assembly
  - G. Paliaga
  - W. Rowe
- Machining and Assembly
  - A. Webster
- Graduate Student
  - Yuko Nakazawa
- Undergraduate Students
  - Jeff Clark
  - Dennis Melton
  - Michael Sears
  - Sean Stromberg
  - (numerous others in past)
- REU program & summer interns

Schedule for this Afternoon

- 2:30 Introduction — R. Johnson
- 2:45 GLAST Instrument Mechanical Engineering — W. Miller of Hytec, Inc.
- 3:30 Silicon-Strip Detectors — H. Sadrozinski
- 3:50 Break
- 4:00 Tracker Readout Electronics — R. Johnson
- 4:30 GLAST Software Efforts at UCSC — W. Atwood
- 4:45 Laboratory Tour
- 5:30 Leave for dinner
- 6:00 Dinner at Casa Blanca, near the wharf, corner of Beach Street and Main Street.

Silicon-Strip Readout Electronics

Silicon solid state detectors date back to the beginning of the transistor age. What has made silicon microstrip detectors possible since the late 1980's is the availability of custom VLSI circuits for readout of the devices.

The result has been detector systems with revolutionary capabilities:

- Ultra-high-precision tracking
- Reliability, low maintenance
- Robust and radiation hard

Recent UCSC experience with silicon-strip readout systems:

- Zeus LPS, bipolar amplifier chip, CMOS digital pipeline.
- SDC/ATLAS, rad-hard bipolar amplifier chip and CMOS digital back-end.
- SLAC B-Factory, rad-hard CMOS amplifier, digitizer, back-end on single chip.

The GLAST system inherits a great deal from the B-Factory experience, despite very different requirements.

Readout Electronics Requirements

Requirements

- Low power: ~200 μW/channel.
- Low noise: occupancy $<10^{-4}$, or ENC<2000 electrons. Especially critical for implementation of self triggering.
- High efficiency in fiducial volume.
- Minimal dead space around tray edges.
- Fault tolerance. Redundant readout and control paths.
- High readout rate (order 1 kHz), with buffering for low dead time.
- Minimize cabling in tower.
- Minimize mass of electronics and cables (multiple scattering between towers).

Important issues considered in the current system design.

- Single-sided versus double-sided detectors.
- Detector thickness, 300μm vs 400 μm.
- Detector strip pitch & width (charge collection, capacitance, *etc.*).
- Digitized pulse-height versus binary readout.
- Amplifier time constant—amp noise versus triggering requirements and (measured) radiation damage.
- Tray size (study of 40-cm tray concept recently written up).
- Electronics location: on faces of trays or on the sides?

Noise versus Power

The noise and power goals appear inherently contradictory, but we have ***met the requirements*** by ***keeping the readout simple:***

- Single-sided detectors.
  - lower capacitance (lower noise).
  - no large voltage-level translation needed for the signals.
  - (Also more robust and less expensive)
- Binary readout.
  - No digitizers.
  - Minimal amount of data to move.
  - Fits well the physics requirements.

Other factors:

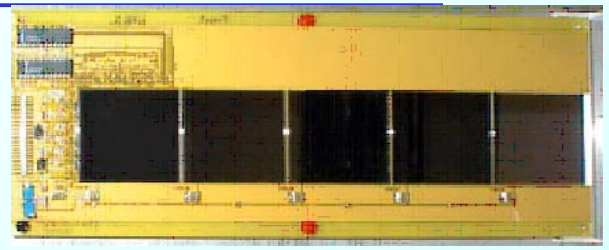
- Amplifier time constant.
- Optimizing tray size (strip length)
- Digital voltage (3V).
- Low-Voltage-Differential Signaling for communication.
- Filtering, decoupling, and shielding on the PC boards and flex circuits.
- Turning off clock when not needed.

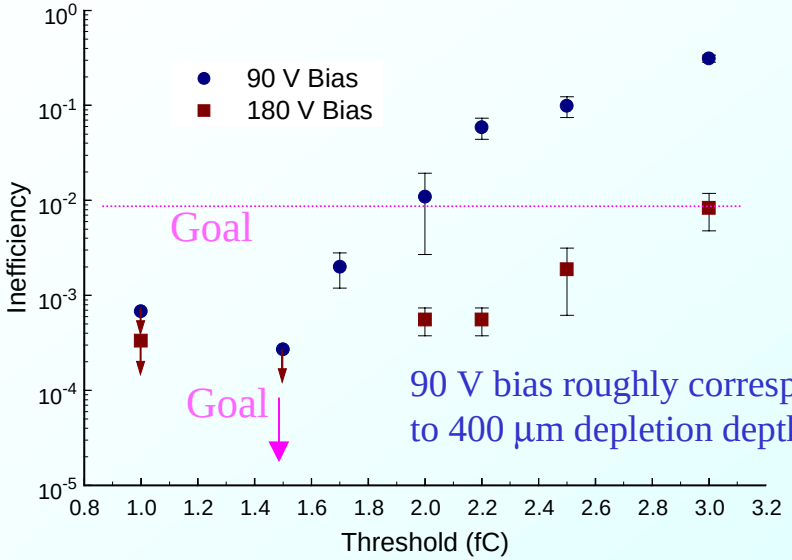
Results: ***verify with actual hardware***

- Early amplifier prototypes (1996).
- 1997 SLAC beam test.
- Completed prototype readout section, October 1998.

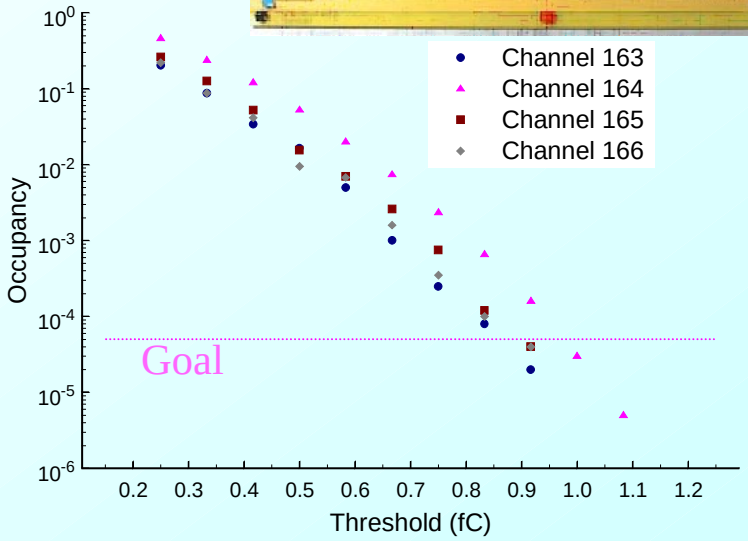
Noise vs. Power Verification

October 1997: Tracker electronics performance measured with a 30cm long detector ladder in beam test.





Inefficiency for detection of minimum ionizing electrons at normal incidence in a single detector plane.



Noise occupancy, in a 1μs window, versus threshold for four different channels connected to 30 cm long detector strips.

October 1998: complete readout section, with full digital functionality and 1600 amplifiers, demonstrates ~210μW/ch with pessimistic assumptions: 12.5 kHz trigger rate, 400 bits/trigger, and end-of-life detectors.

Readout Rate/Cabling/Redundancy

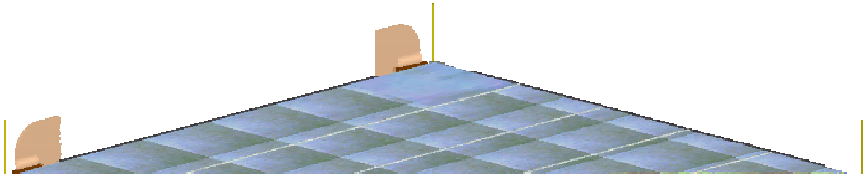
Minimize trigger complexity and maximize versatility by providing rapid readout of the tracker.

Move data and control signals in serial lines, with tower layers daisy chained, to minimize cabling.

Two redundant control and data paths for each tower side.

- 8-deep FIFO buffering in the front-end chips.
- Two-stage readout:
  - FE chips into controller chips.
  - Controller chips into TE˝1 1chi25 front-end chips

Minimizing Dead Space



- Dead space around the tower edges was greatly reduced by placing the electronics on the tray sides.
- However, this does complicate the interconnects.
- Dead space within trays is being minimized by going to larger detector wafers.

Reliability; Quality Control

To assemble complete trays (3200 channels) with <1% loss of functionality requires extensive testing at each step.

Component testing before tray assembly:

- IC chip probing on wafers.
- Testing of PC boards.
- Testing & burn-in of completed readout sections.
- Detector testing at manufacture and at UCSC.
- Testing of detector ladders after wire bonding and potting.

These steps are already in place at the prototype level at UCSC.

To maintain high quality components for the prototype tower, we must pay close attention to handling.

- Clean rooms being installed for GLAST assembly at UCSC and SLAC.
- Safe storage containers are being constructed for detectors and electronics.
- Wire bonds will be protected by epoxy as much as possible.
- A relational data base is being set up for tracking parts.
- Handling procedures for the detectors and chips are being worked out.

Toward a Flight Instrument

- Improvements in electronics, for lower noise, lower power, enhanced reliability.
  - Moving to new process with smaller feature size. (SOI?)
  - Second discriminator for trigger.
  - Fail-safe memory for configuration registers.
  - Further tests of radiation damage, plus latch-up immunity.
  - Study other ideas: ULP-CMOS; turning on/off communication lines; *etc.*
- Electronics system issues.
  - Power supply system.
  - Interference.

- Improvements in detectors.
  - Larger wafers.
  - Investigate other interconnect schemes (GFSC).
- Assembly procedures
  - Build upon prototype tower experience.
  - Increased automation.
  - Documentation.
- Space qualification of custom parts, materials, adhesives, *etc.*
- Tray materials
  - Carbon-composite structures
  - Minimize tower mass.
- testing

Schedule Milestones

- Nov. ‘98: First fully functional GLAST tracker tray.
- April ‘99: Electronics components fabrication completed for the prototype tower (quotation is in hand for ASICs).
- April ‘99: Final tower geometry decided—re-optimize amplifier design.
- Dec. ‘99: Prototype tower completed and tested.
- Dec. ‘99: New CMOS processes evaluated.
- Mar. ‘00: Prototype chips available from the selected new process , with enhancements already discussed.
- Oct. ‘00: Complete tests on detector trays of the final readout electronics design on the new process.
- Dec. ‘00: Complete space qualification studies of the electronics components.
- Jun. ‘01: Complete fabrication of the ASICs, hybrids, and flex circuits for the GLAST instrument.