GLAST Silicon Microstrip Tracker Status

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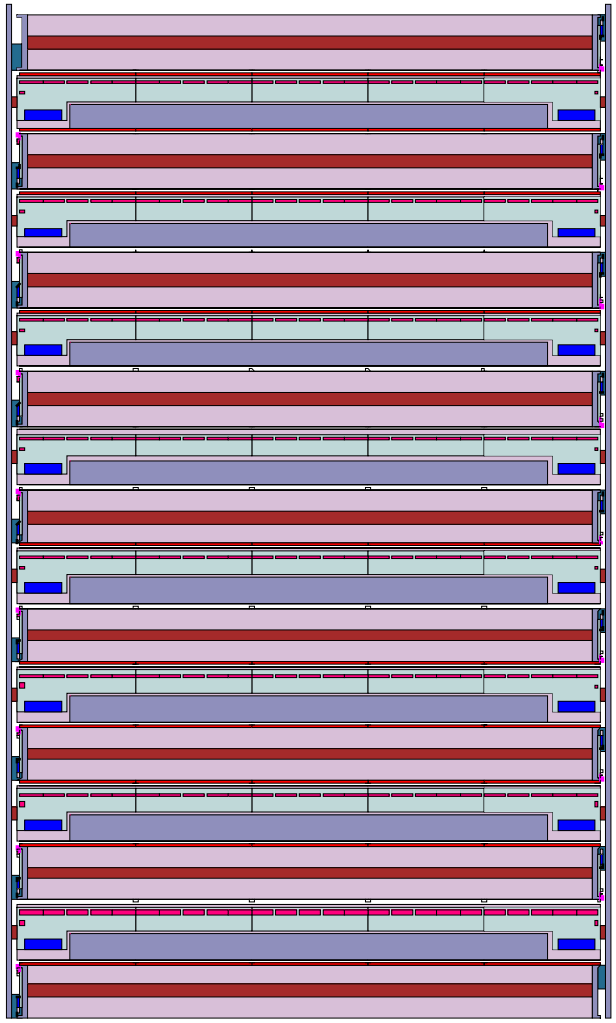
- Mechanical Design
- Detector Procurement
- Work list for the Prototype Tracker Construction.
- ASIC Development
- Hybrids
- Kapton Interconnects and Cabling
- Assembly and Testing
- Schedule

Tracker Mechanical Design

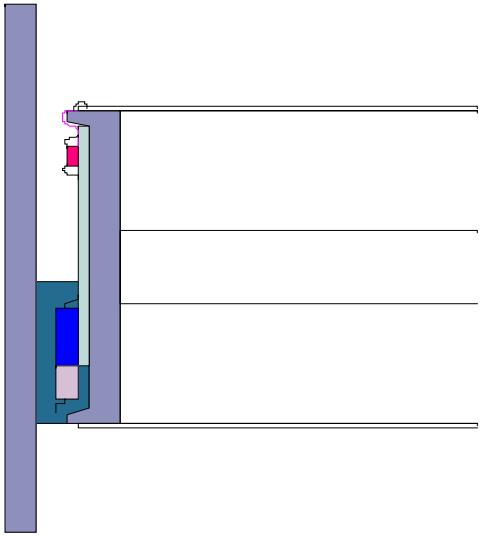
- Design work is being carried out by several groups. Refer to the talks of this afternoon.
  - Hytec Inc. (William Miller *et al.*): Structural and thermal modeling. Emphasis on optimization of the design with respect to the amount of material and dead space. This work began with the tracker but is now being integrated with the calorimeter and ACS.
  - SLAC: Working on a specific baseline design, with current emphasis on preparing to build the prototype tower.
  - Lockheed-Martin: thermal modeling.
- GSFC also will collaborate on the overall mechanical design. NRL is working on the calorimeter design, which is a big factor in the overall tower design (most of the weight!).

Prototype Tower Mechanical Layout

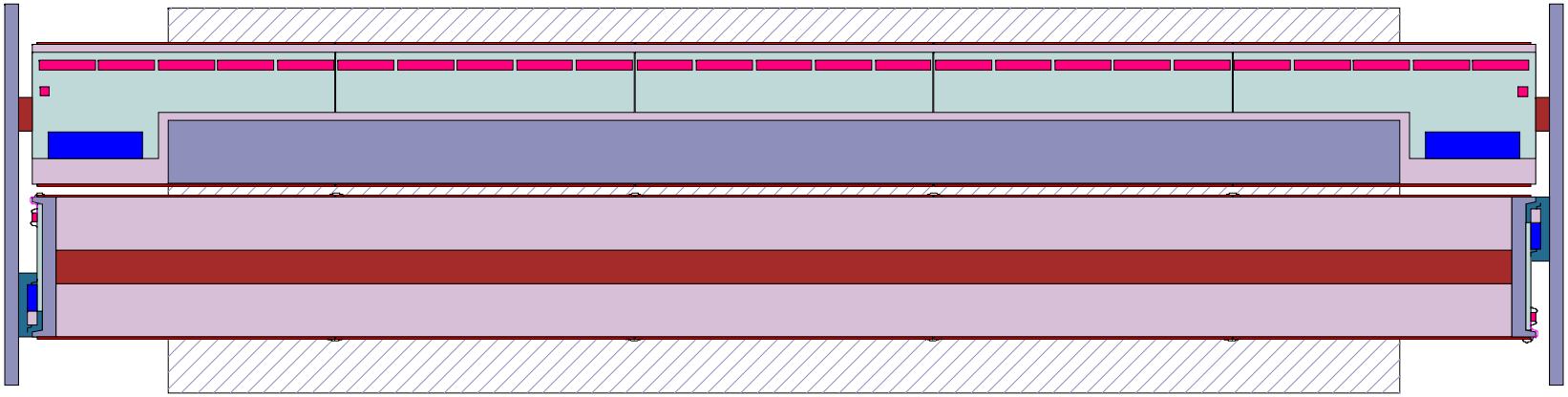
- 17 thick, stiff “trays.” 16 x,y planes
- Detectors on top and bottom.
- Radiator foils beneath detectors on the bottoms of top 13 trays.
- Electronics on all four of the sides.
- 90° rotation from one tray to the next for stereo view. All trays are identical.
- Minimal gap between trays, to keep detectors close to radiator foils.
- Be walls for support and heat conduction.



Prototype Tower Mechanical Layout

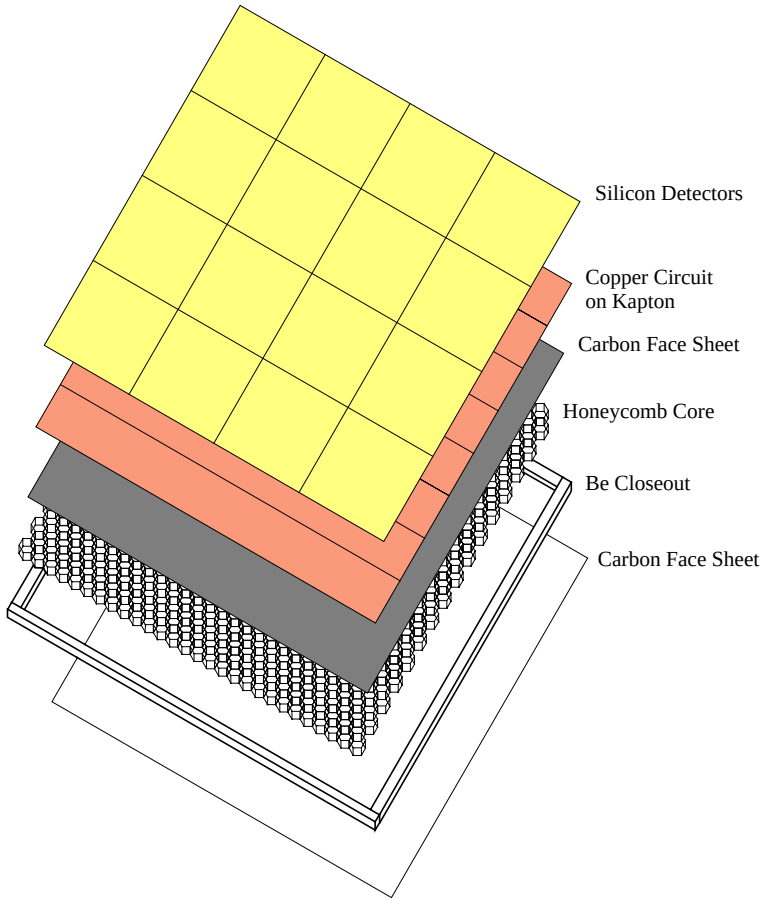


- Walls leave the corners open for access to cables and connectors.
- Kapton flex circuits bring the signals around the corner from the detectors to the readout chips.



Prototype Tower Mechanical Layout

- Detector trays are a light composite structure with a beryllium closeout.
- The core may be a hex cell or a more uniform foam
- A Kapton flex circuit provides the bias voltages to the detectors as well as bringing the signals around the corner to the readout chips.



Detector Procurement

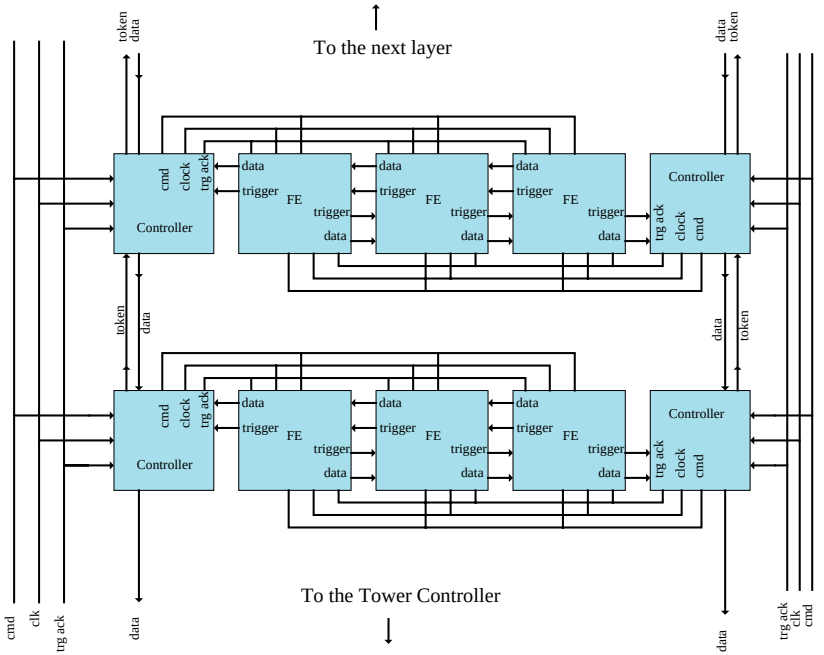
- The specifications for the silicon detector wafers are complete.
  - Tokyo, Hiroshima, SLAC, and UCSC collaborated on making the specifications.
  - The specifications were reviewed by experts outside of the GLAST collaboration, as well as within.
- Probably only Hamamatsu Photonics will contribute to the production (problems with Seiko SSD division). 150 ordered so far, to be ready by December. (400 are needed for a complete 16-plane tower.)
- Highlights of the specifications:
  - 195 micron pitch
  - 50 micron wide strips
  - 6.4 cm by 6.4 cm square
  - 385 microns thick
  - ~50 MΩ polysilicon bias resistors

Work for the Prototype Tracker

- 1997 beam test (see later talk)
- Further studies & optimization of the amplifier design (UCSC).
- Characterization and testing of the detectors (UCSC *et al.*).
- Readout chip design and testing (UCSC).
- Controller chip design and testing (UCSC).
- Hybrid circuit design (UCSC).
- Kapton detector interconnect design (UCSC).
- Tower cabling design (UCSC).
- Hybrid assembly and testing (UCSC).
- Tray construction (SLAC).
- Mounting of Kapton interconnect, detectors, and hybrids (SLAC).
- Wire bonding (UCSC).
- Tray testing and calibration (UCSC).
- Assembly of the trays into the tower (SLAC).
- Data acquisition (Stanford).

Tracker Front-End Readout

- 25 64-channel amplifier-discriminator chips per detector plane.
- 2 controller chips per plane—1 at each end.
- Data in each chip can be shifted to the left or the right controller.
- Each readout chip can be initialized and controlled by either controller chip.
- All data and commands are passed on differential serial lines.



- Formatted, zero-suppressed data are passed down through the controller chips in a token-controlled readout.

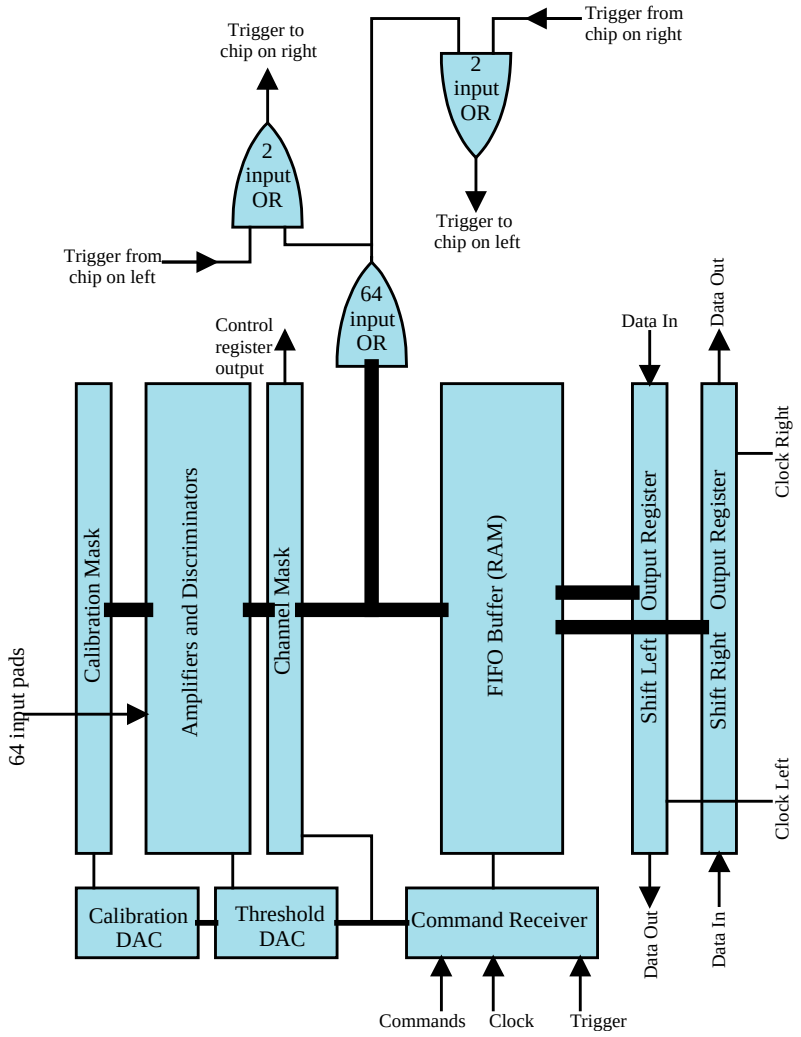
Front-End Readout Chip

Differences from beam-test chip:

- 64 channels, 195-micron pitch.
- Calibration mask to select any set of channels to pulse.
- 7-bit DACs for calibration and threshold levels.
- 8-deep FIFO event buffer.
- Redundant command decoders and output registers—each chip can be controlled by either controller.
- Low-voltage differential I/O.

Status:

- Schematic-level design complete.
- Mask design in progress.
- Simulation and other verification steps in progress.

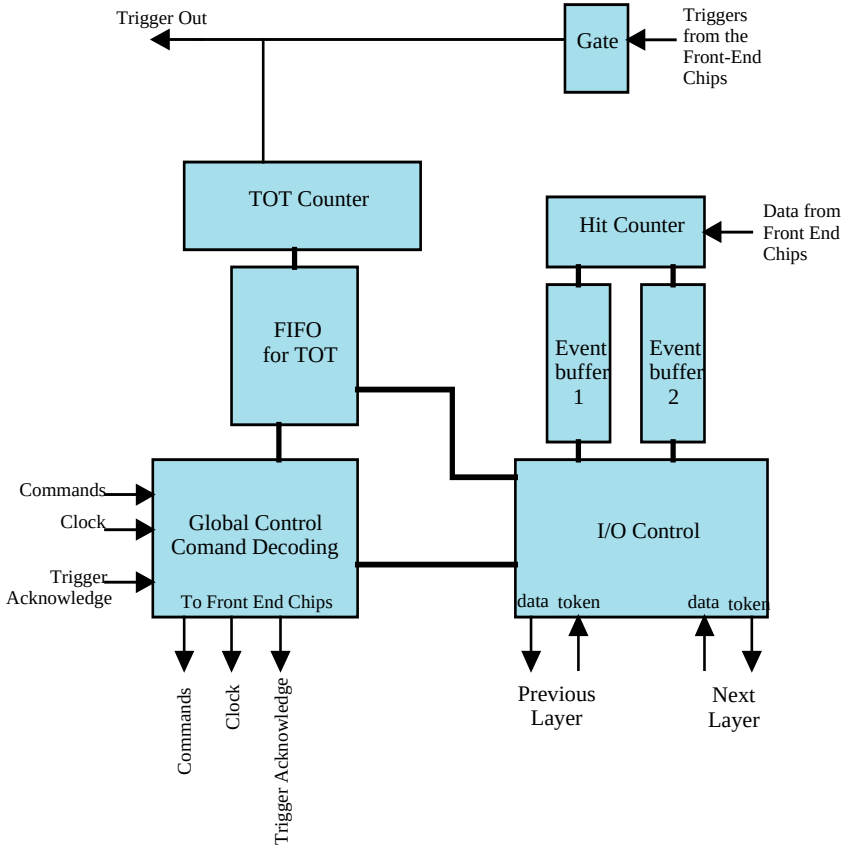


Tracker Controller Chip

- Control initialization, calibration, and readout of the front-end readout chips.
- Sparse readout—build list of hit-strip addresses.
- Calculate the time-over-threshold of the prompt trigger output.
- Build events and coordinate the readout with neighboring layers via a serial data line and a token.

Status:

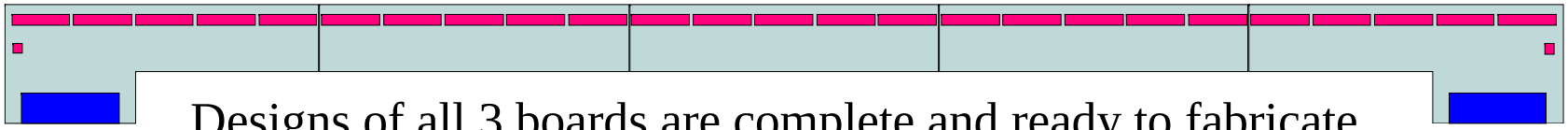
- Only the conceptual design exists.
- An experienced digital IC designer recently arrived from Europe to do the detailed design and layout.
- Cadence CAD system and MOSIS CMOSX design kit have been obtained and installed for use on this design.



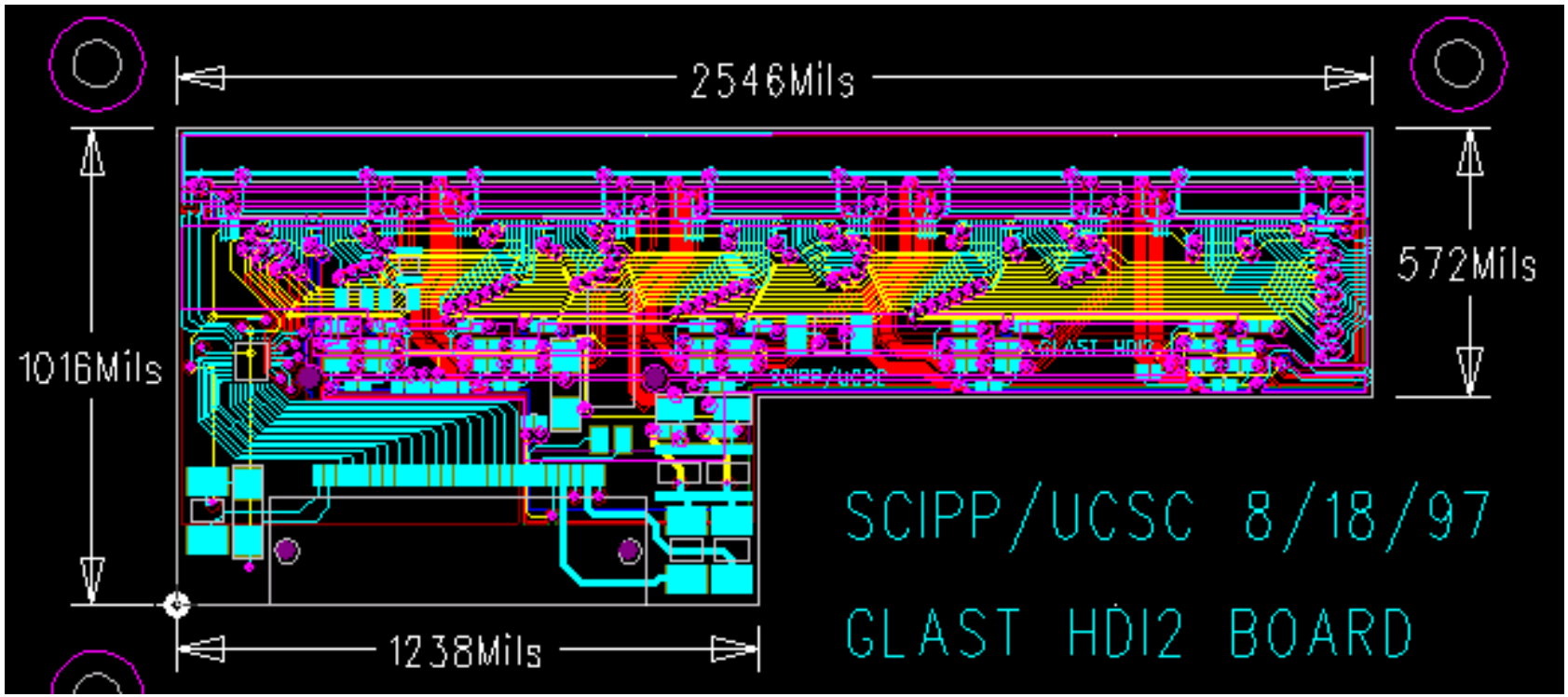
- Design will use standard CMOSX cells and automated place-and-route.

Tracker Hybrid Circuits

8-Layer Printed Circuit Board



Designs of all 3 boards are complete and ready to fabricate.



Hybrid Circuit Characteristics

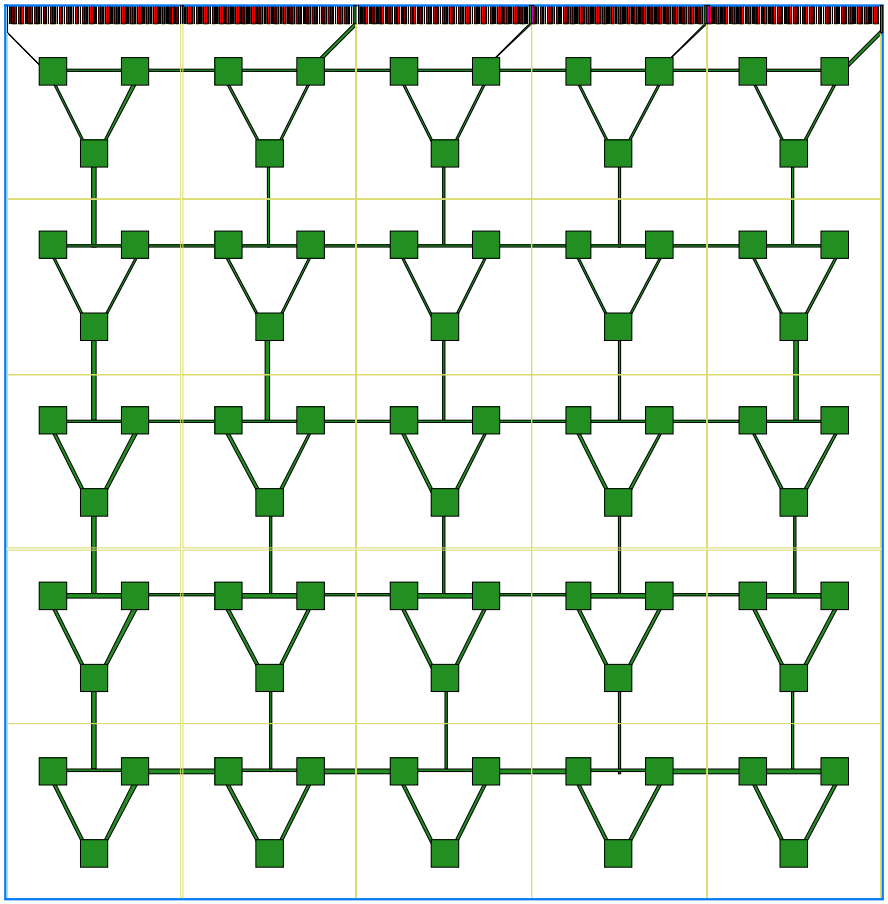
- Solid ground and power planes are used to shield completely the analog traces from digital activity.
- Wide traces and planes are used for low-inductance connections to regularly spaced decoupling capacitors.
- A solid HV plane provides a low-inductance path from the detector backs to ground via decoupling capacitors. In general, the signal current is returned via a low-impedance path that is well shielded from digital activity.
- Fuses and filtering circuitry are present on the power inputs.
- The end hybrids include temperature transducers.
- Wire bonds must be used to connect from one board to the next.
- A ledge forward of the chips is used for gluing down the Kapton interconnect prior to wire bonding.

Kapton Flex Circuit Interconnect

- Single layer of conductors.
- 3 pads to supply bias to the backs of each of 25 detectors.
- 5 traces to bond to the bias-voltage plane on the hybrids.
- 5 traces to bring the ground of the hybrid around the tray corner to the detectors.
- 1600 traces to bring the signals from the detectors around the tray corner to the readout chips.

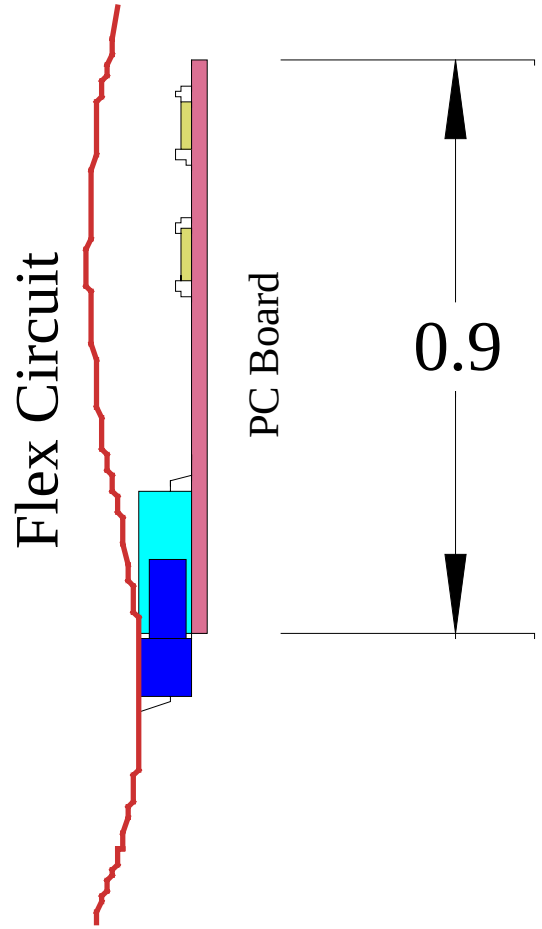
Status:

- Consulted a vendor—it appears to be manufacturable.
- Detailed design is nearly complete.



Tracker Inter-Layer Cabling

- Samples of space qualified miniature connectors have been obtained and are being evaluated.
- Design will begin soon of a multi-layered flex circuit to connect from layer to layer.
- Standoffs and clamps for supporting the flex circuit still need to be designed.



Hybrid and Tray Assembly and Testing

This is still a ways off, but preparations must begin:

- A $200k NSF grant has been obtained by UCSC to purchase an automated large-area wire bonder and an automated probe station.
- A large room at UCSC has been dedicated to GLAST assembly work, as well as other rooms for testing and prototyping. One major task there will be setting up the necessary electronics test stations.
- A room at SLAC is being set up for the tower assembly.
- Work should begin soon at SLAC on design and construction of assembly jigs, especially that required for precision placement of the detectors.

Tracker Prototype Fabrication Schedule

- *There is no serious, detailed schedule that is being tracked at this time.*
- Nevertheless, the critical path appears to be the ASIC design and prototyping (not unusual in this type of project).
  - The front-end readout chip can probably be submitted for prototyping in early November.
  - It is too early to tell how fast the controller chip design will go, but the hope is to have the design ready for a January submission. In principle this is much easier than the readout chip—it is nearly all digital and will be composed almost entirely of standard cells that are already designed, tested, and modeled. Automated tools are being used: logic synthesis, followed by automatic place and route.
- Hence, an *optimistic* forecast (*i.e.* assuming only one prototyping round) is to have prototypes of all electronics components in hand in March, 1998.

Conclusion

- The design of the first prototype tower is well advanced, and most parameters are frozen or need to be frozen very soon.
- At the same time, we will continue to investigate how best to build the eventual GLAST flight instrument.
- The basic detector and readout concepts have been verified on the lab bench and will soon be tested in a beam.
- The detailed readout electronics design is progressing but remains a critical path in the schedule of the prototype tracker. The interface with the data acquisition needs to be firmed up at this time, as the controller chip design is in progress.