GLAST Silicon-Strip Tracker Progress Report

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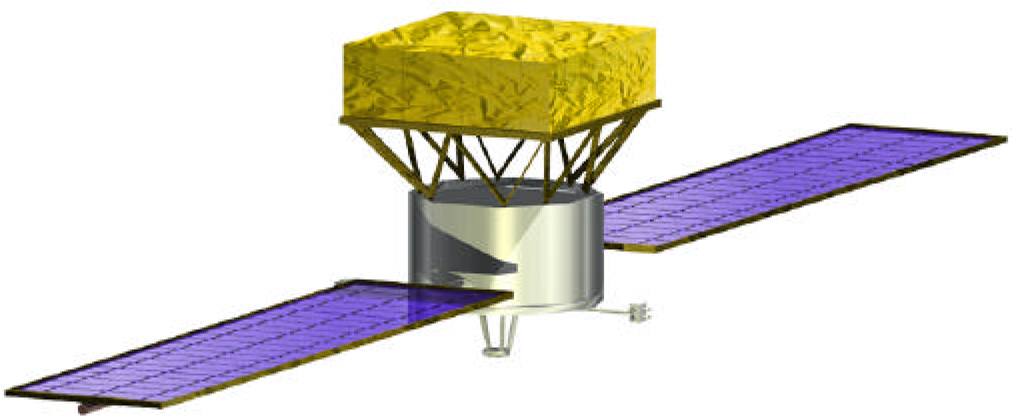
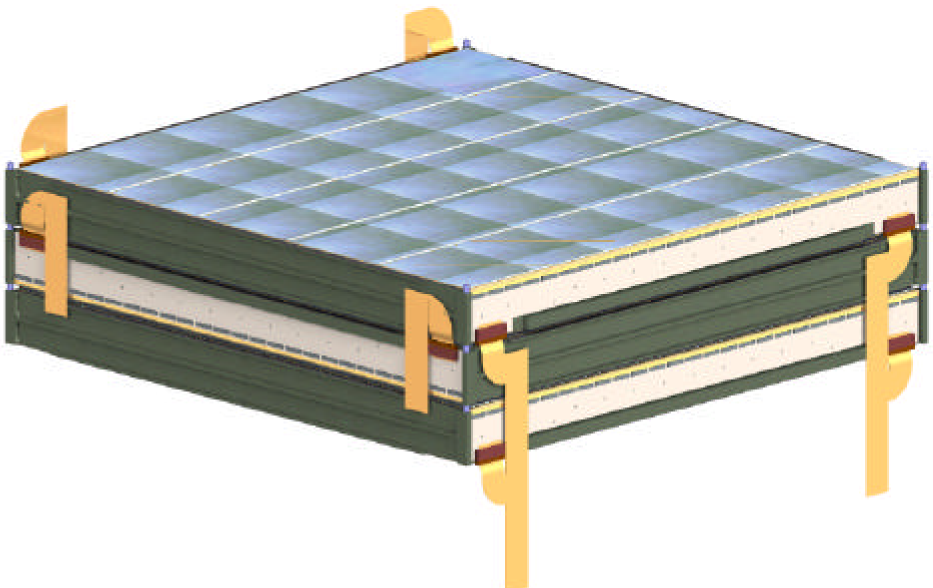
- Mechanical Design
- Tray Core Material
- Bigger towers? More Layers?
- Reconstruction Improvements
- Electronics
- Quality Control
- Prototype Tower Construction



Mechanical Design



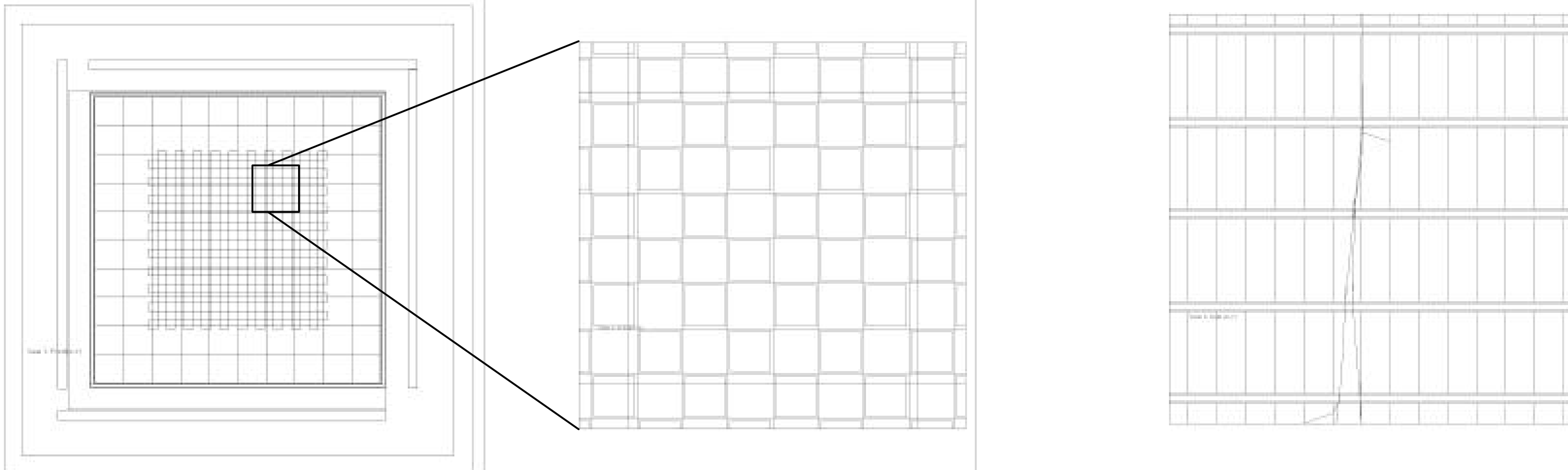
Three stacked tracker trays, with kapton cables attached. Corner posts align the trays and hold tensioning cables. Thin carbon-fiber walls attach to all four sides to conduct heat and add structural support.

No significant design changes since the June 1998 collaboration meeting.

- All dimensions of the closeout design have been agreed upon and fixed.
- The electronics design has been integrated with the closeout design.
- Some aluminum closeouts have been machined.
- The choice of core material and structure is still under study (Monte Carlo simulations).
- The face-sheet material and thickness is also still under study (structural analysis).

Tray Core Material Trade Study

Top View - 1 Tower   *Blow up of Core*   *Example Track Crossing Wall*



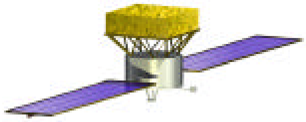
On axis 100 MeV γ's have ~ 32% chance of having the higher energy track cross cell walls.

Grazing angles produce large multiple scatters.

Issue: can hex-cell be used as a tray core material?

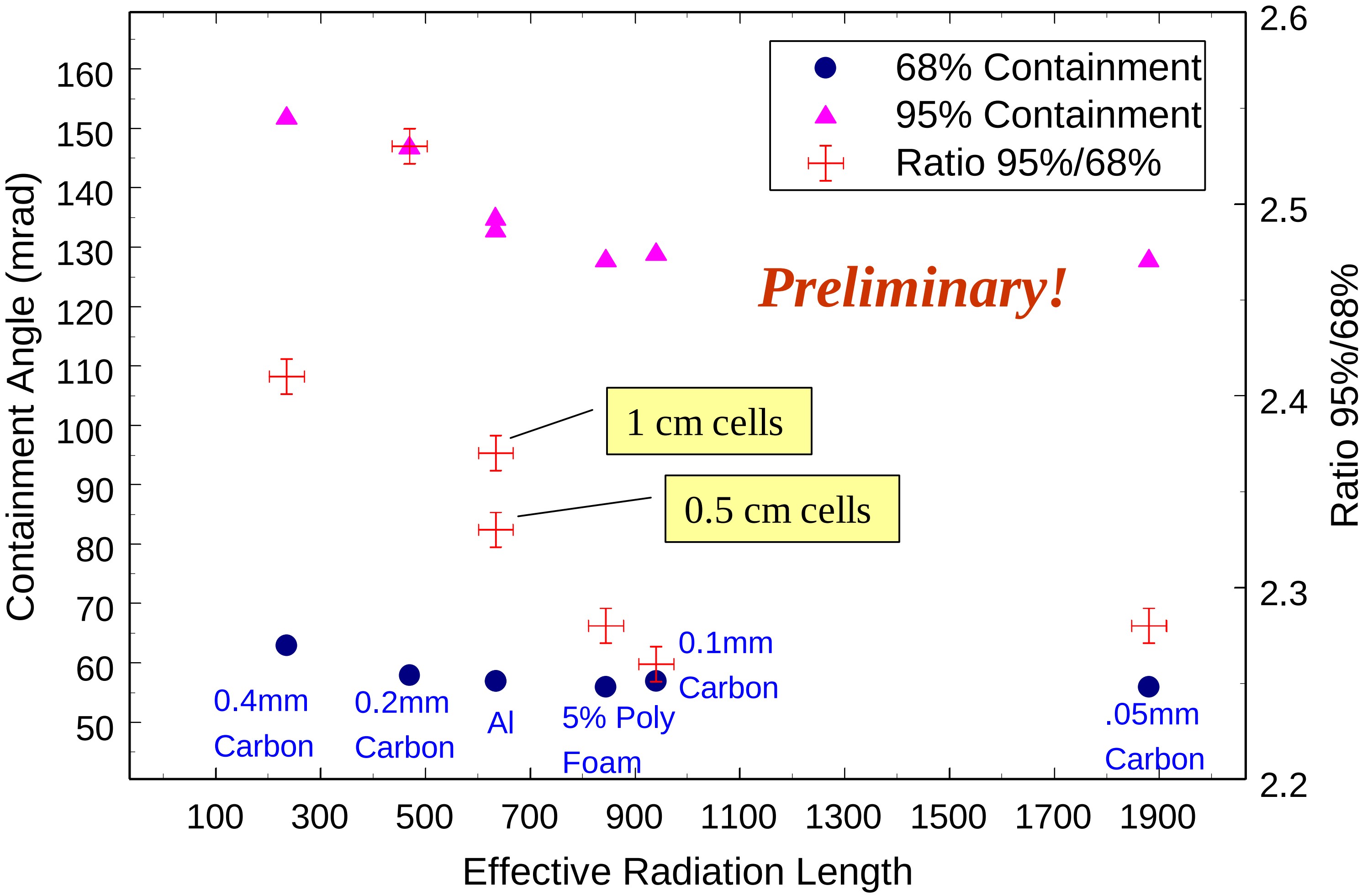
- Advantage: Cost and availability.
- Risk: Increased tails on PSF's at low energy.

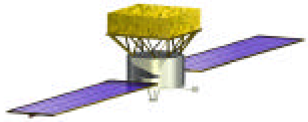
Simulate in GLAST-Sim with square cells.



Tray Core Material Trade Study

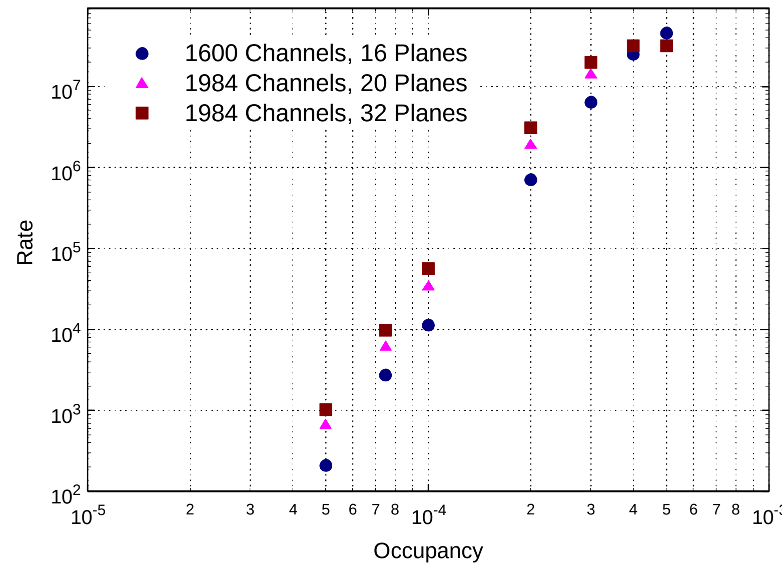
Monte Carlo Simulation Results for 100 MeV On-Axis Photons

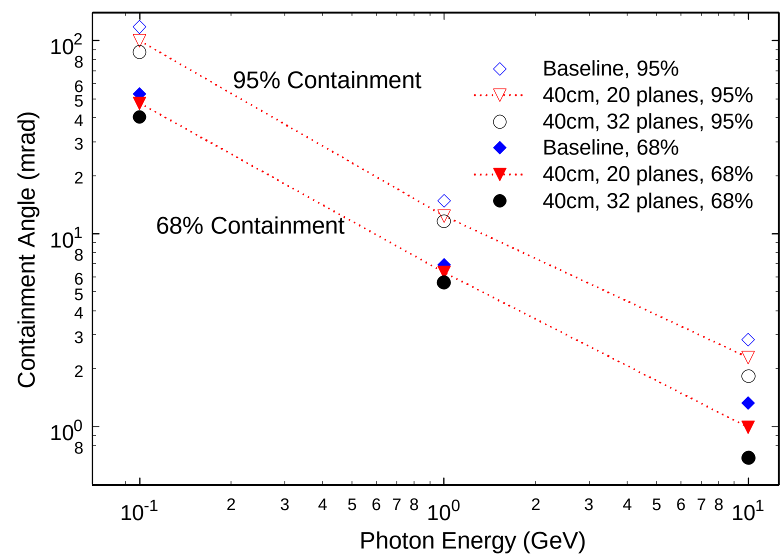


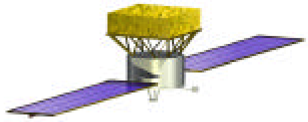


Evaluation of 40 cm Trays

- A partial draft has been prepared to compare the baseline (32-cm trays, 5×5 array of towers) with a 40-cm design (4×4 array).
- Tentative conclusions:
  - On paper, the signal/noise looks OK with the existing electronics, (Total ENC=1770 e⟶2060 e; 2400 e is the maximum tolerable).
  - But the performance needs to be verified with the prototype tower.
  - There are no serious mechanical or thermal problems with 40-cm trays. CsI calorimeter probably okay.
  - 32 planes probably not ruled out from mech/thermal point of view.
  - 32 planes gives 0.75 improvement in resolution at 100 MeV (thinner converters); 0.5 at very high energy (double the lever arm); slight improvement at 1 GeV.
  - 20% increase in total instrument power for 32 planes. About 450 kg increase in mass.
  - With 16 planes and 40 cm trays, the power and weight are improved.





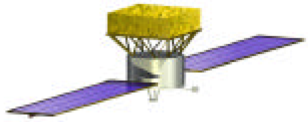


Improvements in Reconstruction

- Kalman Filter introduced for track fitting (talk by Jose Hernando at GFST meeting on Tuesday).
- Work in progress to integrate the Kalman filter into the pattern recognition, to treat the event globally (Hernando's talk).
- Meanwhile, the pattern recognition recently has been greatly improved:
  - Prevent loss of efficiency from noise hits and calorimeter back-splash hits.
  - As a bonus, the PSF is improved slightly.

Pattern Recognition Algorithm:

- Combinatorial "Hypothesis" Generator
  - Use calorimeter energy centroid as "seed"
  - Loop over tracker hits, starting in layer furthest from calorimeter
  - Two hits define a line … select hits consistent with the line.
- Find an Acceptable Set of Tracks
  - quality criteria are used to limit the size of the set (typically < 10)
- Order this set to find the "best" solution



Pattern Recognition Upgrade

Pattern Recognition Problems

- Strong bias to use first hit layer in fits, in order to avoid degradation of the PSF at low energy.
  - Failure to use first hit gives about a factor of 2 degradation in resolution!
  - ***But***, old algorithm fails in the presence of noise hits. *Impossible to find tracks correctly with hits 3 or more layers prior to the conversion point!*
  - Gives falling A_{eff} with increasing E_γ (increasing # of back-splash hits).
- Complete decoupling of *x* and *y* projections ⇒ incorrect material thickness used to compute multiple scattering error.

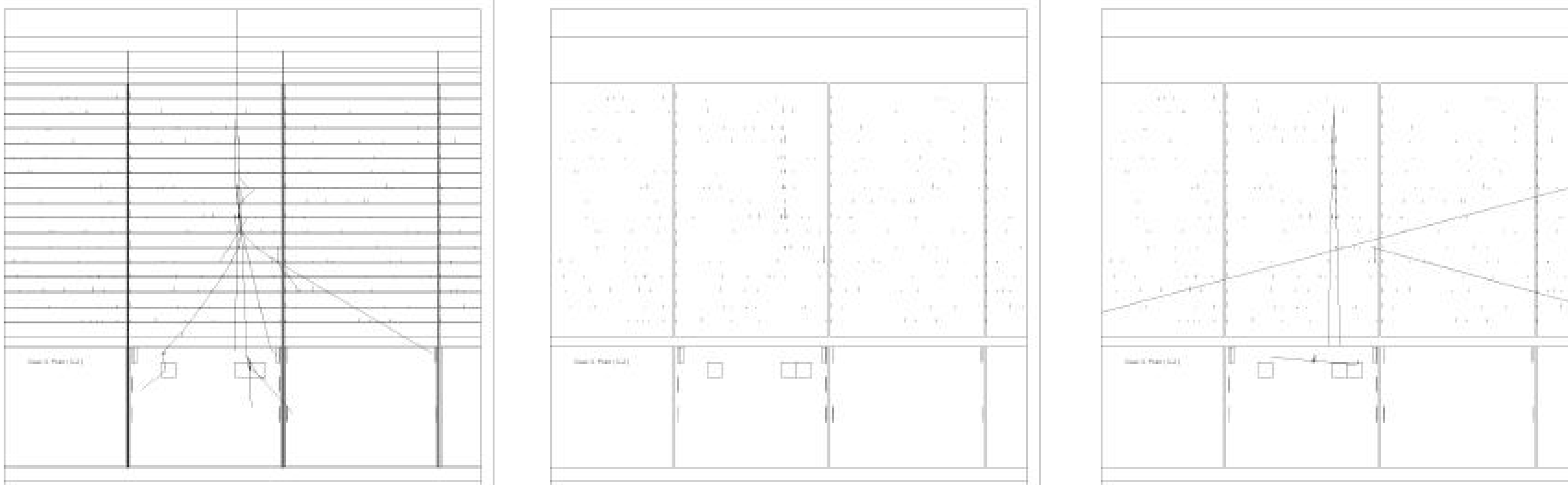
Solutions

- Make selection and ordering criteria independent of 1st-hit layer
- Eliminate solutions with partial hit complements
  - Tracks with subsets of hits can often have better “quality” than full track.
  - Discard solutions with subsets of hits in already found tracks.
- Interate solutions
  - Feed the missing projection in (couple *x* and *y*).
  - Bias *x* and *y* solutions to start in the same layer, using a penalty function.

Pattern Recognition Upgrade

The new code works well, independent of random noise and back-splash, and it even improves the angular resolution by about 10% at low energy.

MC Event | Detector Response | Reconstructed Event



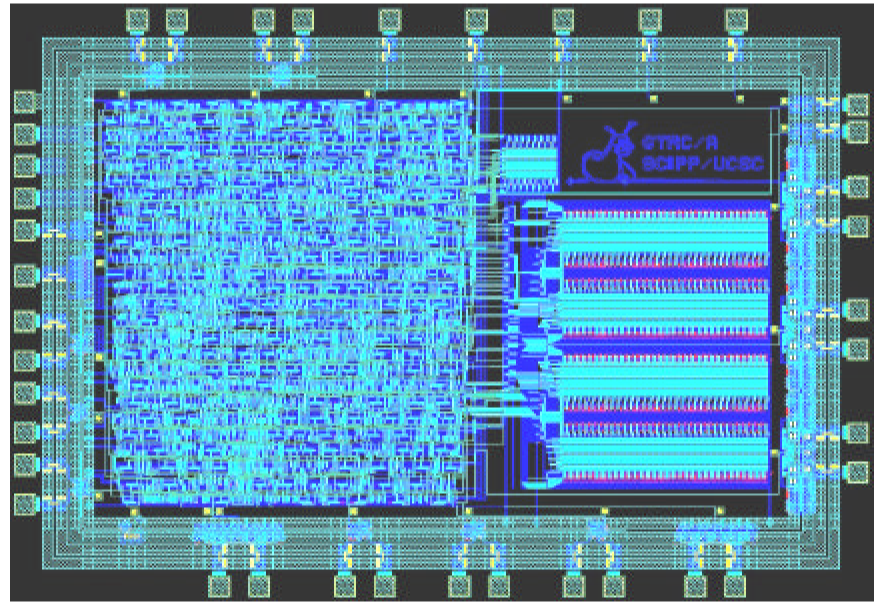
Example of a 100 MeV Gamma Event
with Noise Occupancy = 5×10^{-4}

(for illustration)

Tracker Readout Electronics

ASIC's

- The readout controller chip prototype was received and tested. It is 100% functional and works well together with the front-end chips. Only two modifications are needed:
  - Disconnect the banana slug from the power rail!
  - Change the reset pad to active high, to agree with the front-end chips.
- The second front-end chip submission (GTFE64-B) was also received and tested. The yield was 24 good chips out of 25!
- We now have enough prototype chips to instrument a complete readout section, which is under construction.



The GTRC controller chip layout.

Power

Based on ***measurements*** of the GTFE64 and GTRC chips, the tracker power works out to 219 μW/ch, including data transmission and detector bias.

Tracker Readout Electronics

Digital Noise Problem

- Turning the readout clock on or off injects charge into the amplifiers close to the desired threshold level. ☹
- With the clock already on, moving various patterns of data through the readout register induces noise far below the threshold level. ☺
- The digital layout of the GTFE64 chip has been completely redone to improve the isolation between the analog and digital grounds. We hope that this will make it possible to keep the trigger active during readout.
- The new design (GTFE64-C) cannot be submitted until October 21. ☹

ASIC Production Plans

- Fabricate 75 to 100 GTRC chips October 21 to early January.
- Fabricate GTFE64-C prototype October 21 to early January and then test quickly (≈2 weeks).
- Prepare in advance two production submissions of the GTFE64 chip
  - C version, to use in case of a successful test of the prototype.
  - B version, in case the C prototype is a failure.
- Submit production for 20 wafers of GTFE64 chips in late January.

Feb 3 is the drop dead date, as HP will decommission the 0.8 μm foundry!

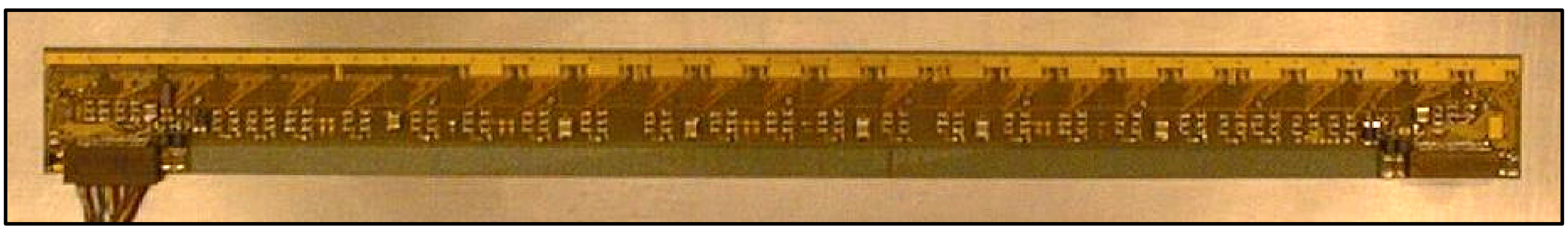
Tracker Readout Electronics

Hybrid Circuit

- The full-size (1600 channel) PC board has been fabricated and tested.
- It has several errors and will need to be iterated, but workarounds have been found for purposes of prototyping.
- Up to now, two front-end chips and one controller chip have been operated successfully on the hybrid.
- Total average thickness, including all parts: 1.35% radiation length.

Kapton Flex Cables

- The design of a prototype for two layers has been completed and submitted for production. It will be used in the first tests of the readout with the Stanford prototype DAQ system.
- The design has been integrated with the tray closeout design.

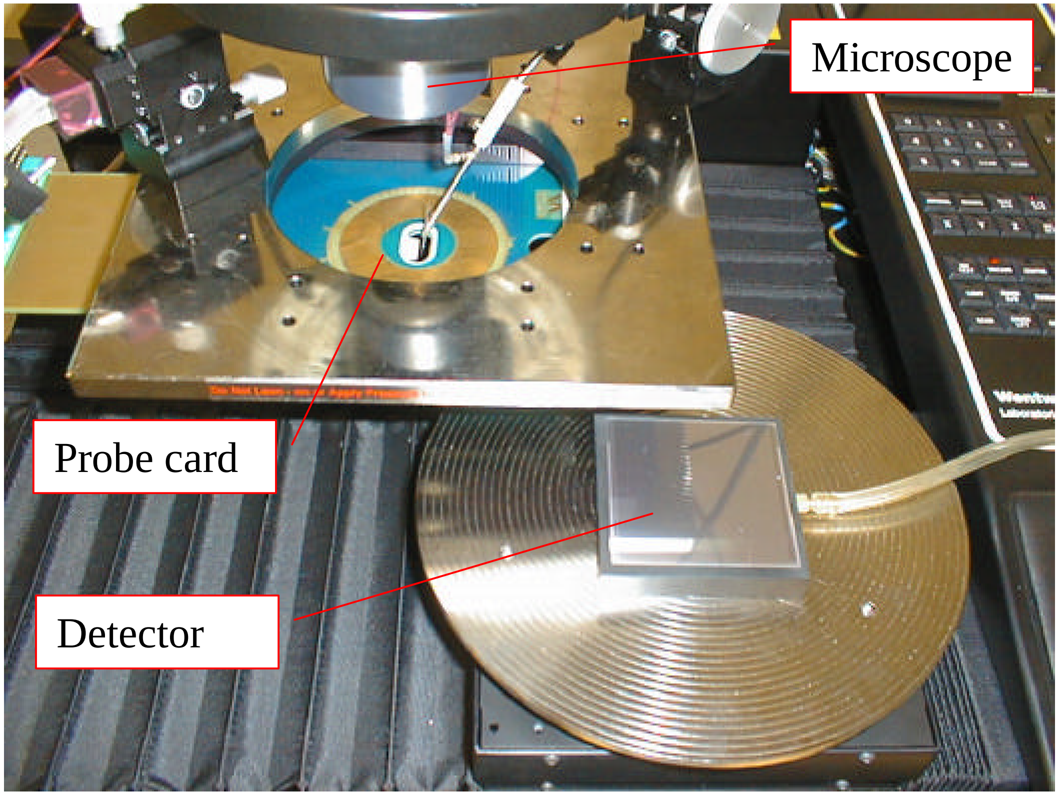


Hybrid circuit with one controller chip and seven front-end chips loaded.

Tracker Quality Control

Detector and ASIC Test Stations

- We now have experience with testing detectors in quantity with the UCSC automated probe station.
- A test station for the GTFE64 chip has been constructed (probe card, interfaces to electronics, software, test patterns). It was used to test the 50 chips produced so far.
- A similar test station for the GTRC chip is under construction, to be followed by a test and burn-in station for the completed hybrids.

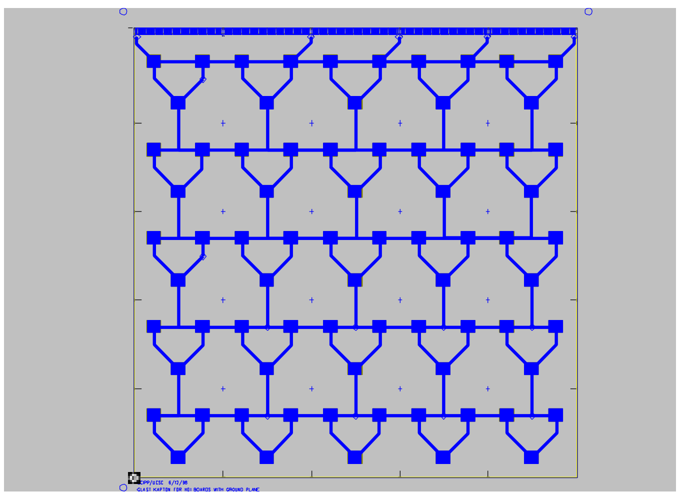


The automated probe station, with the probe card for detector installed.

Tracker Tray Assembly

Kapton Detector Interconnect

- The final prototype has been fabricated and appears to be of good quality.
- Thickness is 0.18% radiation lengths. We plan to halve the copper thickness in the production version.



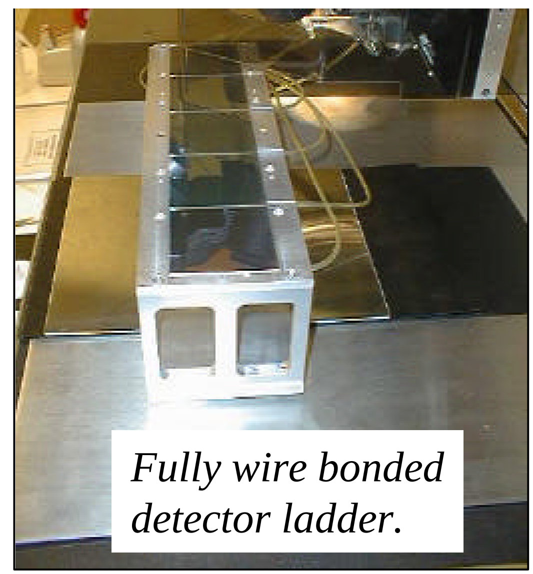
Layout of the top layer of the kapton detector interconnect.

Detector Ladders

- Several ladders of reject detectors have been edge bonded with epoxy.
- One ladder was completely wire bonded without difficulty.
- A spray method has been found that does an excellent job of encapsulating the wire bonds in epoxy.

Jigs

- Various gluing and wire bonding jigs and storage boxes are under construction.



Fully wire bonded detector ladder.

Proto Tracker Schedule Highlights

- This month: complete tray of dummy detectors (1 side).
- Oct: complete and test fully functional tray (1 side). Structure will be all aluminum. First tests of readout with prototype DAQ system.
- Dec: order parts and materials for building the trays.
- Jan. ‘99: GTRC production complete. Hybrids and flex circuits completed.
- April ‘99: all front-end ASIC’s in hand and tested.
- May ‘99: all detector wafers in hand and tested.
- July ‘99: 17 trays completed.