GLAST Tracker Readout Electronics Status Report

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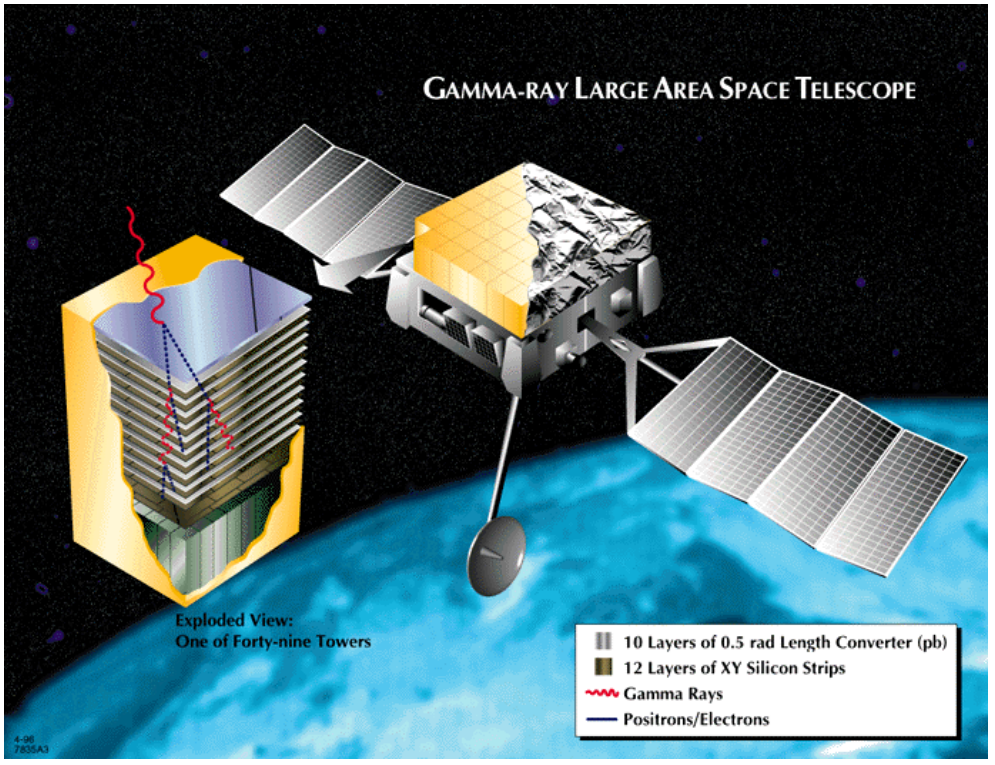
- Review of the design.
- 1997 beam test performance.
- Readout chip design.
- Controller chip design.
- Hybrid circuit design.
- Kapton interconnect.
- Cabling and connectors.



Cast of Characters

Engineering:

- Gerrit Meddeler
- Pavel Poplevine
- Ned Spencer

PC Board Design:

- Serguei Kashiguine
- Delbert Rassmusson

Testing and Measurements:

- Jose-Angel Hernando
- Masaharu Hirayama
- Wilko Kröger
- Andrea Pocar

Electrical Assembly:

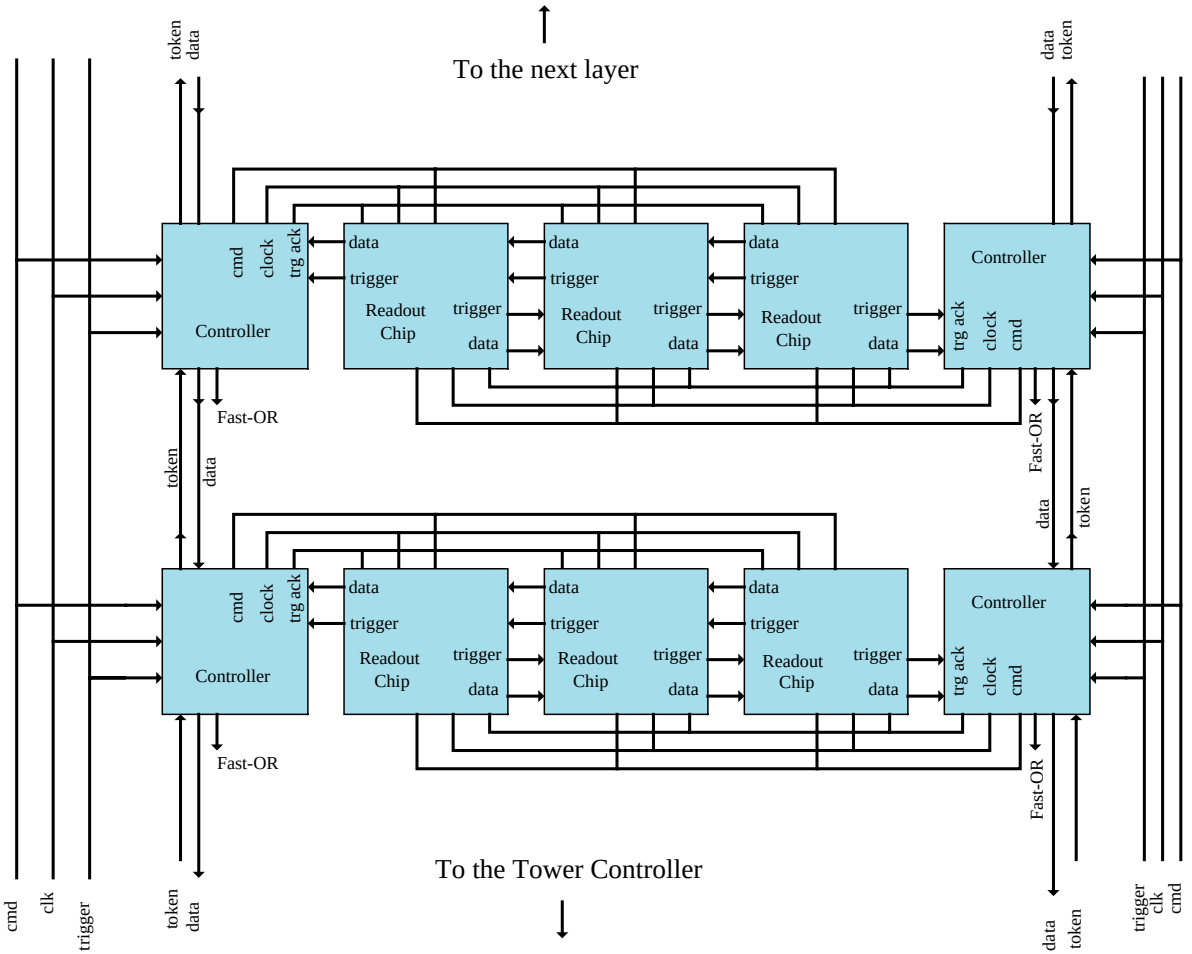
- William Rowe

Machining and Assembly:

- Alec Webster

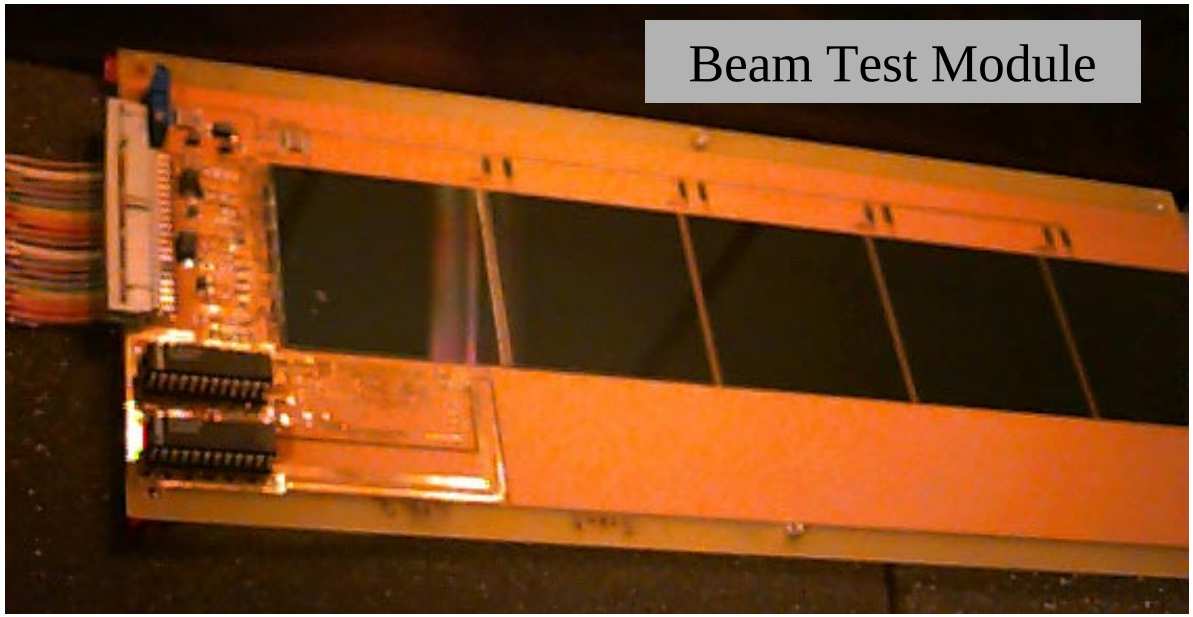
Review of the Conceptual Design

- 25 64-channel readout chips per layer of detectors.
- A readout controller chip at each end of the chain of readout chips.
- Each chip can be controlled and read out by either controller, for redundancy.
- Sparse readout.
- Data come out in a serial stream, one layer at a time.



Beam Test Electronics

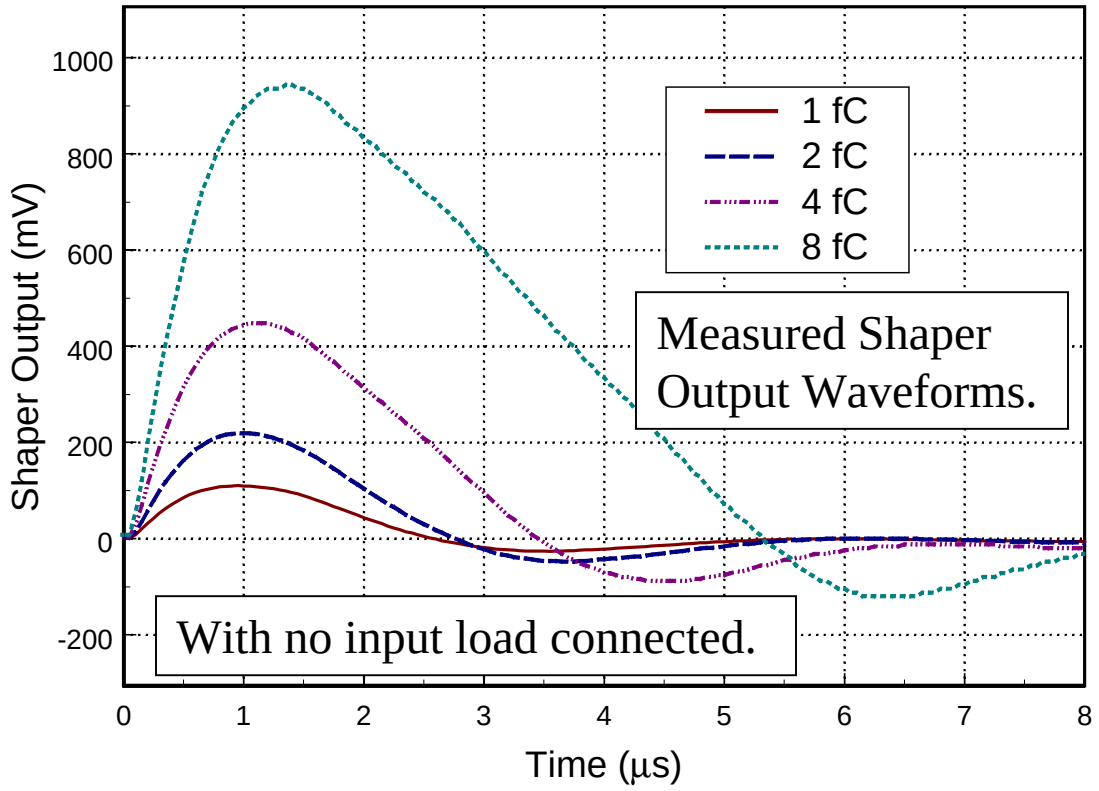
- One side of one beam test module was implemented with the full set of 5 detectors in order to make a realistic test of the signal-to-noise performance.
- Unfortunately, the company that did the wire bonding damaged the detectors (see the talk by Jose Hernando), making many channels dead or noisy.
- Nevertheless, we could still study channels connected to undamaged regions of the detectors.



Beam Test Electronics

- The shaping time for this chip was reduced with respect to the first prototype to bring it closer to 1μs. In effect, it was reduced from 1.6 μs to 1.3 μs with a 38 pF load.
- That increased the noise, for 38 pF, from 1400 electrons to about 1600 electrons.

- Measured power dissipation: 140μW per channel.
- Gain: 115 mV/fC.
- Measured noise, when connected to 5 detectors: 1600 electrons, except near damaged regions.

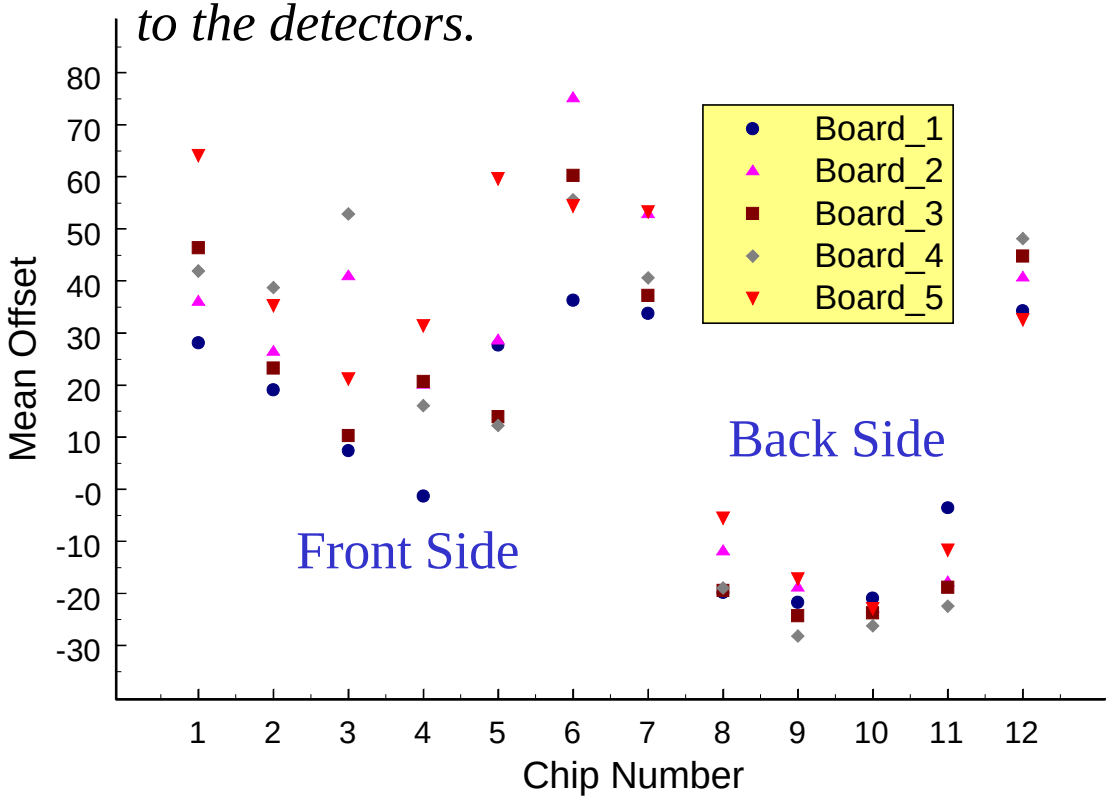


Beam Test Electronics

The beam test modules have a problem that when multiple channels are enabled, activity in the trigger logic feeds back and shifts the discriminator thresholds.

This effect is systematic with the position of the chip in the module and is believed to be due to inadequate grounding, shielding, and power-supply decoupling in the printed circuit board.

Measured threshold offset versus position of the chip in the module, before wire bonding to the detectors.



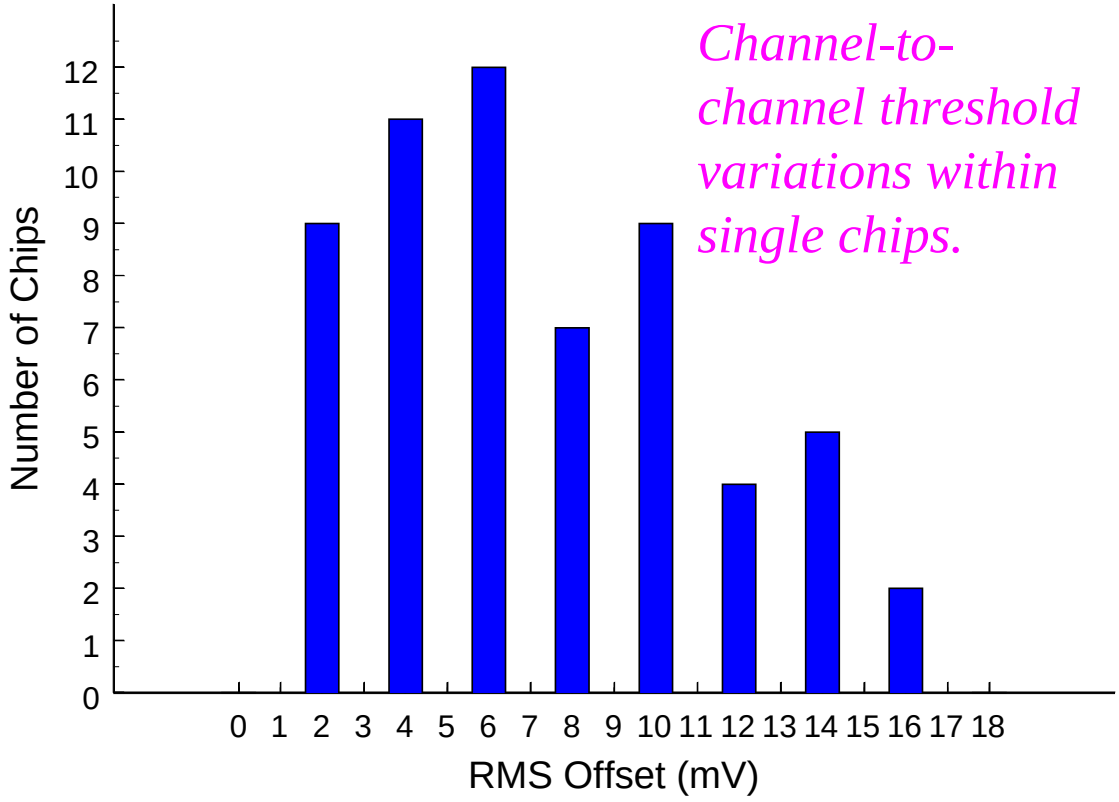
Beam Test Electronics

The noise and threshold dispersion meet the GLAST requirements:

- Minimum signal: 5.1×0.5 ×0.7=1.8 fC=206 mV for 400 μm detectors.
- Subtract 4σ threshold variation: 206 mV – 4 ×15 mV=146 mV.
- Noise: 1600 e=29 mV.
- **The minimum threshold is 5σ above the noise.**

Thus, our measurements indicate that it should be possible to achieve 100% efficiency with $<<10^{-4}$ noise occupancy.

But, we must fix the dependence of the offset on the trigger electronics (see talk by Wilko Kröger for more details.)



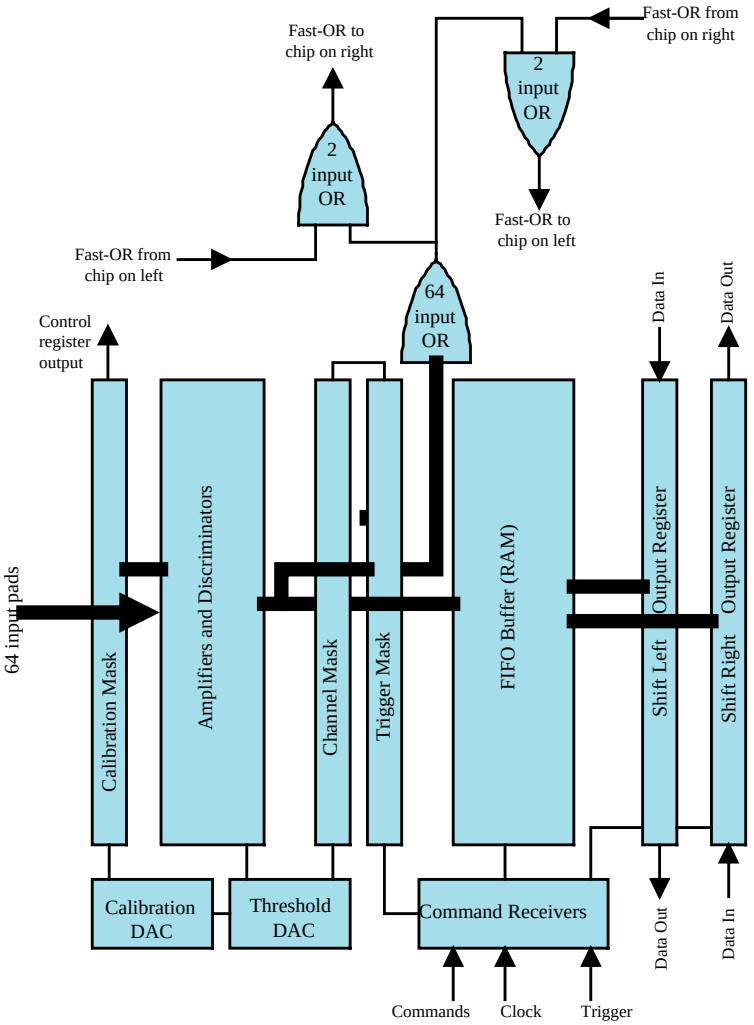
Channel-to-channel threshold variations within single chips.

Readout Chip Design

- **First prototype production of the full-scale chip was submitted in December and is due back next week.**

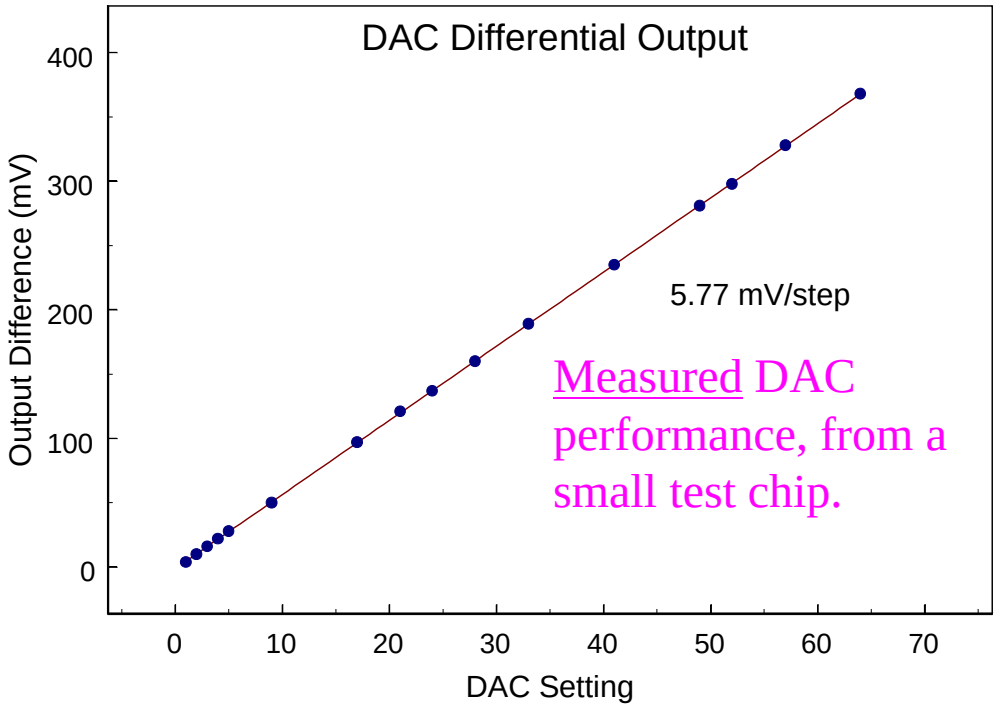
NEW FEATURES

- 64-channels, with 194 μm pitch.
- 8-deep FIFO for readout buffering.
- Left-right redundancy for the fast-OR trigger output and the data output.
- Dual redundant serial command decoders, to minimize control lines on the hybrid.
- Control input and trigger output via low-voltage differential signals (LVDS), to avoid crosstalk to the preamps.
- 3V digital operation, to minimize digital power and minimize crosstalk to preamps.
- 7-bit DAC for threshold control, to avoid bussing analog levels and to allow chip-to-chip variations to be removed.



Readout Chip Design

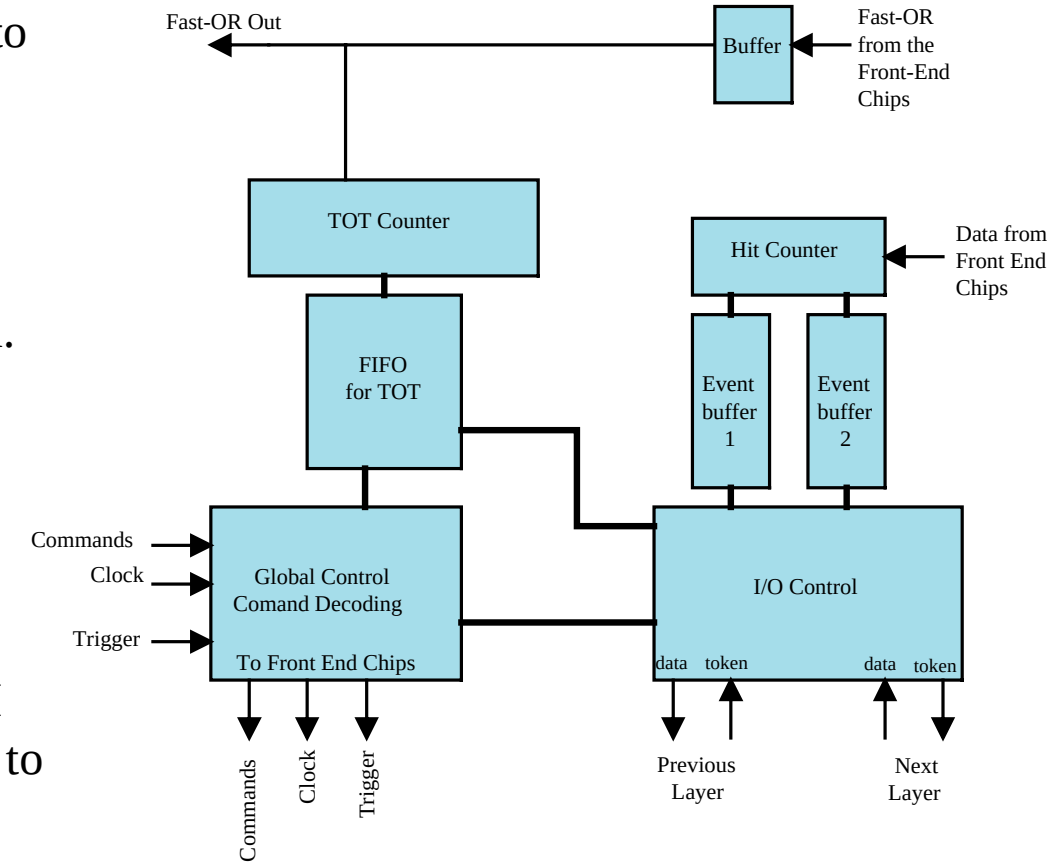
- 7-bit DAC and 64-bit mask for calibration, to avoid bussing analog calibration signals and to allow any subset of channels to be pulsed.
- Separate 64-bit masks for the data and trigger fast-OR output, to allow data to be kept from slightly noisy channels that must be masked from the trigger.
- (Sort of) sparse readout in the output register: only a single bit is output if there are no hits in the chip. Otherwise 65 bits are output. This can dramatically increase the maximum readout rate.
- Improved (we hope) transistor matching in the shaper, to reduce the threshold dispersion.
- Size: 11.7 mm by 2.2 mm.



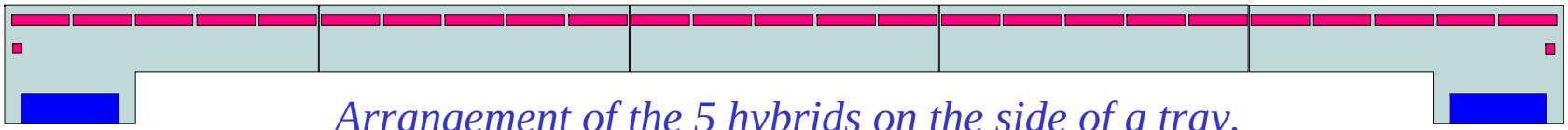
Oops! We already know of one bug, from simulations: a hard reset will be necessary before loading the control register each time. That will not hinder the testing and is easy to fix next time.

Controller Chip Design

- Functional specification are complete, including the interface to the Stanford DAQ.
- A complete Verilog HDL description of the chip has been made and thoroughly simulated along with the readout chip model.
- Now working on synthesis of the logic into standard cells, to be followed by automatic place and route.
- The LVDS cable driver design is still being evaluated. It, the RAM cells, and the pad frame will have to be laid out by hand.
- Target submission date: March 5.



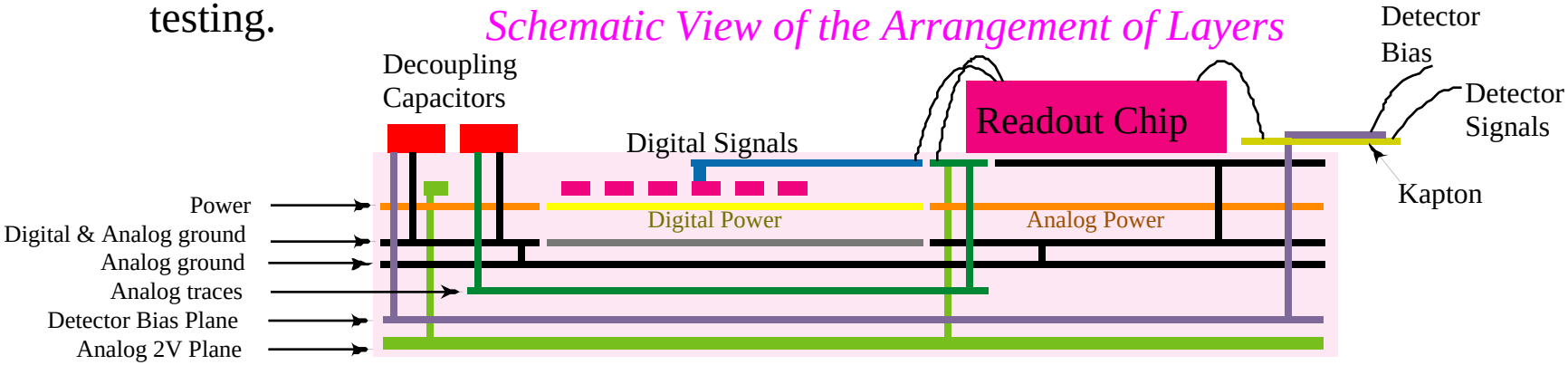
Hybrid Circuit Design



Arrangement of the 5 hybrids on the side of a tray.

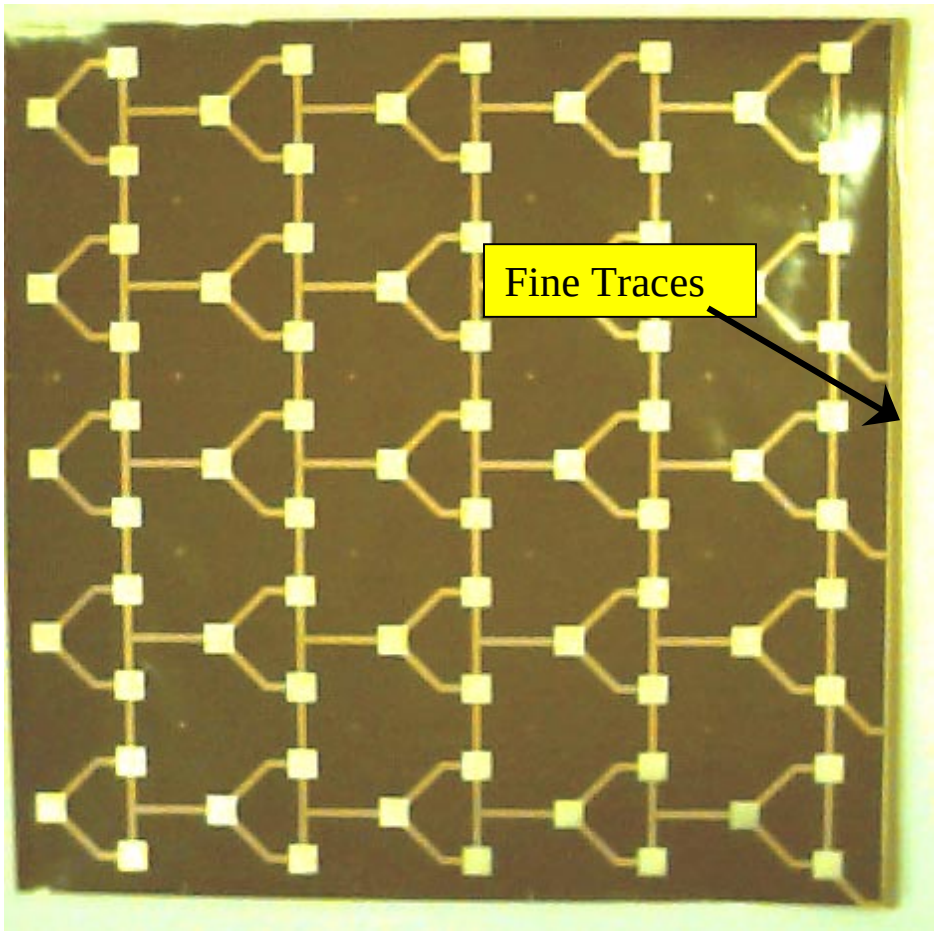
- Problems with noise pickup in the beam test boards led to an effort last summer to design a very robust hybrid.
- Four extra layers (total of 8) are used to provide
  - shielding between analog and digital sections
  - very wide, low-inductance traces to connect the chip to decoupling capacitors
  - complete plane to carry the detector bias to HV decoupling capacitors
- 30 pieces of the central board type were produced for mechanical and electrical testing.

Schematic View of the Arrangement of Layers



Kapton Interconnect

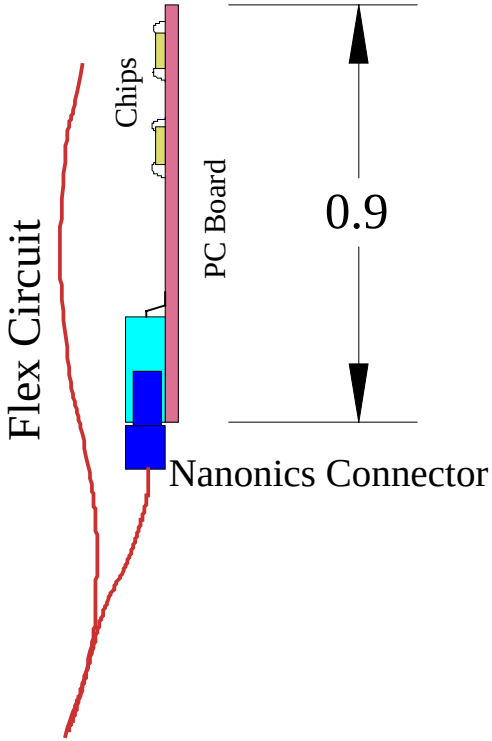
- This flex circuit is needed to
  - supply bias to the detectors
  - shield the detectors from noise
  - carry the signals and bias voltages around the corner of the tray
- There is some concern about whether it is practical to bend the narrow strip with ~1600 traces around the corner to glue to the 5 hybrids.
- We are investigating other possible solutions.
- And we are making trial assemblies to study the problem. So far the original concept looks promising, but lots of details need work.

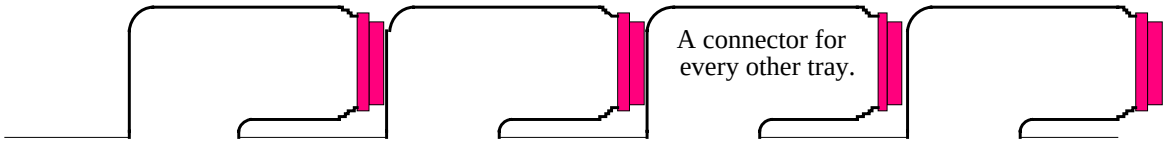


One of 6 kapton interconnects made so far.

Cabling and Connectors

- We have found a simple and robust method to connect a flex circuit cable to each of the readout sections on the side of a tower.
- The connectors must lie flat, to minimize the dead space between trays.
- This method makes a secure crimp connection from the cable to the plug and keeps the cable away from the plugs, to allow easy access.
- The Nanonics connectors are space qualified.





Tower Base

Digital traces, surrounded by digital power & ground.

Analog power & ground, plus detector bias.

Conclusions

- The beam test electronics worked well, except for some digital-analog interference believed to be due to inadequate grounding and shielding in the PC boards. The amplifier noise, threshold matching, and power meet the GLAST requirements.
- The complete 64-channel read chip prototype will be ready next week and will be tested on a greatly improved PC board.
- Recent modifications in the readout chip design will give
  - greatly increased readout speed, due to zero suppression at the front end.
  - better flexibility in controlling the trigger, due to the addition of separate masks for data and trigger.
- The trigger control could be improved even more by adding separate discriminators for data and trigger.
- The controller chip design is nearly complete.
- Designs of the hybrids, flex circuits, and cables are proceeding, and work is in progress to develop and evaluate assembly techniques.