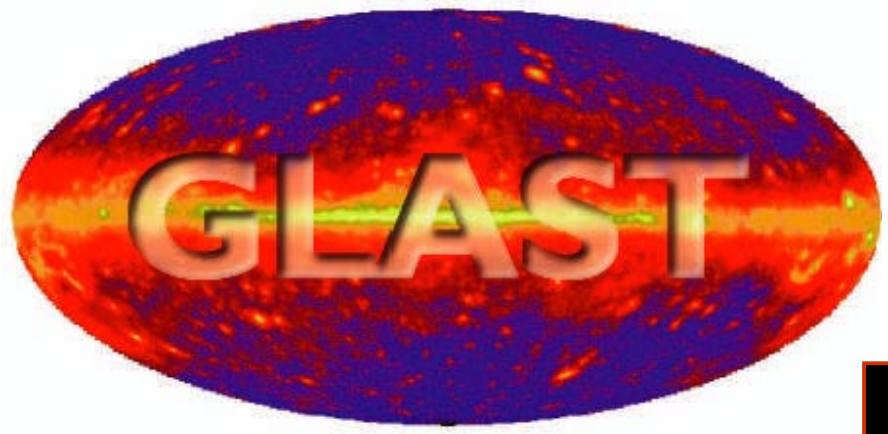
Gamma-ray Large Area Space Telescope

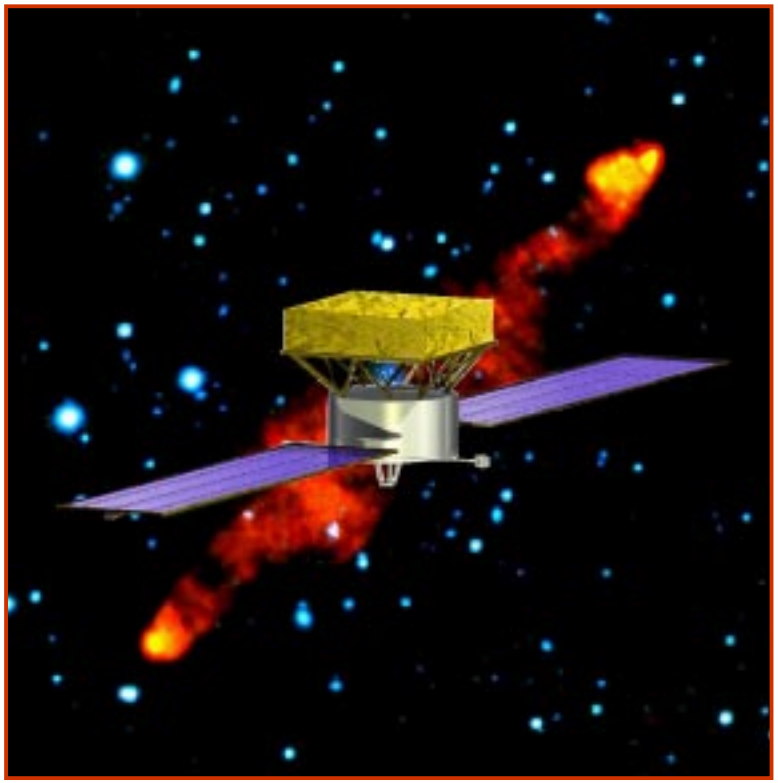


Technology Development I

Tracker & DAQ

Robert P. Johnson
University of California
at Santa Cruz

GLAST Council Mtg.
January 27, 1999



Technology Development Approach

Monte Carlo Simulations of Instrument:

- Verify science measurement capabilities of instrument design.
- Develop and model event triggers and DAQ; determine background rejection capabilities, γ-ray trigger efficiency, and develop realistic tracking algorithms.
- Tools for instrument optimization and trade studies.
- Eventually becomes an integral part of flight instrument calibration and science data analysis.

Demonstration of Integrated Measurement System

- Validate Monte Carlo simulations and hardware performance (e.g., beam tests: 1996, 1997, 1999).
- Instrument modularity allows prototype development and testing on an appropriate scale; establishes performance margins - reduce risk.
- Engineering prototype tower now under construction.

Development of Subsystem Technologies

- ACD: high-efficiency charged particle rejection.
- Tracker: low-power, low-noise readout; optimize mechanical/thermal design.
- Calorimeter: optimize calorimeter-shower imaging; low-power, large dynamic range readout.
- DAQ: system architecture to support flexible trigger modes; reduce data bandwidth.

ATD Engineering Prototype Tower

A major focus of the Silicon-Strip GLAST effort during the basic contract period is the construction and demonstration of a full-scale engineering prototype tower, including all four subsystems: ACD, Tracker, Cal, DAQ.

- Further validate our simulations of the performance of the instrument concept and design by operating the tower in beam tests.
  - Large angles of incidence not covered in the small 1997 beam test tracker.
  - Response to hadronic background particles.
  - Test non-uniform distribution of converter foils (see tracker trade studies).
- Reduce cost and schedule risks associated with the flight-instrument development by confronting engineering challenges at an early date. The goal is to make the tower as realistic as possible—a faithful, fully functional prototype of a full module of the flight instrument.
- Begin learning about assembly problems, where work needs to be done on redesign and tooling for mass production, quality control requirements, *etc*.
- Validate the GLAST technologies at a realistic scale and in a realistic environment of an integrated system of all four subsystems. For example:
  - Tracker readout electronics: noise occupancy, EMI, reliability.
  - Tracker trigger: noise rates, dead time.
  - DAQ: timing, reliability.

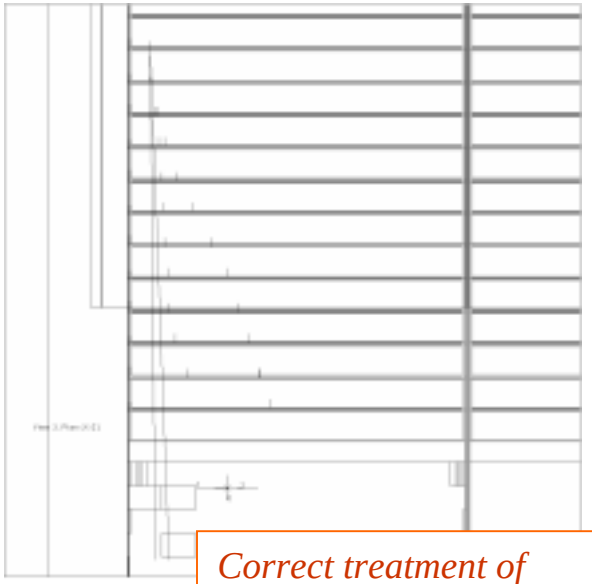
Outline

- Software Development
- GLAST Instrument Engineering
  - Preliminary Mechanical Engineering and Integration
  - Preliminary Thermal Engineering
  - Trade Studies
- Silicon-Strip Tracker Technology Development
  - Tracker Beam Test Results
  - Tracker Mechanical Design and Engineering
  - Silicon-Strip Detectors
  - Tracker Electronics
  - Electronics and Assembly Quality Control
  - Status of the Tracker for the Prototype Tower
  - Tracker Trade Studies
- Data Acquisition Technology Development
  - DAQ System Design
  - Status of the DAQ for the Prototype Tower
  - DAQ Trade Studies
- ATD Option I Objectives
- Conclusions

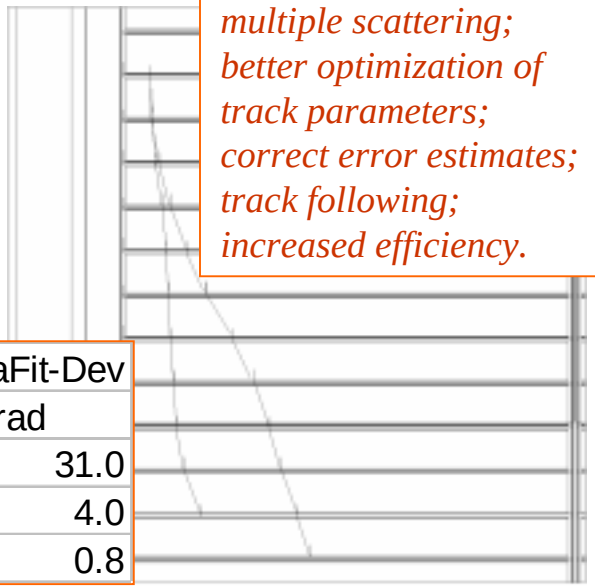
Software Development

- Continuing process of refinement of the simulation program.
  - Program structure (software engineering).
  - More detailed simulation (*e.g.* readout and trigger system).
  - Incorporation of changes in the evolving baseline design.
  - Support Trade studies of design options.
- Work in progress on the reconstruction program.
  - Kalman-Filter approach to track fitting and pattern recognition in the tracker.
  - Increased sophistication in energy corrections, resolution of ambiguities, *etc*.
  - Tuning of cuts in the algorithm, especially to track evolutions in the design.

GLASTSIM event with least-squares tracking.



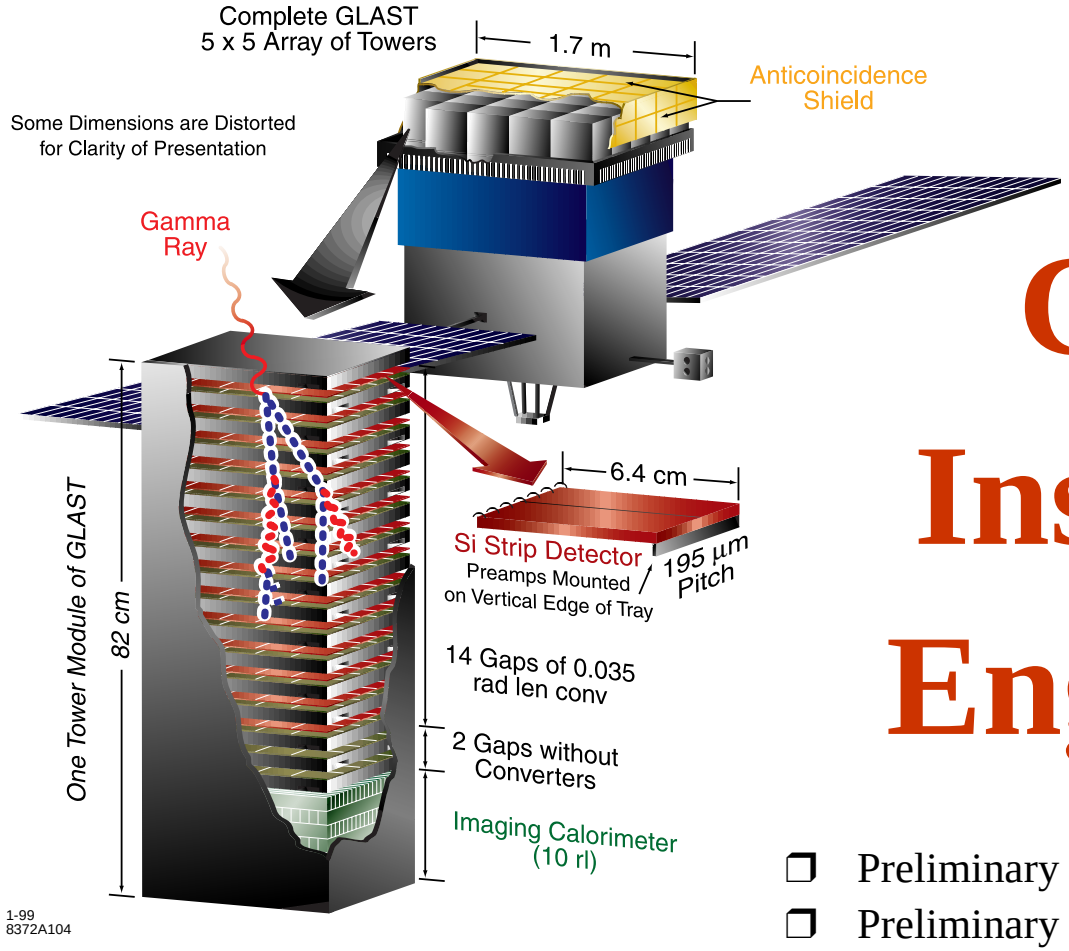
GLASTSIM event with Kalman Filter tracking.



Correct treatment of multiple scattering; better optimization of track parameters; correct error estimates; track following; increased efficiency.

*	LSQ-Dev	KaFit-Dev
	mrad	mrad
100 MeV	33.0	31.0
1 GeV	4.5	4.0
10 GeV	0.9	0.8

GLAST Technology Development I



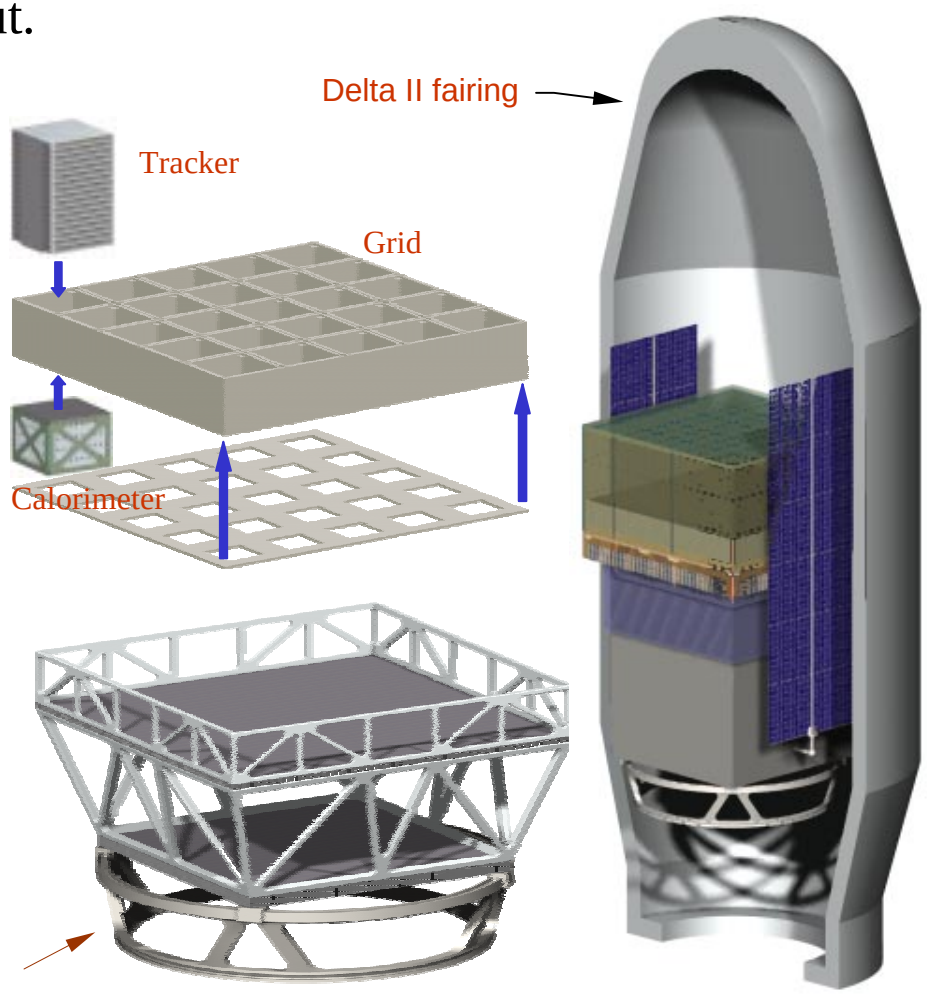
GLAST Instrument Engineering

- Preliminary Mechanical Engineering and Integration
- Preliminary Thermal Engineering
- Trade Studies

Mechanical Engineering & Integration

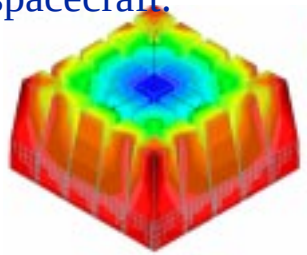
Significant preliminary mechanical engineering and thermal studies of the GLAST design have been carried out.

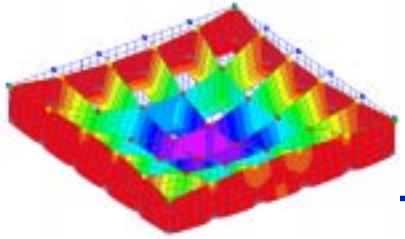
- Collaboration of SLAC & Hytec Inc. (Los Alamos):
  - Studies of integration of the GLAST subsystems into an instrument.
  - Preliminary looks at integration of the instrument onto the spacecraft and into the rocket fairing.
  - Stress, vibration, and thermal analysis of the designs, starting from the support ring.
- Lockheed:
  - Grid design and global thermal studies.

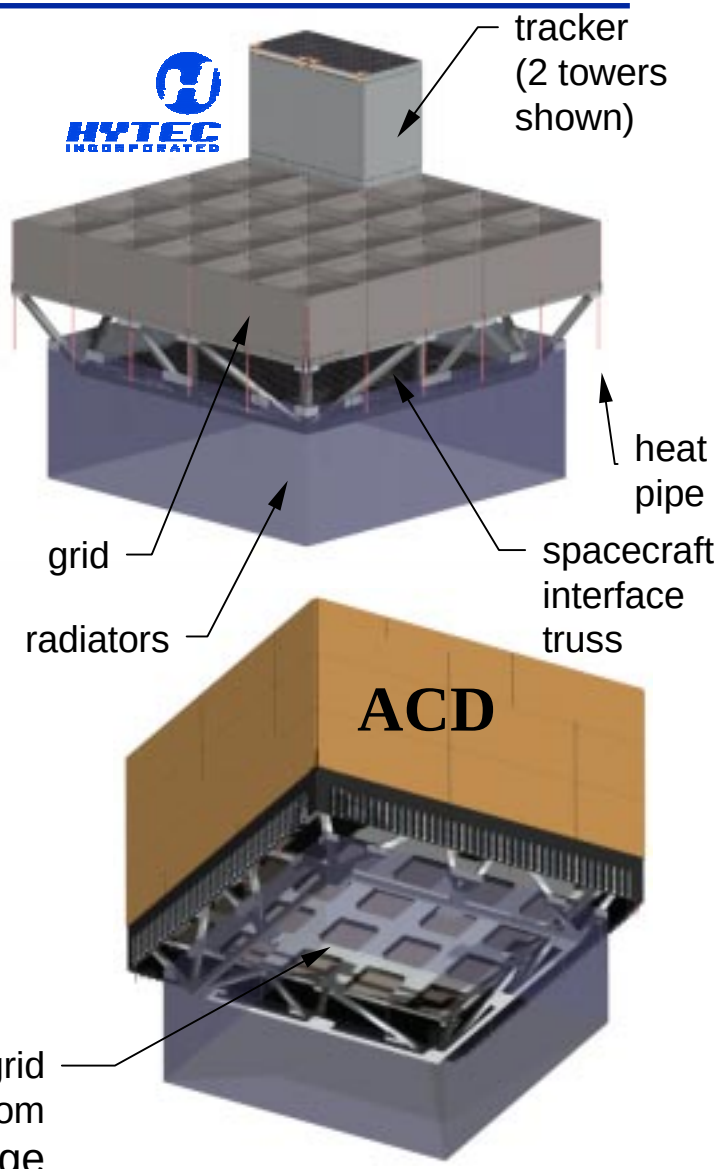


Instrument Engineering Analysis

- Engineering
  - Integration of the instrument components.
  - Dynamic analysis by FEM and lumped-parameter models. Meets Delta-II launch requirements.
  - First studies of integration with a spacecraft.
- Single Tray
  - Fundamental frequency > 400 Hz.
  - Deflection < 25 microns.
- Single Tower (top free)
  - Random vibration response (base input = Delta II).
  - Fundamental frequency = 141 Hz.
  - 95% response peaks < 0.54 mm.
- Support Grid
  - *Analysis with edge support only* (conservative).
  - Stresses ~ 7 ksi (aluminum yields @ 40 to 60 ksi).
  - Fundamental frequency = 80 Hz.
  - Static center deflection < 1.2 mm @ 10g.

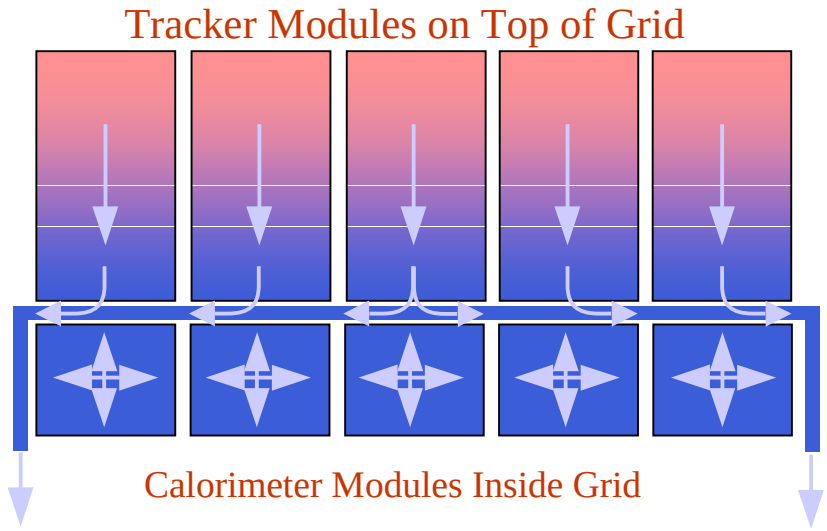




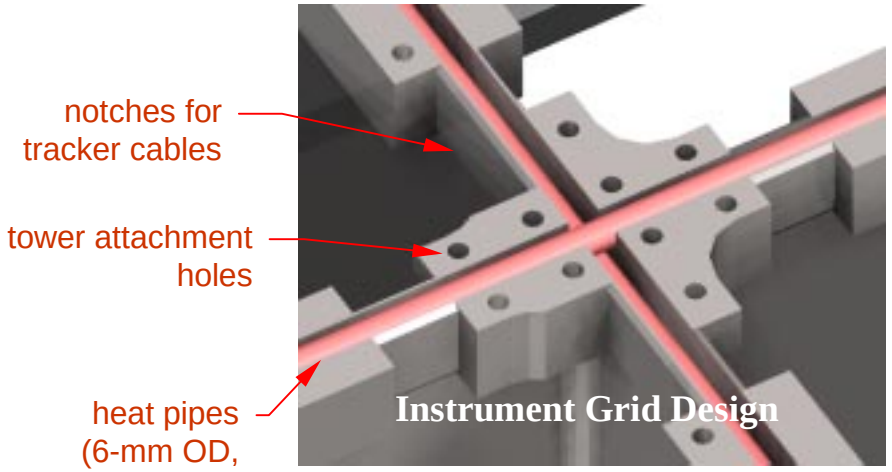


Instrument Thermal Engineering

- Thermal Requirements/Goals
  - Maintain end-of-life maximum silicon detector temperature < 20°C.
  - Maintain minimum CsI temperature > 0°C.
  - Minimize orbital temperature swings.
  - Minimize effect of orientation switch.
- Lockheed On-Orbit Thermal Analysis (Full Sun) to study radiator area needed.
  - One kilowatt, one meter high radiator (not in field of view).
  - Steady state (*i.e.* worse case), aircraft viewing mode.
  - 80% packing factor, absorptance = 0.10.
  - Temperature range: -14°C to +15°C.
- Internal Instrument Temperature Drops
  - Tracker electronics to wall: < 1°C.
  - Top to bottom of tracker wall: < 5°C.
  - Grid center to radiator: 3°C.
  - *Passive design meets our requirements.*



Heat pipes used to make grid ≈ isothermal.



Trades: Instrument Power and Mass

We are studying an alternative to the baseline design that would increase the weight and power margins and provide more room between the towers and the rocket shroud:

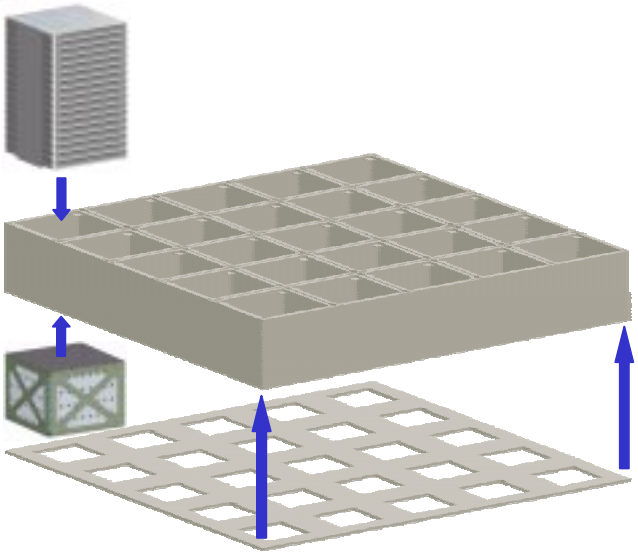
- 16 larger towers, slightly larger Si pitch (209 μm), to reduce the tracker channel count (by 28% for 16 *x*,*y* planes).
- Approximately 10% less geometric area, to reduce calorimeter weight and fit better into the shroud.
- Maintain 10 r.l. calorimeter for energy reach.

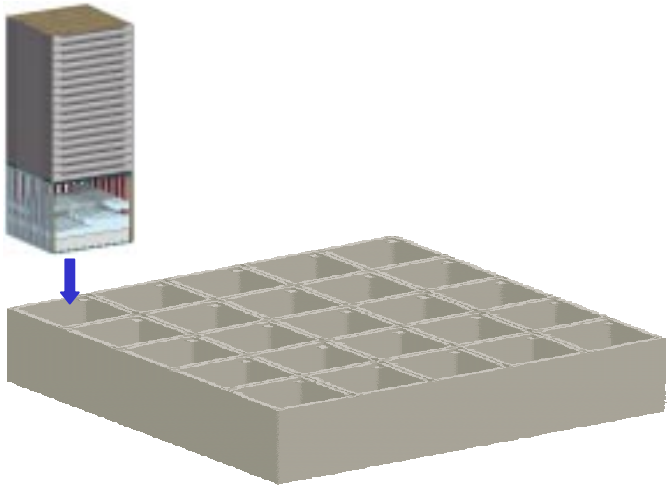
Key issue: can we still achieve our required low noise occupancy with the silicon-strip length increased from 32 cm to 38 cm?

Measurements made on existing prototype chips and detectors strongly indicate that there is sufficient remaining noise margin, even after including end-of-life radiation damage. (See the section on tracker electronics.)

16-tower array	Nominal	Contingency
Instrument Mass (kg)	2677	34%
Instrument Power (Watts)	466	39%

Trade Study of Calorimeter Mounting





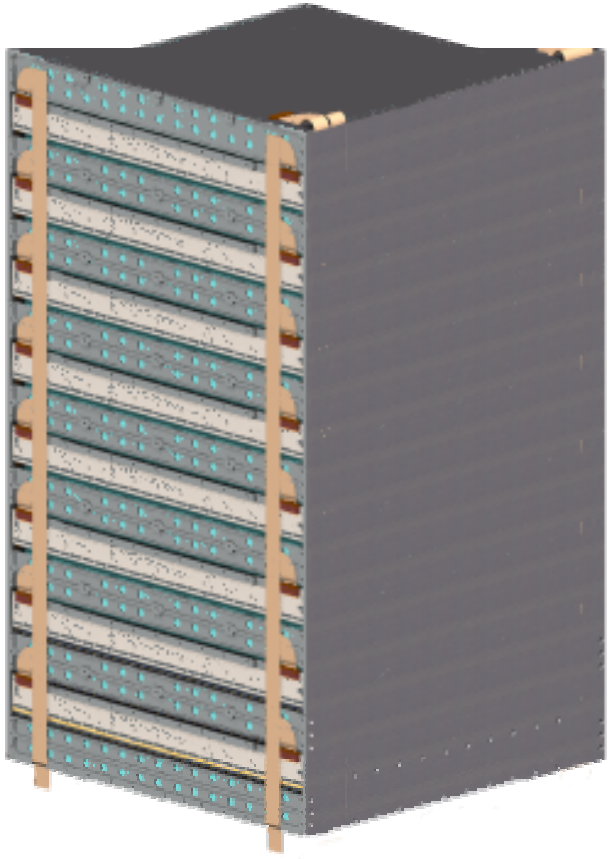
Calorimeter Inside Grid

+ Direct heat transfer from tracker into grid
+ More compact instrument
+ Tracker alignment based on grid features
+ Calorimeter / tracker are independent units
• Must remove calorimeter to remove tracker
– More structural material around calorimeter
• Each calorimeter held in place individually, back plate required for stiffness
– More constraints on grid thermal design

Calorimeter Above Grid

• Heat transfer into grid must bypass calorimeters
– Taller instrument
– Calorimeter dimensional stability critical
• Calorimeter / tracker is one assembly
• Must remove tracker to remove calorimeter
+ Less structural material around calorimeter

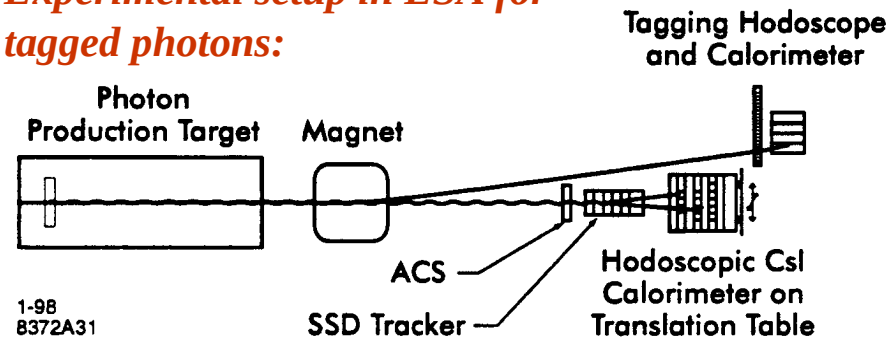
Silicon-Strip Tracker Technology Development

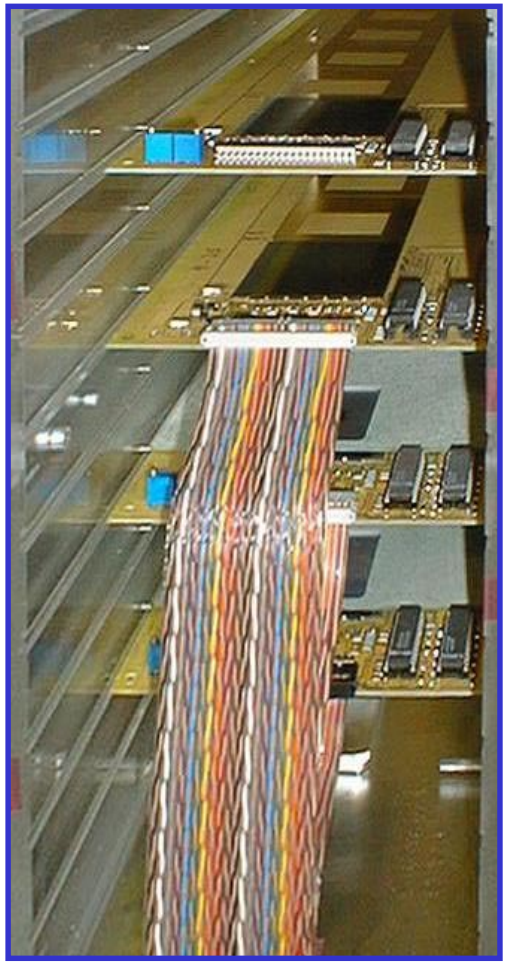


- Tracker Beam Test Results
- Tracker Mechanical Design and Engineering
- Silicon-Strip Detectors
- Tracker Electronics
- Quality Control
- Status of the Tracker for the Prototype Tower
- Trade Studies

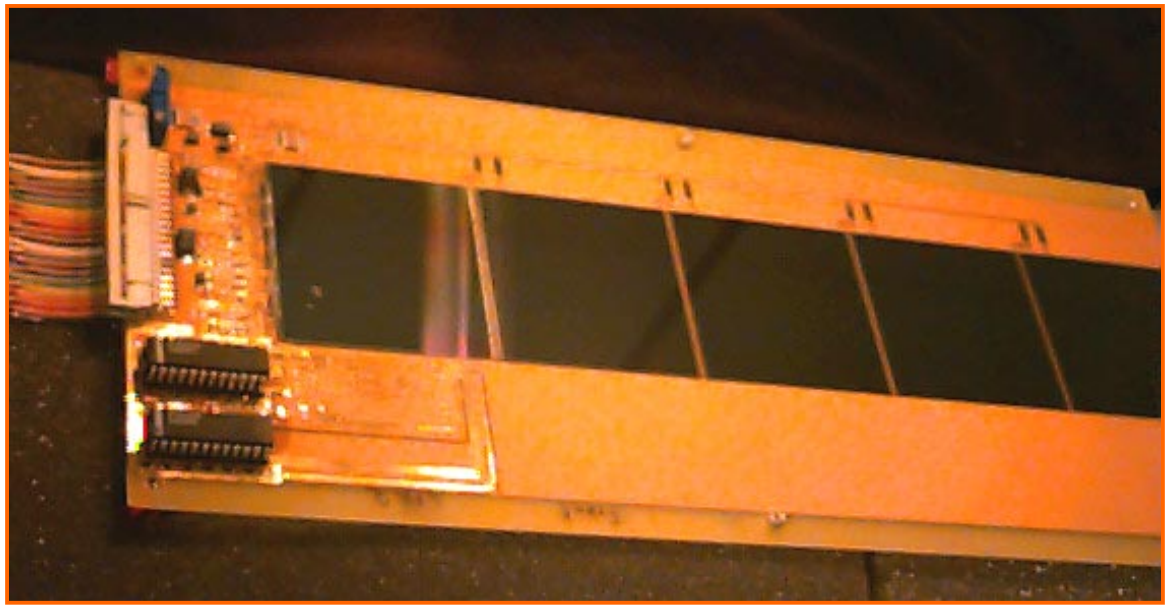
1997 Beam Test at SLAC

Experimental setup in ESA for tagged photons:





The top side of one beam test tracker card, with 5 detectors.

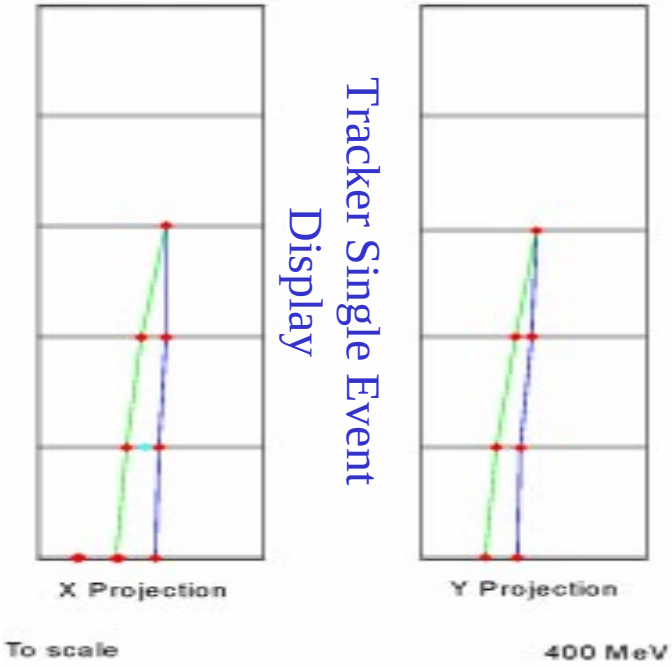


The '97 beam test tracker enclosure with 4 of 6 x,y cards, in the "stretch" configuration.

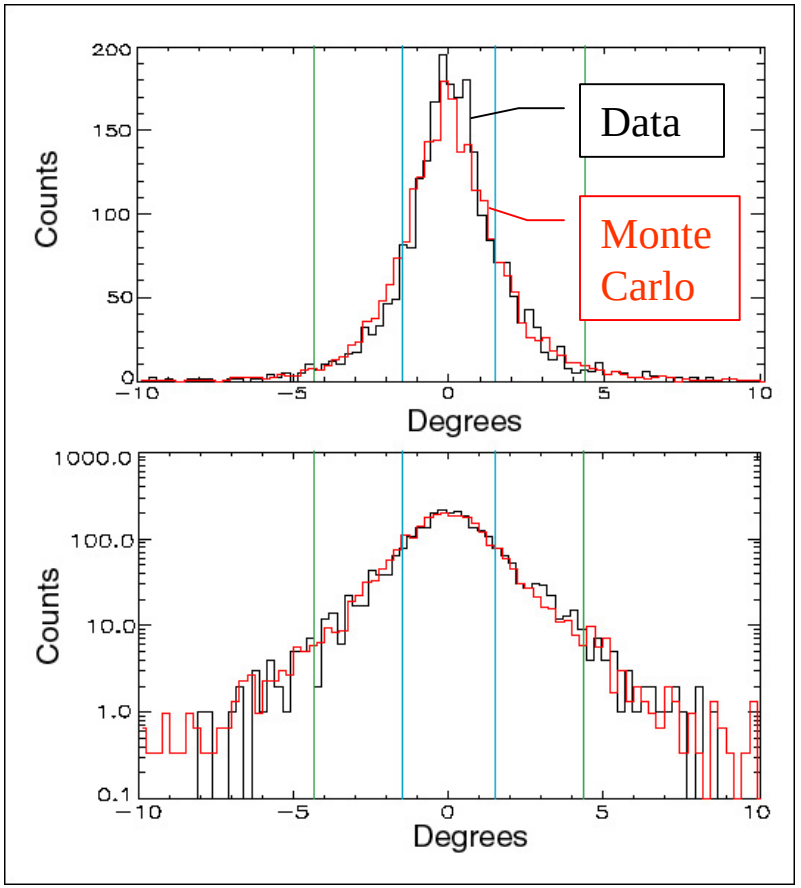
1997 Beam Test at SLAC

The beam test conclusively demonstrated the ability of our Monte Carlo to simulate the instrument performance far out into the tails of the distribution.

3-cm spacing, 400 MeV photon



X Projected Angle
3-cm spacing, 4% foils, 100-200 MeV

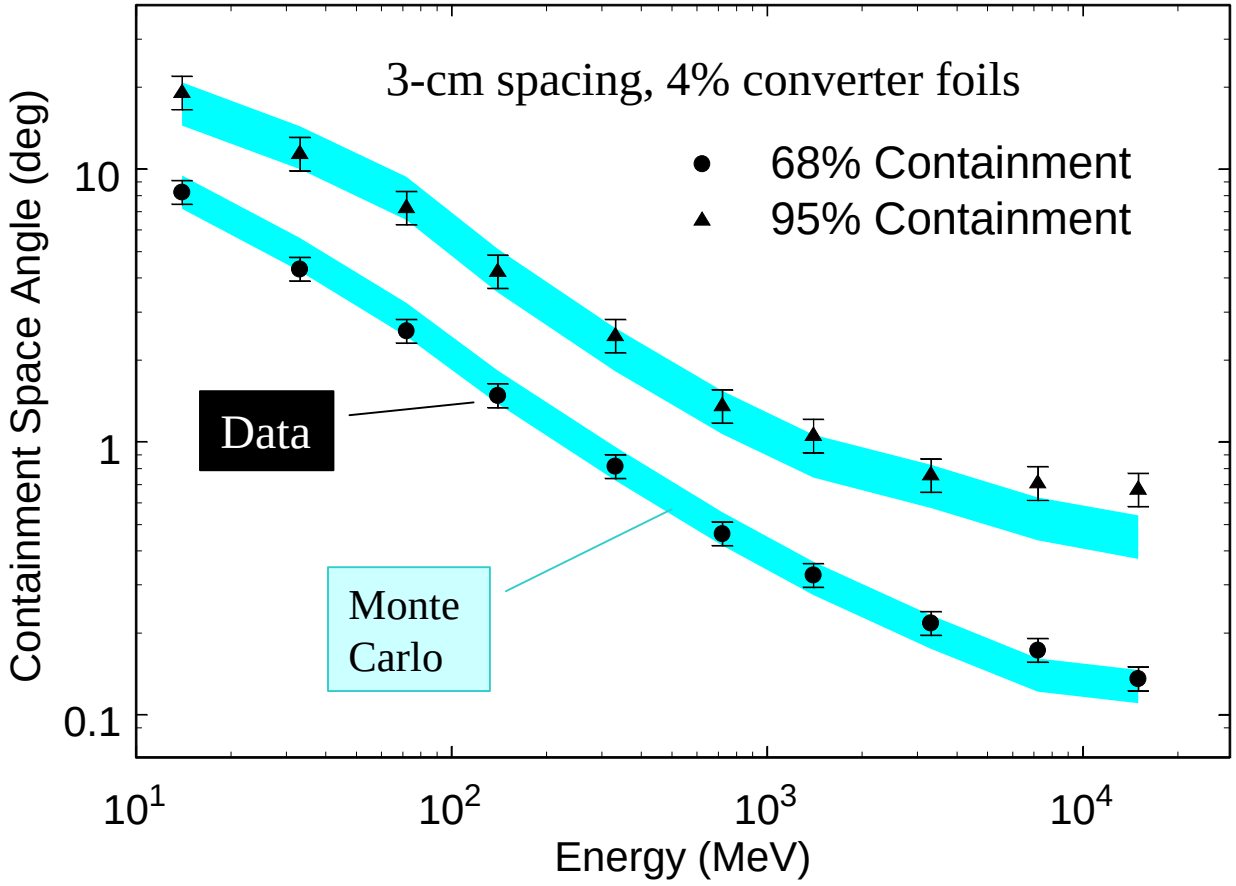


"Pancake" (3-cm spaced) configuration.

1997 Beam Test at SLAC

Excellent agreement of data with MC simulation.

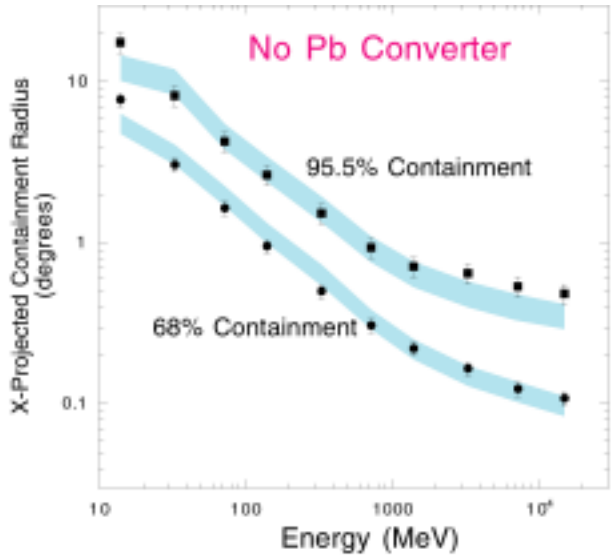
Tagged Photons

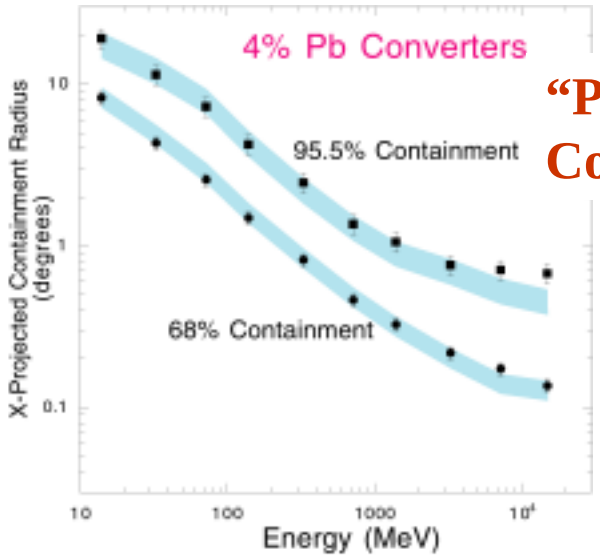


(Note that the performance shown here differs from that of the full-scale GLAST, especially at low energy, due to the small aperture of the beam-test tracker.)

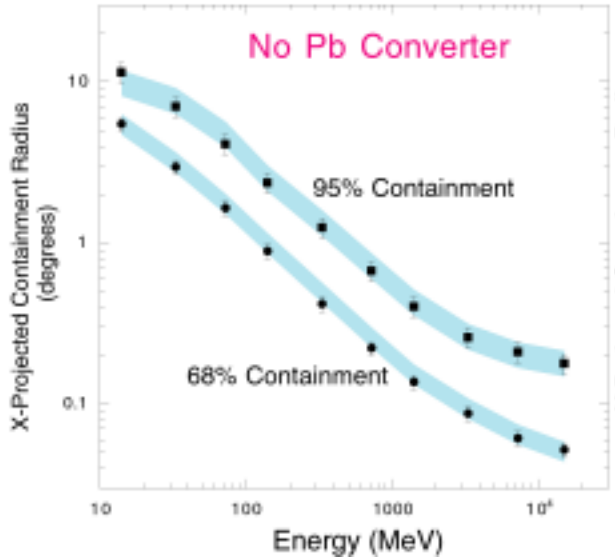
1997 Beam Test at SLAC

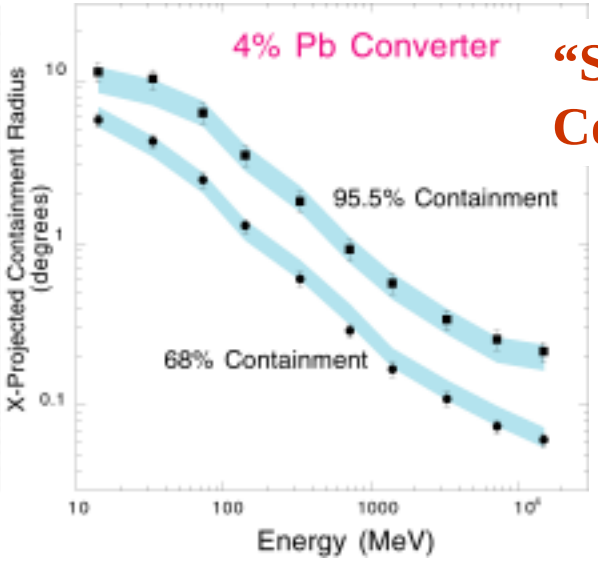
The good agreement between simulation and data held for all tracker configurations tested.





"Pancake" Configuration





"Stretch" Configuration

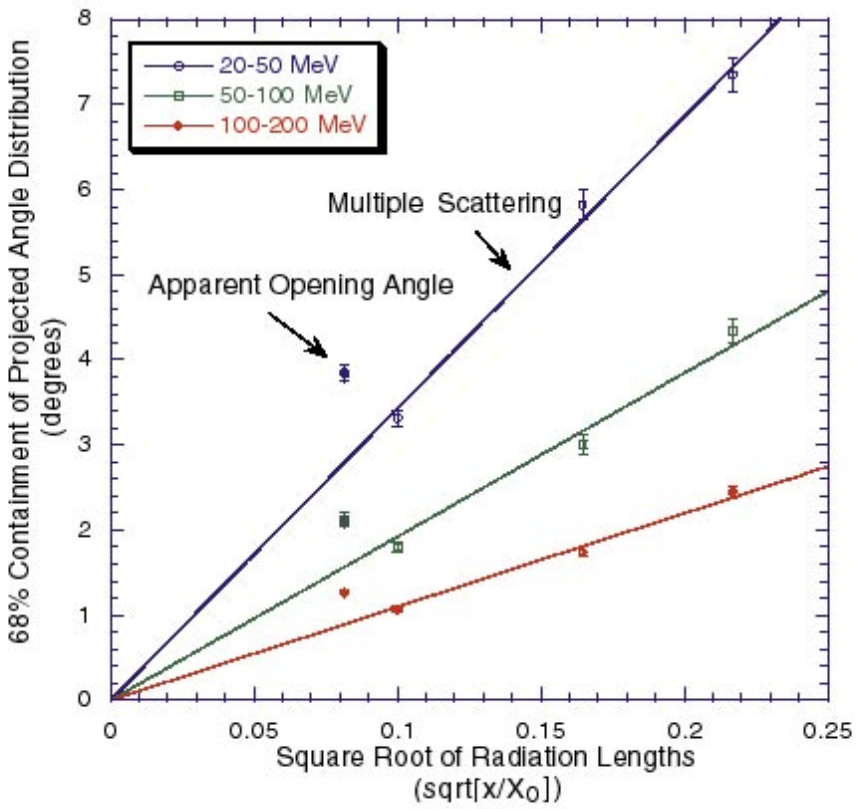
GLAST

1997 Beam Test at SLAC

Measuring the Gamma-Conversion Opening Angle

- Monte-Carlo simulations have shown that Silicon-Strip GLAST will have some statistical sensitivity to photon polarization from the brighter pulsars.
- A prerequisite is to have sensitivity to the electron-positron opening angle, which tends to be masked by multiple scattering.
- Beam test data clearly show the effect of the opening angle (with no Pb foils).

Comparison of measured gamma half-opening angles with measured electron scattering angles.



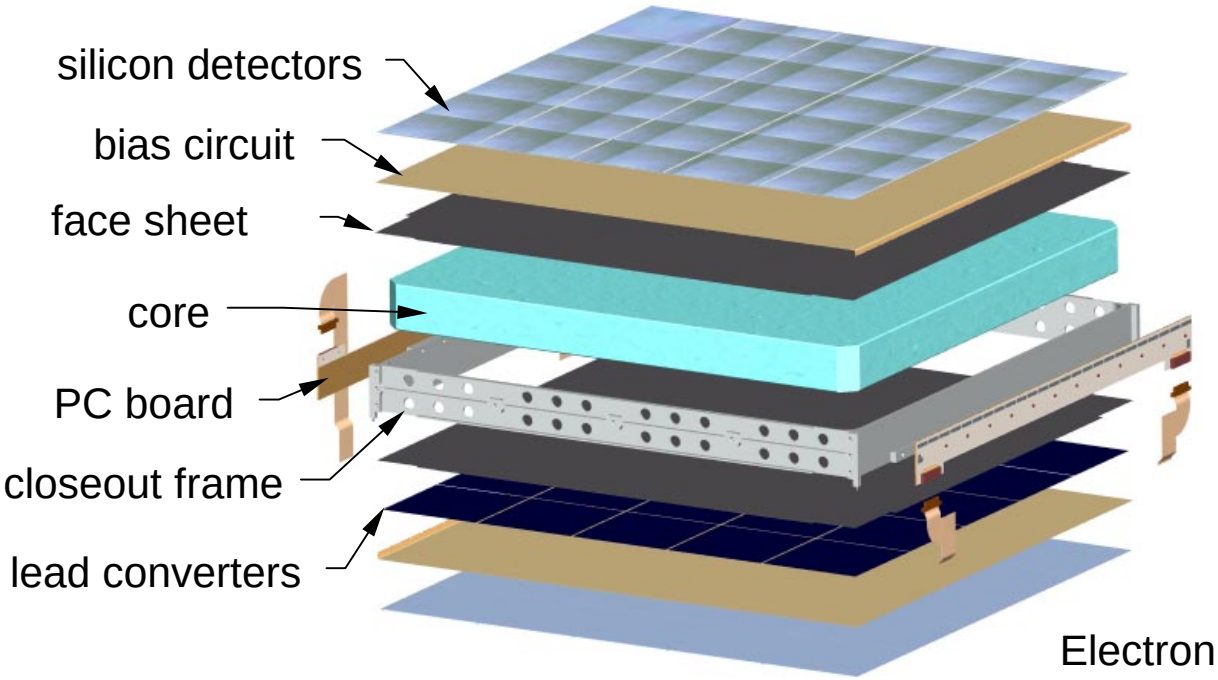
Tracker Mechanical Design

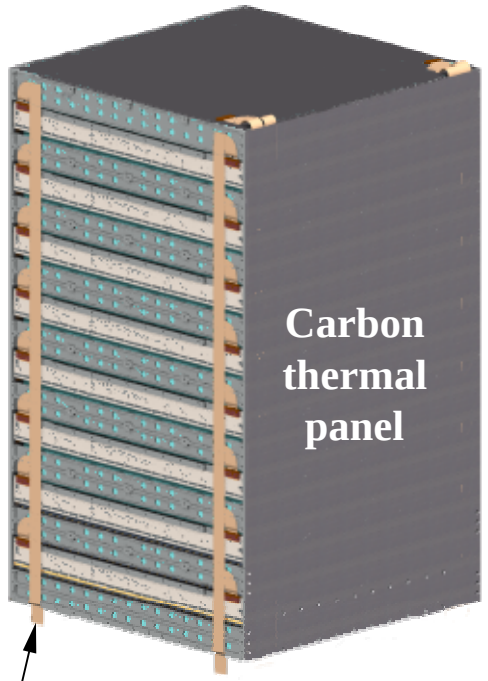
- Thick, lightweight composite trays provide a rigid, stable structure on which to mount silicon-strip detectors.
- Materials are chosen to minimize multiple scattering (carbon, or possibly beryllium).
- Stacked-tray concept combines simplicity with good alignment and a stable pre-stressed structure.
- Hytec Inc. has done a detailed engineering design and analysis of the tracker tower, including construction and testing of a 10-tray prototype.
- The detailed design is currently being implemented (in aluminum) in the tracker of the prototype tower.

Tracker Mechanical Design

Stacked Trays Concept

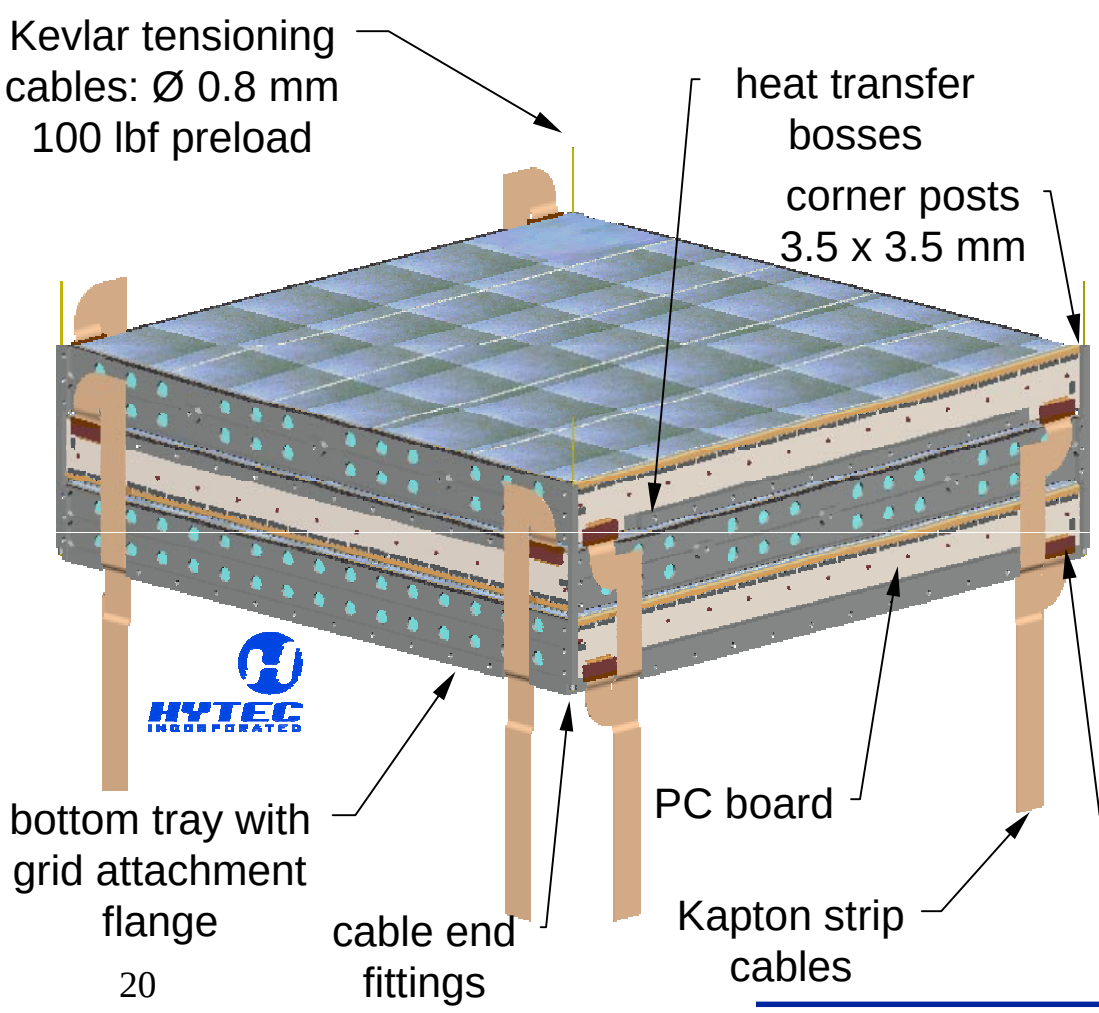
- Trays are lightweight sandwich with close-out frame.
- Trays are stacked on top of each other, aligned on corner posts.
- Stack is held together with Kevlar cables running through corners.
- Carbon composite side panels provide thermal pathways and significantly stiffen the tower.



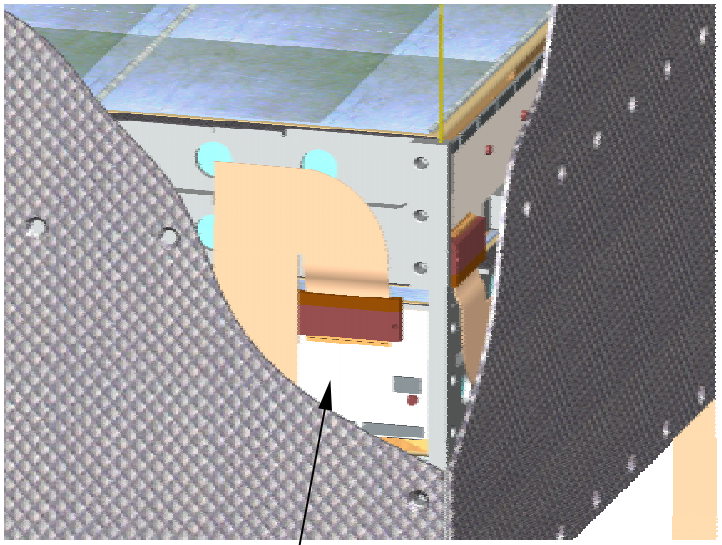


Tracker Mechanical Design

Tracker Tower: Lower 3 Trays

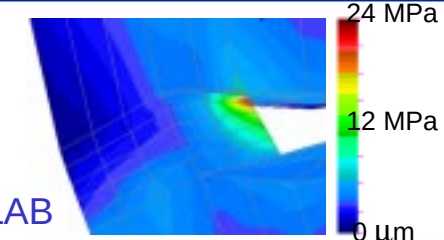


Corner Detail with Side Walls



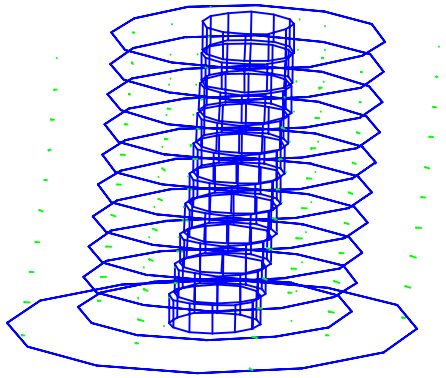
Testing the Tracker Mechanical Design

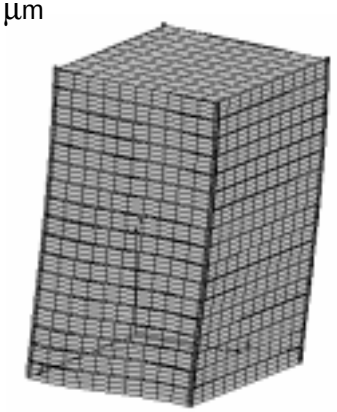
- Dynamic Analysis.
- Thermal Analysis.
  - calculation of temperature gradiant: < 5°C from top to bottom with 1-mm carbon walls.
  - Contact resistance between tray and wall: thermal-vacuum measurements at Stanford show negligible temperature drop: <0.2°.
- Prototype Tower (Hytec SBIR).
  - 10 trays, stacked, with Kevlar tensioning cables, very close to GLAST prototype tower design.
  - Vibration testing with and without side walls.
  - Results compare very well with the dynamic analyses.
  - Meets Delta-II launch requirements.



Detailed Local and Global FEM models

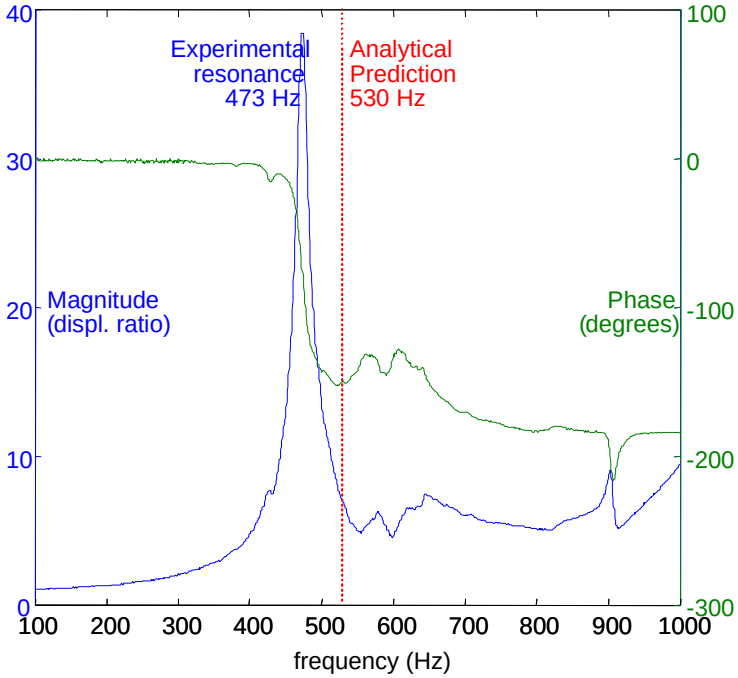
Global MATLAB dynamic models



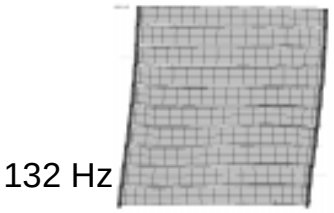


Hytec Stacked Tray SBIR

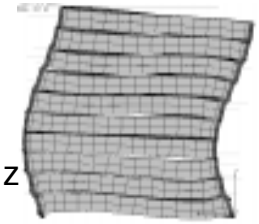
Measurements of the resonance frequencies of a single tray agree well with the numerical predictions (after measuring carefully the elastic properties of the core and face-sheet materials).



Frequencies and amplitudes calculated for the tower modes agree well with measurements.

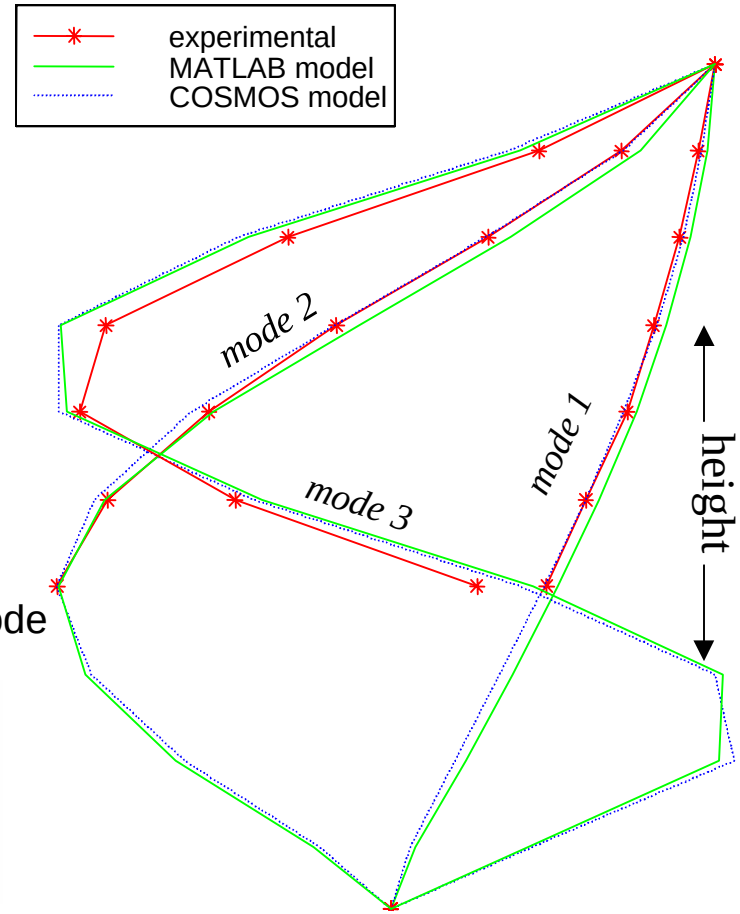


first shear mode



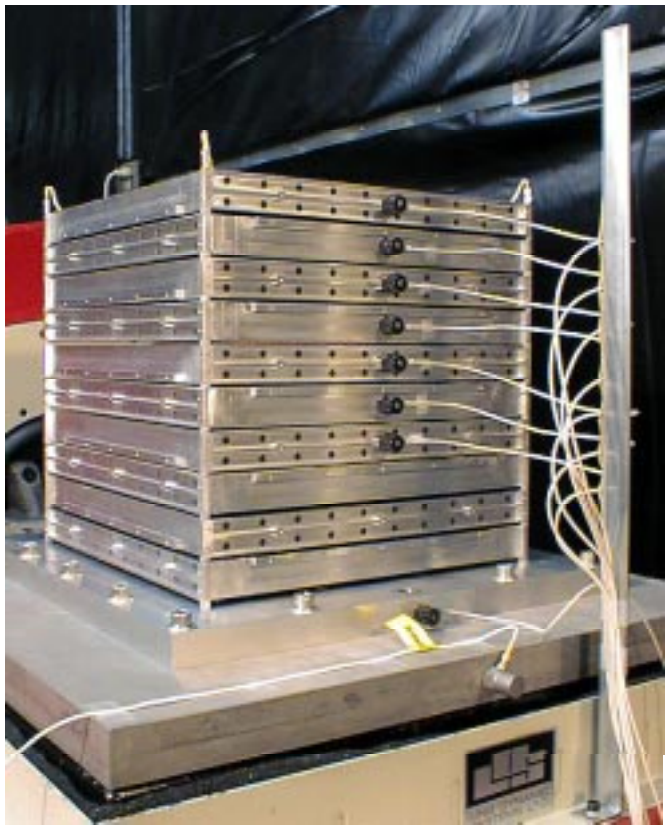
second shear mode

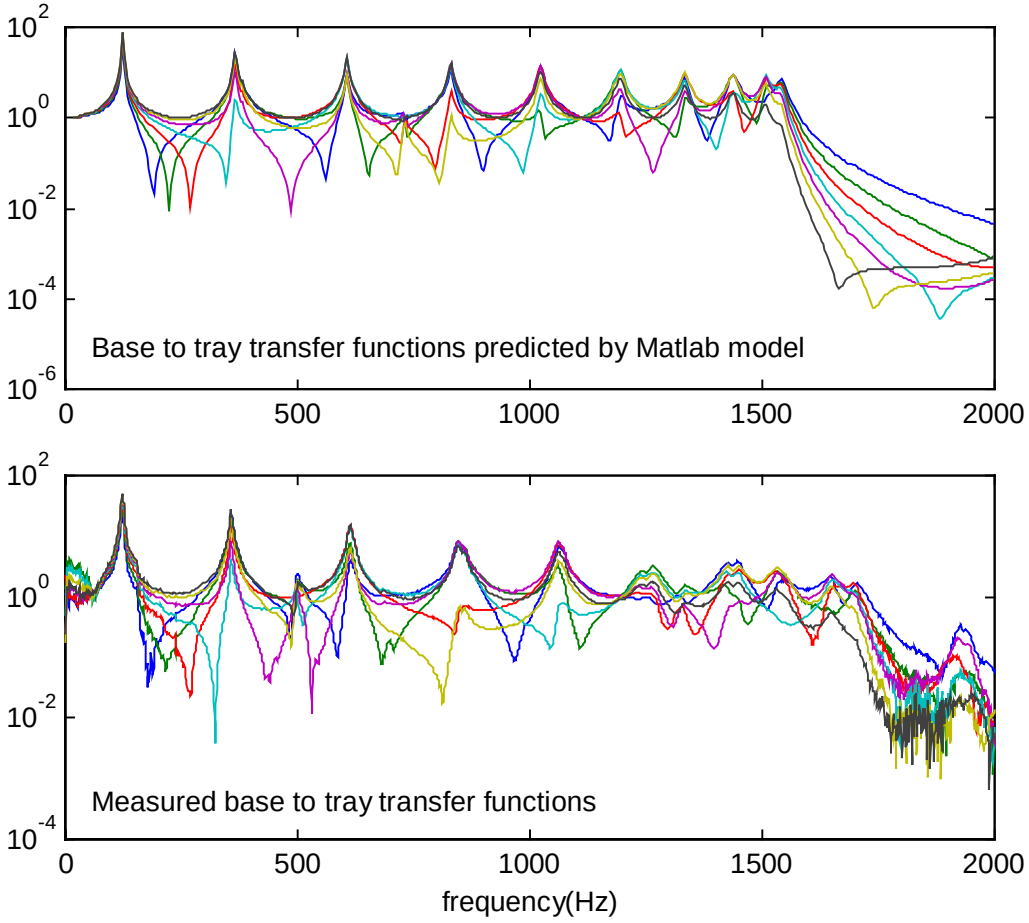
third shear mode



Hytec Stacked Tray SBIR

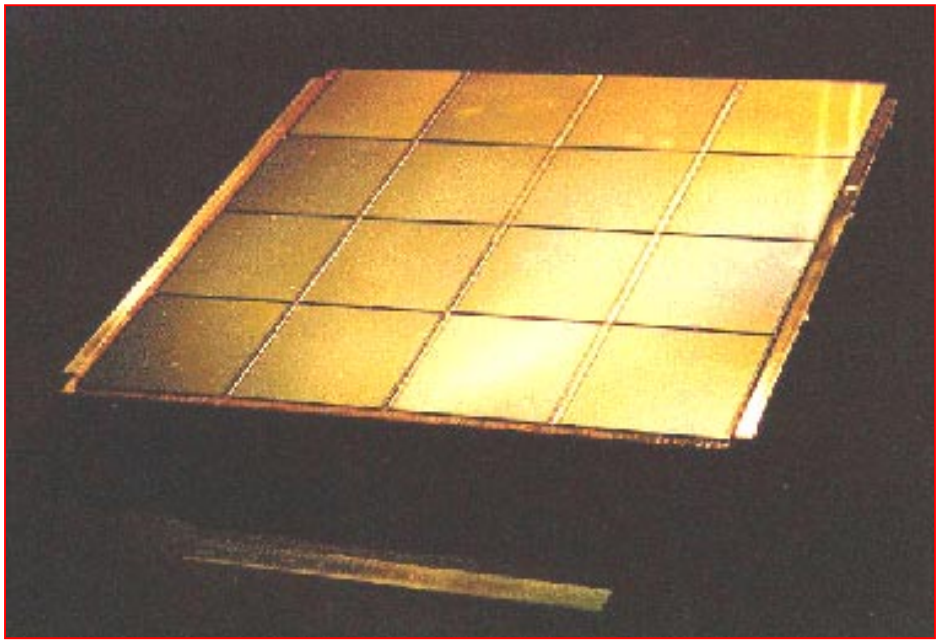
- Measurements of the tower dynamics agree well with the dynamic model.
- Side walls were measured to add a factor of 30 to the stiffness.
- This work assures us that we understand very well how to analyze our tracker design to assure a successful launch.





Environmental Testing of Trays

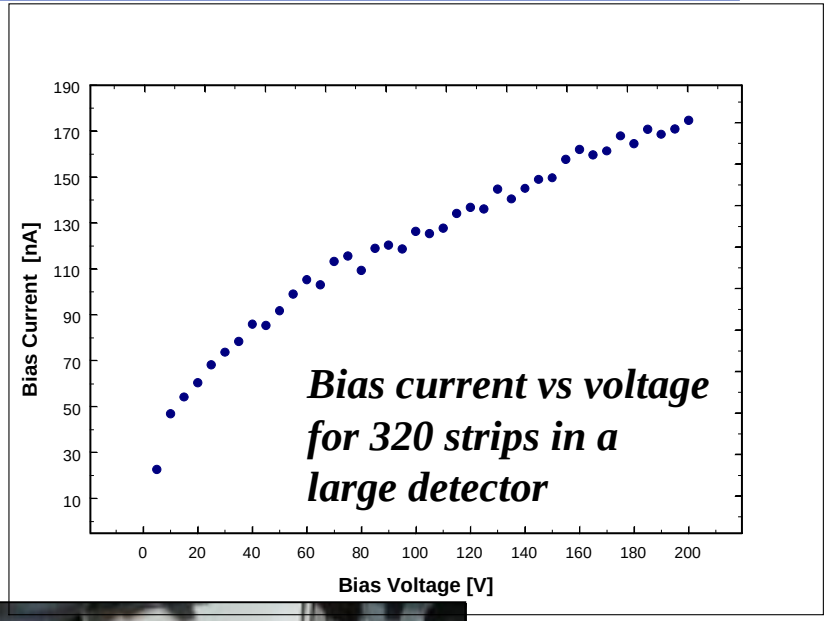
- Attention has already been paid to environmental testing of the detector/electronics assemblies as well.
  - Early 1-sided prototype tray built at SLAC/Stanford was vibration and thermal-vacuum tested.
    - ***None*** of more than 3000 wire bonds failed (no potting).
    - No failures of any sort even at the limits of the shake table—greatly exceeding the Delta-II requirements.
  - Preparations are under way to do vibration testing of a complete prototype-tower tray.
    - Detector ladders with potted wire bonds (the potting is done for protection during handling).
    - Live detectors and electronics.
    - Test robustness of our assembly.

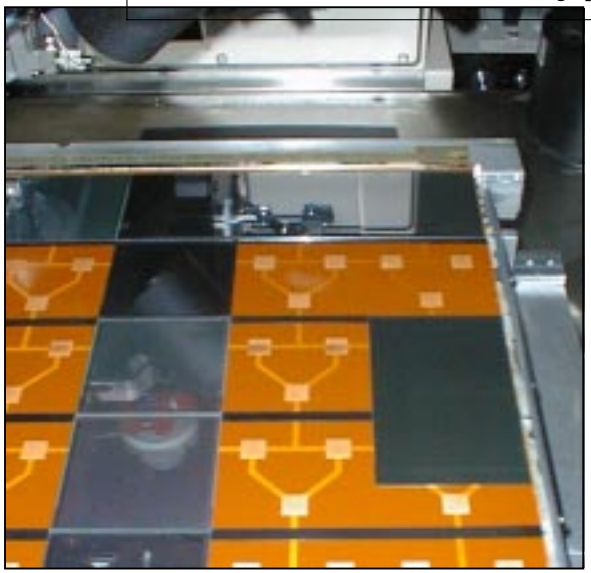


Prototype 4×4 tray for mechanical testing.
It was tested under vibration and thermal/vacuum at the Loral Corp.

Tracker Si Detector Development

- Prototype detectors functioned well in the beam test, but we have progressed to a design with polysilicon resistors for enhanced radiation hardness.
- 300 detectors have been produced from 4-in. wafers for the prototype tower. Quality is very high: only 0.02% bad strips and leakage current ~1 nA/strip. Exceeds specs.
- Techniques have been developed to build "ladders" of detectors (edge glued, wire bonded, potted) before mounting on trays.
- A few longer detectors have been made from 6-in. wafers. They look very good: 0.6 nA/strip! The remainder of the prototype tower will be instrumented with these.
- RFI's were sent to 12 manufacturers of SSD's. 7 have responded with expressions of interest. The procurement schedule for the mission is being intensively studied.





One large and several small detectors on a GLAST tray, mounted in the wire bonder.

Silicon-Strip Detector Specifications

Specs for detectors used in the prototype tower.

A 3rd page, not shown, specs the QC procedures.

GLAST SENSOR SPECIFICATION

1) Sensor Type: n-bulk, p-strip, single-sided, AC coupled readout

2) Substrate

option A= 4 inch wafer,
option B = 6 inch wafer

type:	n type
resistivity;	4-8 kΩcm
absolute thickness	400 +5, -15 um
uniformity of thickness:	+/- 5 um
local surface flatness:	+/- 1 um

3) Size

There are two options of silicon strip detector (option-A, option-B) to make a tower of 32 cm x 32 cm. A gap of 200 um is assumed between sensors to assemble a tower.

3-1) Outside Dimensions

	width x length x thickness	wafer size	Tray arrangement
Option-A:	64.0 mm x 64.0 mm x 0.4 mm	4 inch	5 x 5 sensors.
Option-B:	64.0 mm x 106.8 mm x 0.4 mm	6 inch	5 x 3 sensors

64.0 x 5+0.2*4(gap) = 320.8, 106.8 x 3 + 0.200 x 2(gap) = 320.8 mm
(a diagonal length of the sensor = 124.5 mm in 6 inch =152.4mm)

3-2) Sensitive area of unit sensor

	width	length	pitch	No.of channels
Option A:	62..274mm	62.430mm	194 um	320
Option B:	62.274 mm	105,230 mm	194 um	320

3-3) Percentage of dead area on one tray
Option A: 5.6 %
Option B: 4.5 %

4) Detailed dimensions

Option-A:	number of strips:	320
	strip pitch:	194 um
	strip width implanted:	50 um
	strip length implanted:	62410 um
	Al readout strip width:	52 um
	length of Al readout strip:	61733 um
	edge dead area: strip end;	785 um
	side edge:	985 um
Option-B:	number of strips	320
	strip pitch;	194 um
	strip width implanted:	50 um
	strip length implanted:	10521 um
	Al readout strip width:	52 um
	length of Al readout strip:	104533 um
	edge dead area: strip end:	785 um
	side edge:	985 um

5) Technology

5-1) positioning accuracy of mask pattern: <+/- 1 um

5-2) Implanted strip
implant-ion density: >1 x 10**14
implant + diffusion depth: 1.0 +/- 0 3 um
any corner of the implant and Al electrode: radius > 10 um

5-3) Biasing resister: Poly-Si, implant-density: > 10**l4

5-4) Guard ring; one extra-guard ring with the extendcd A1 electrode [1] outside of the bias ring, with the gap of 40 um from the bias ring (to improve the breakdown voltage).

5-5) Bias ring: Bias ring consists of Al electrode (extended electrode structure) and an p-implant underneath the Al electrode to collect leakage current from the edges.

5-6) N-side (ohmic contact side) n+ implantation. technology selection is left to the manufacturer to minimize the leakcage current.

6) Electrical properties

6-1) Full depletion voltage:	70V - 125V
6-2) Leakage current (at 125V and 25°C);	< 50 nA/cm**2
dI/dV/cm**2 at 125V:	< 0.2 nA/V/cm**2
6-3) Resistance of biasing resistors: (variation sensor to sensor)	30 - 80 MOhm
maximum vanation in one sensor:	< +/- 10 %
6-4) Breakdown voltage of Juncton:	
Catastrophic breakdown at 25° C:	> 200 V
on-set of micro-discharge [2]:	> 165V
6-5) Breakdown voltage of coupling capacitor:	> 100 V
6-6) Capacitance of coupling capacitor:	> 40 pF/cm
6-7) Resistace of Al electrode on the strip:	< 5 Ohm / cm
6-8) Isolation between adjacent strips:	> 30 MOhm

7) Maximum tolerable number of bad strips: <1%
(No. of bad channels =
Shorted capacitors + bad isolation
+ disconnection of Al electrode)

Tracker Electronics Development

An early emphasis of our technology development program was to ***demonstrate*** that silicon-strip readout electronics could be developed to meet the GLAST requirements, especially:

- Low power: 200 μW/channel.
- Low noise: occupancy < 1×10^{-4} per channel per trigger.
- Low dead time (1% at 1 kHz): 20 MHz readout and deep buffering.
- Redundancy: immune to single-point failures.
- Compact: minimize dead space between towers and minimize the cabling within a tower.
- Reliable: QC during assembly, encapsulation, radiation hardness, latchup immunity.

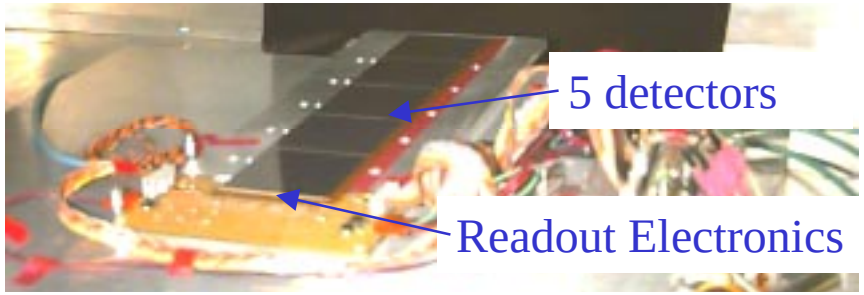
1996: 16-channel amplifier-discriminator ASIC achieves noise goal with 140 μW/ch.

1997: Improved 32-channel version operates successfully in the beam test (total 2300 channels).

1998: 64-channel version with full digital functionality demonstrated with complete detector ladder (320 channels).

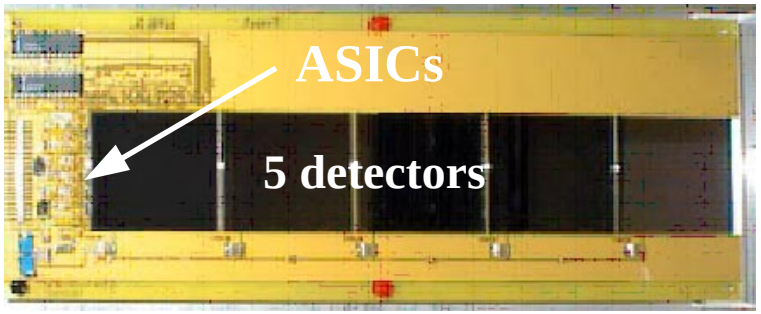
1998: Readout controller ASIC prototyped and successfully tested.

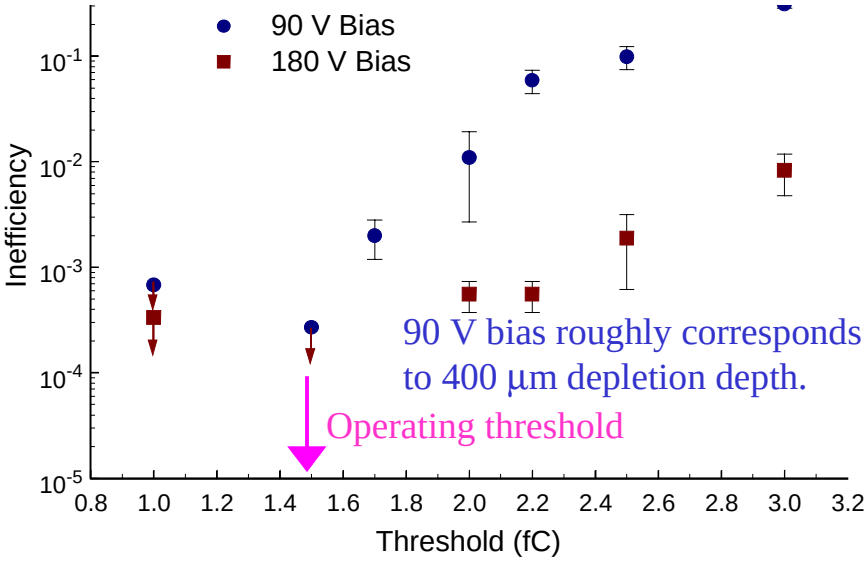
1999: Complete tray readout section completed and tested (1600 ch.)



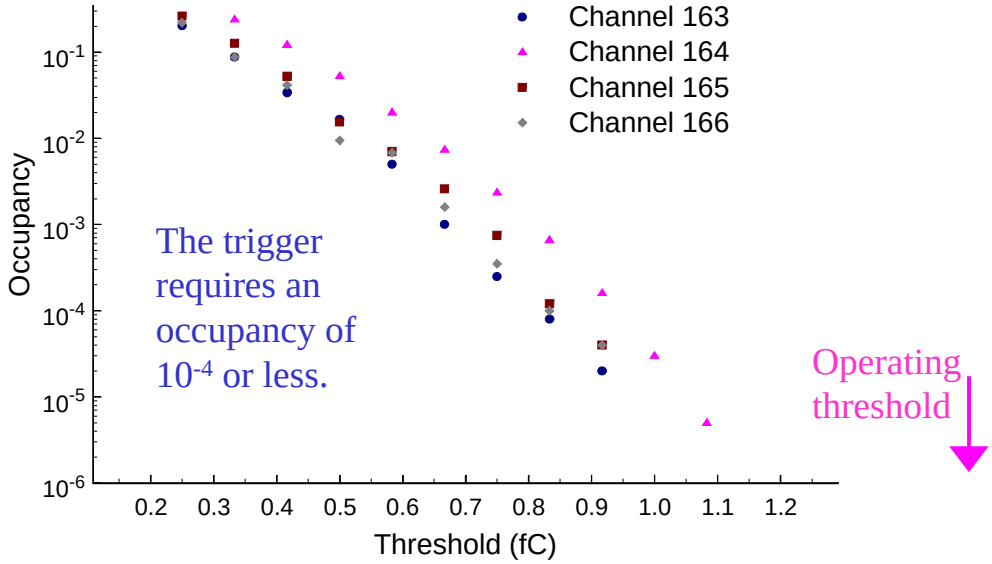
Tracker Readout Performance

- Tracker electronics performance measured with a 30-cm long detector ladder (1997 beam test).
- The noise requirements are satisfied with a threshold that gives 100% efficiency.
- Only 140 µW/ch consumed (digital readout not included here).





Inefficiency for detection of *minimum ionizing electrons* at normal incidence in a single detector plane. ***The nominal threshold used is 1.5 fC.***

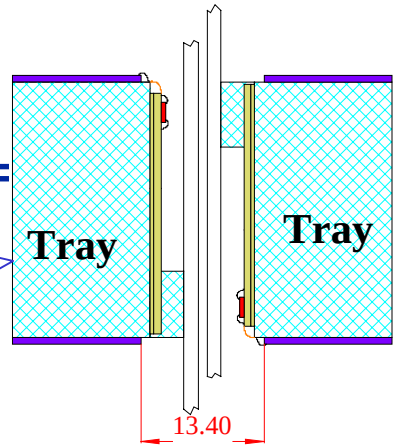


Noise occupancy, in a 1 µs window, versus threshold for four different channels connected to 30 cm long detector strips.

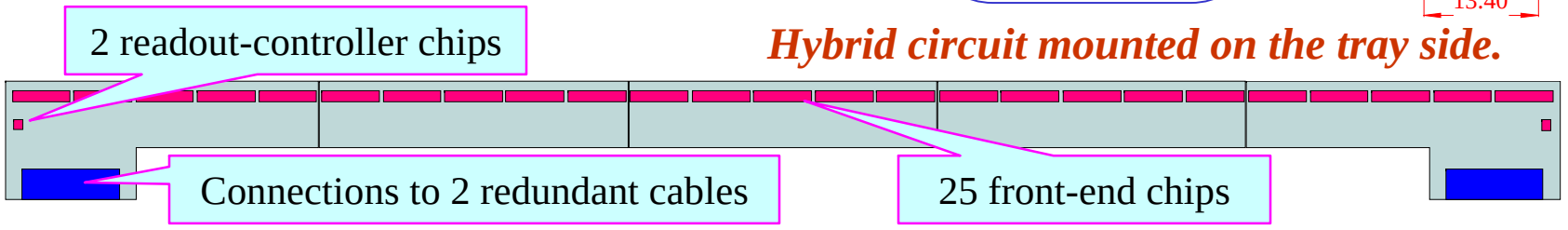
Tracker Readout Electronics

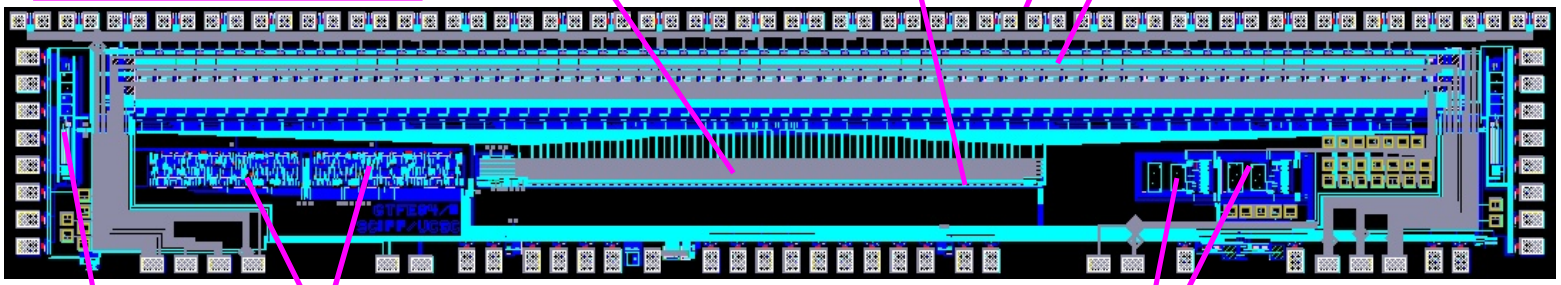
- A complete readout section satisfying the GLAST power, noise, speed, redundancy, and dimensional requirements has been designed and prototyped.
- The design includes two different ASICs.

Dead gap between towers only ~1.3 cm



Hybrid circuit mounted on the tray side.





Measured total system power: 209 µW/ch at conservative 12.5 kHz trig.

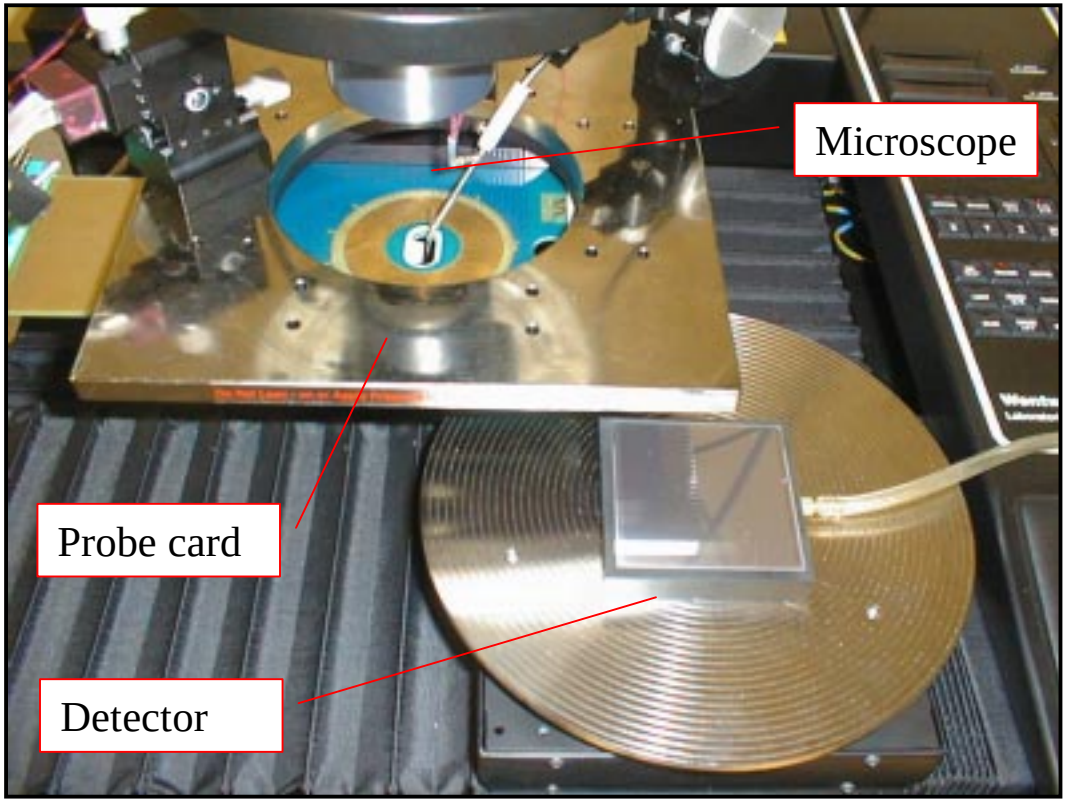
Layout of the 64-channel front-end readout chip.

Tracker Quality Control

To build a mega-channel solid-state detector requires serious attention paid to quality control during assembly in order to have ~99% working channels.

- Test all VLSI chips before and after mounting on hybrids.
- Test and burn in assembled readout sections before mounting on trays.
- Test all detectors before assembling ladders, before mounting on trays, and after wire bonding.
- Careful environmental control during assembly.
- Automated measurement of detector placement accuracy.

All of these procedures are very close to being in place on the small scale of the prototype tower assembly.



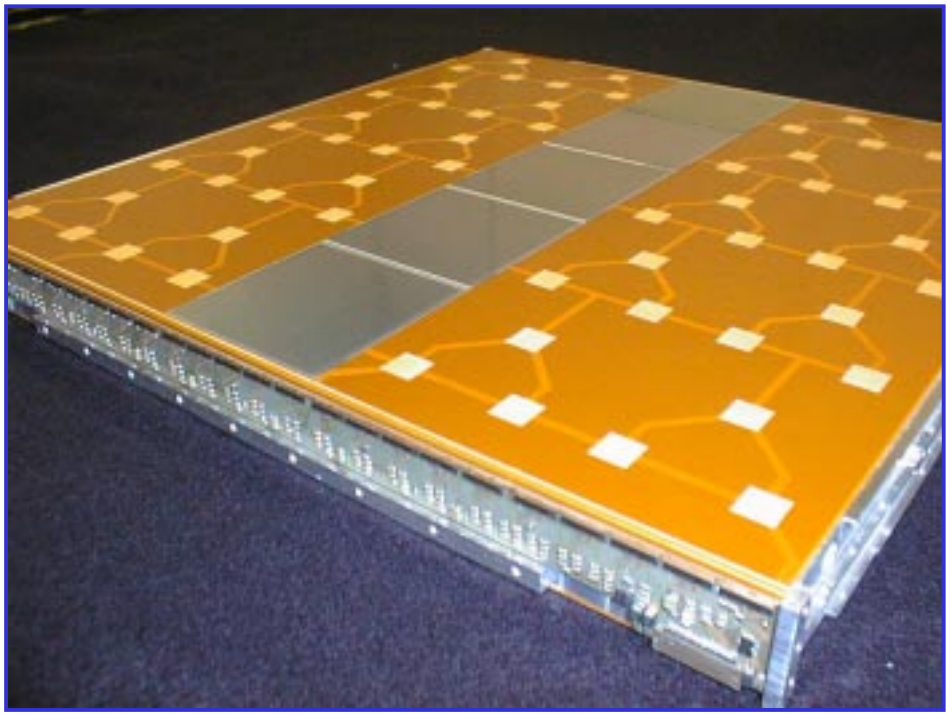
An automated probe station, used for testing of all ASIC's and Silicon-Strip Detectors before assembly.

Prototype Tower and 1999 Beam Test

- Engineering & Science Tests of All Four *Integrated* Subsystems:
  - ACD (scintillator on 5 sides).
  - Tracker (17 trays).
  - Calorimeter (Hytec compression cell fully instrumented with CsI).
  - Data Acquisition.
- Principle Tracker Beam Test Goals
  - Further validate the instrument performance, with electrons and photons incident at all angles.
  - Test the performance of the electronics and DAQ designs.
  - Test of trigger and readout systems, with all instruments working together (possible EMI).
- Some Goals of the Engineering Prototype Tracker Tower
  - Full size, with all 17 trays, as a test of the mechanical/thermal design.
  - All 51,200 electronics channels, to fully test the readout system & DAQ.
  - Meet all power, speed, dead time, noise, miniaturization, and QC specs needed for the flight instrument.
  - Vibration testing of complete trays.
- Some Limitations
  - Only about 2/3 of the live silicon-strip detectors will be installed, for reasons of cost.
  - Aluminum closeouts are used in place of the carbon composite structures that we want to develop.
  - Not all procedures, materials, and parts have yet been space qualified.

Prototype Tower Tracker Status

- Complete tracker electronics chain—front-end ASICs, data transmission, DAQ —has been prototyped and tested.
- All readout controller chips are in hand. Front-end chip order will go out Feb. 1, 1999.
- Assembly methods are mostly worked out. Placement of detectors in “ladders” verified to be better than 25 microns accuracy.
- Two complete trays have been fabricated, one with a completely functional readout section mounted. Ordering of production parts is in progress.
- About half of the Si detectors are in hand, with the rest ordered (from 6-in wafers).
- On schedule for completion in August, 1999.



Photograph of a tracker “tray”, with a complete readout section mounted on the side, with 1600 amplifier channels. One 32-cm “ladder” of Si-strip detectors is mounted on the top surface.

Tracker Trade Studies

- Tracker configuration
  - # towers—much recent work in evaluating 25 towers versus 16 larger ones.
  - # tracker planes—power budget versus performance.
  - Optimization of the SSD size, thickness, pitch. 4-in wafers vs. 6-in wafers.
  - Graded radiators—work in progress to access various options.
- Detector technology:
  - Single-sided vs. double sided.
  - DC-coupled vs. AC coupled.
  - Punchthrough vs. polysilicon resistors for biasing.
- Mechanical.
  - Side wall mounting vs. corner posts.
  - Converter material, thermal conductor material, tray core material, closeout material.
  - Electronics on tray faces or sides.
- Readout electronics, triggering, data acquisition.
  - Pulse-height information—per channel or per trigger plane.
  - Architecture: redundancy, cabling complexity, speed, buffering.
  - Data format: where is zero suppression done?
  - *Etc*.

Varying Converter Foil Thickness

- Optimization of the distribution of converter material in the tracker has been studied extensively in the past year.
- In general, the optimization is soft and the merits depend on the science topic. By redistributing the baseline radiator material, modest improvements can be made, depending somewhat on the point of view, but *the uniform distribution in the baseline design, in fact, balances well the low-energy performance with the high-energy performance.* (No impact on the engineering design in any case.)
- At the same time, studies of calorimeter modifications to enhance the angular resolution of calorimeter-only photons have been in progress for several years.
  - Gap between front and rear portions of the calorimeter.
  - Silicon-strip plane inside the calorimeter to pin down the start of the shower.

  The results indicate increased complexity with modest scientific gains.
- A more radical redistribution of the converter material in the tracker is currently being investigated and appears promising:
  - Thin the foils in most of the tracker, to improve the angular resolution for low-energy photons.
  - Make the last several layers with thick foils to give a large effective area for high-energy photons. (*To work well, this relies upon the excellent SSD measurement resolution and hit efficiency*.)

  Extensive simulation work is in progress to evaluate and test this concept.

Data Acquisition System Development

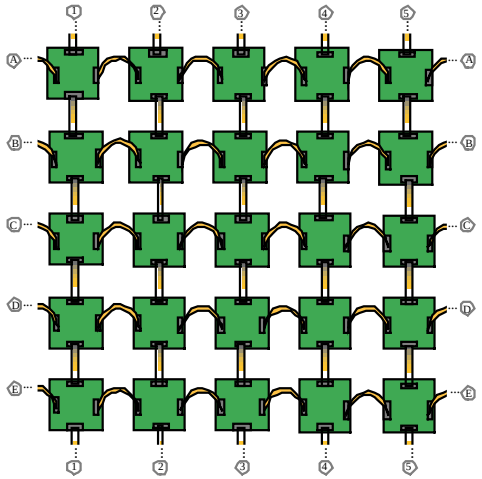
- DAQ System Design
- Status of the DAQ for the Prototype Tower
- DAQ Trade Studies

Data Acquisition Development

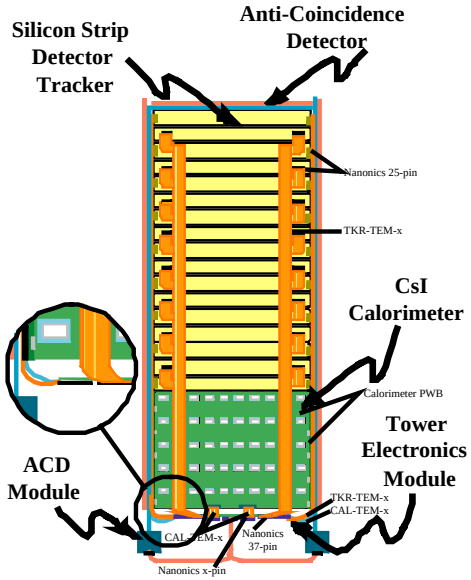
- Challenges:
  - High channel count.
  - High speed readout (min dead time; max event rate).
  - Onboard processing (minimize downlink requirement).
  - Low average power.
  - Space environment.

- A conceptual design is in hand which meets all the requirements without being unduly complex.
- Features:
  - 25 identical boards in a 4-way redundant network.
  - Parallel serial readouts with FIFO buffers.
  - Minimum of part types.
  - Low average power (< 140 W).

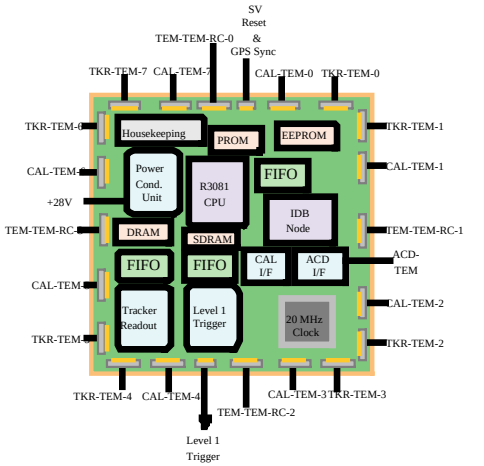
Level 1 Trigger and Instrument Data Bus Cable Diagram



Prototype Tower

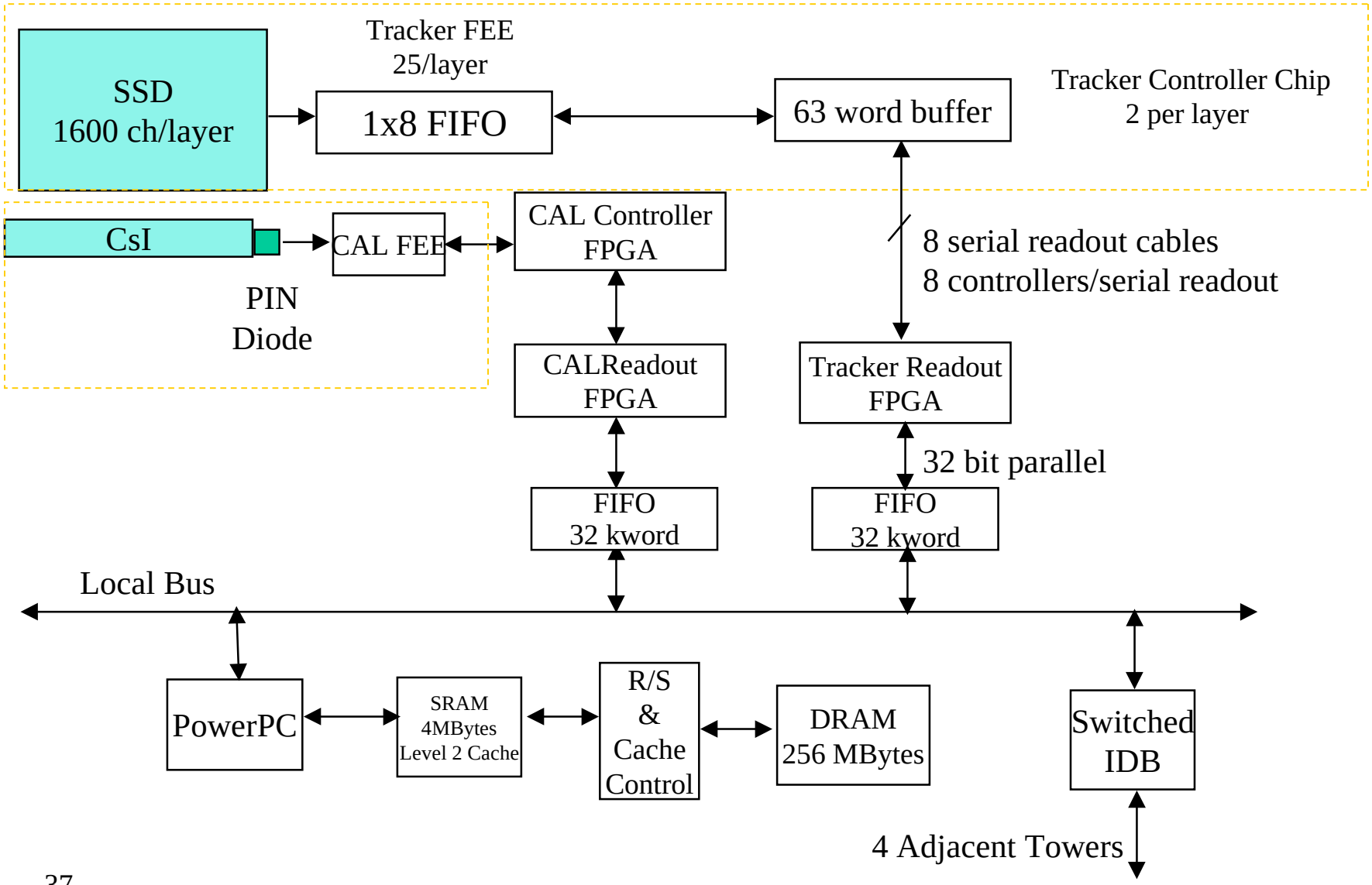


Tower Electronics Module Interface Block Diagram



GLAST

DAQ Data Flow Within a Tower



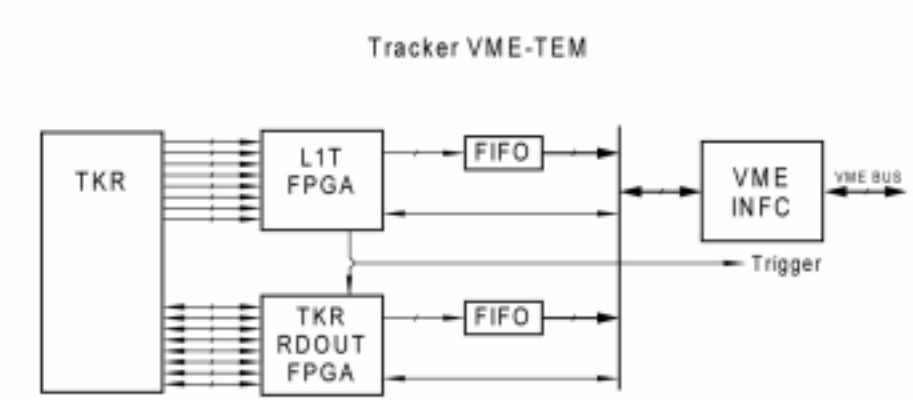
Data Acquisition Development

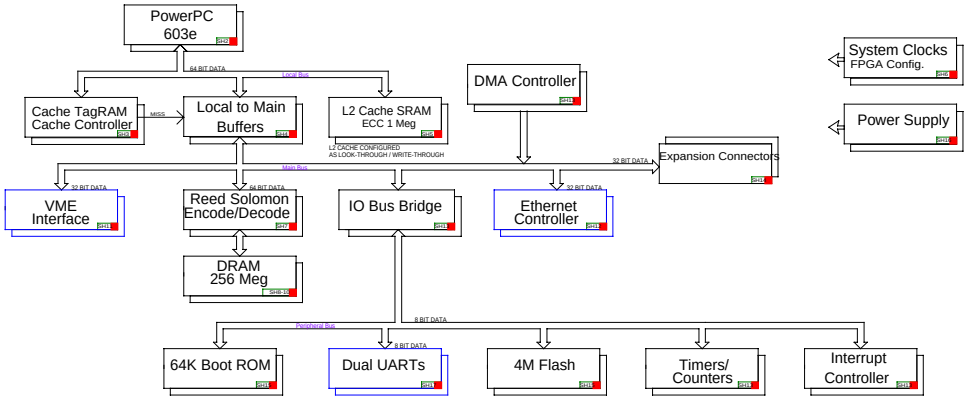
Staged development to minimize cost and schedule:

Design and prototype VME boards to support

- Level 1 Trigger.
- Readouts (Tkr, Cal, ACD, Housekeeping).
- CPU (COTS board).
- PowerPC design for power management.
- Onboard 100 Base T Ethernet for network.
- Backup for prototype tower integration/test.

The tracker readout/trigger VME board has been prototyped and has been successfully tested with two modules of the tracker front-end readout system.



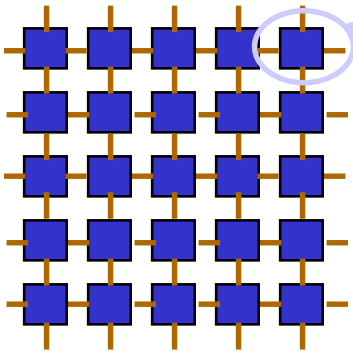


CPU Board Block Diagram

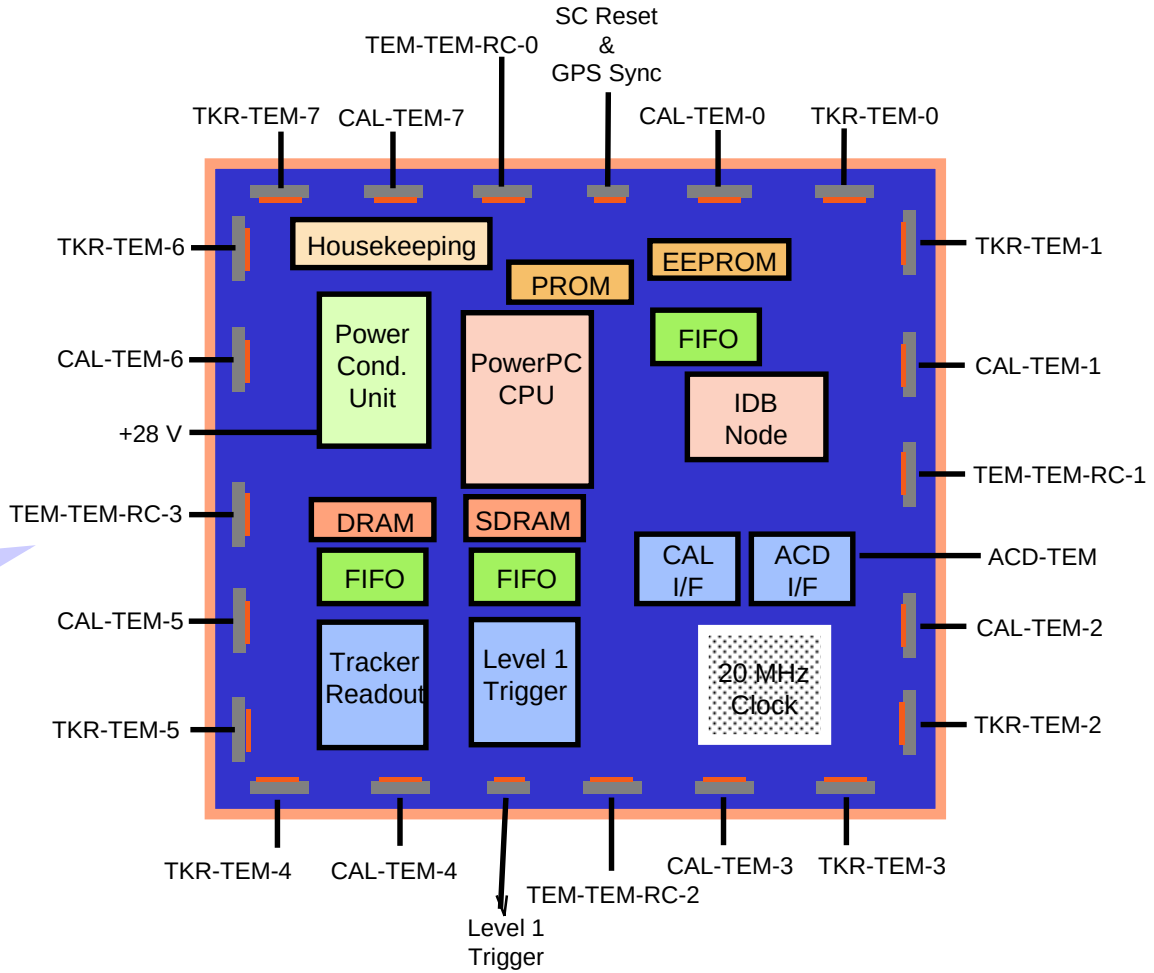
GLAST

Data Acquisition Development

- Tower Electronics Module (TEM)
  - Integrates separate subsystem components from VME.
  - First prototype board is simplified versions with essential functions.
    - 100 Base T Ethernet in place of 4-way switched network.
    - COTS power supplies.
    - Direct readout and control interfaces for CAL and ACD.
  - Swap out TEM board in future revisions.



Level 1 Trigger and Instrument Data Bus Cable Diagram



Tower Electronics Module Interface Block Diagram

GLAST

Prototype Tower DAQ Status

- Two FPGA/VME cards tested and working.
- TKR interface tested with F.E. electronics (FPGA board now at UCSC).
- Proposed CAL-TEM interface to CAL boards sent to NRL.
- IDB Trade Study draft available.
- DAQ Architecture Trade Study available.
- Tower CPU schematic completed at NRL.
  - 10 Base T Ethernet for VME board.
  - Extension connectors will be used on first TEM board for daughter cards: IDB, CAL-TEM I/F, ACD-TEM I/F, *etc*.
- Negotiations in progress with Wind River (real-time operating system).
  - Full licenses for NRL & SU.
  - GSFC & UCSC utilize licenses at NRL & SU via network for compiling new code.

Data Acquisition Trade Studies

Trade	Options	Advantages/Disadvantages
Onboard Data Storage	Distributed Memory vs SSR	Advantages: Memory required on tower boards in any case. Reduced cost, weight, and power. Increased flexibility in data management. Reliability through 25 tower redundancy. Disadvantages: Limits IDB bandwidth
Onboard Data Processing	Downlink average data rate vs onboard processing and power	Advantages: Reduce onboard processing requirement by increasing number of contacts per day in order to increase average downlink data rate. Disadvantages: More ground processing required. Higher contact rate. Less margin in onboard data storage.
System architecture	Instrument data bus vs central data acquisition controller	Advantages: Only one board type required. Very high level of reliability through 25 tower redundancy. Tower controllers required anyway. Instrument dead time not limited by data acquisition rate. Processing speed available is 25 times single processor Advantages(cont): Minimizes power required. Permits single tower checkout prior to calibration. Permits prototype demonstration without complete instrument build. Reduced cost. Reduced software and hardware complexity. Disadvantages: Increased node management.
Instrument data bus type	2D switched network vs FODB, Gigabit Ethernet, Fibre Channel, etc.	Advantages: Lower power. Lower point to point speed required with higher agregate throughput speed. Redundancy level far exceeds LAN type. Radtol simpler to implement, use radhard/tol FPGA if ASIC not avail. Disadvantages: Increased switching complexity. EMI potential appears higher.
Tower CPU	PowerPC vs R3081 or Mongoose-V/VII	Advantages: Device type will be qualified and used by other programs. Lower power/speed ratio. Low cost parts. COTS availability. Industry support. Future upgrades expected. Disadvantages: Greater effort to rad qualify.

Data Acquisition Trade Studies

ACD readout and control	Tower dependent vs standalone (Prototype will be tower dependent)	Tower dependent advantages: Increased system reliability through tower redundancy. Uses same cable as L1T inputs. Reduces ACD stand alone control and data acquisition requirement. Stand alone advantages: Minimizes EMI risk through no tower data flow if L1T inputs omitted. Simplifies integration and test.
Calorimeter readout control	Tower dependent vs stand alone	Advantages: Minimizes readout complexity. Minimizes CAL processing (omit DSP). No network requirement. Minimum power solution. Disadvantages: Requires min of 4 cables per CAL (one per board).
Calorimeter sparse readout	All data available at Level 2 vs sparse readout	Advantages: Eliminates need for additional CAL board (mass, power, cables, test, integration, cost). Simple programming when all data always available. Minimizes data flow risk from deciding how to sparsify data. Reduces decision tree. Disadvantages: Higher average data rate to Tower CPU (9.6 us/event for CAL to TEM vs TBD).
FPGA part type	ACTEL RadHard, Altera, Atmel, Xylinx, ULP-CMOS	ACTEL Radhard: Existing, Rad hard, expensive, high power, one time programmable. Fallback Altera: Programmable, low voltage/low power versions available, unknown radtol. Under study for qual testing. Atmel: Programmable, future version rad hard, probably high power. Current GSFC development program Xylinx: Programmable, reported not to pass radtol tests. Disqualified ULP-CMOS: Essentially zero power for core, rad hard, no SEU/SEL, programmable, requires development, first device could be avail June 1999. Reduce power in all subsystems by extensive use: potential nominal inst. power savings of 140 watts. Proposed

ATD Option I Objectives

★ Complete the prototype tower and test in the SLAC beams.

★ Complete simulations and trade studies needed to finalize the detailed conceptual design.

- Move forward with preparations for procurement of the silicon-strip detectors needed for the flight instrument—obtain prototypes from several manufacturers. (9.5×9.5 cm^2 detectors from 6-in. wafers.)
- Continue with tracker front-end electronics development—investigate new processes (SOI, 3-V 0.5 μm, *etc*.), improvements, latchup tests…
- Move forward with DAQ development beyond the prototype tower.
- Move forward with mechanical engineering needed for eventual construction of flight-ready tracker towers—especially carbon composite tray structures, if possible (funding is lacking at this time):
  - minimal multiple scattering combined with excellent mechanical properties,
  - excellent thermal match to silicon,
  - *but needs a long development lead time*. (We should start this year!)

Conclusions

- The Monte Carlo performance predictions presented for the Silicon-Strip GLAST Tracker are solidly backed up by beam-test results which show excellent agreement between measurements and simulations, *even in the tails of the distributions*.
- The most critical technology for the tracker—complete front-end electronics with low noise and only 200 μW/ch power consumption—has been thoroughly prototyped and successfully demonstrated.
- Detailed engineering design and analysis of the complete tracker tower has been carried out, and construction of a prototype tower is well under way, with beam tests planned for the end of this year.
- A complete data acquisition system design is in hand at the conceptual level, and a working VME-based prototype of the tracker readout and trigger portion has been built and tested together with the front-end readout electronics.
- Significant progress has been made on developing and engineering the design of the integrated flight instrument. In parallel with the prototype tower construction, trade studies involving extensive Monte Carlo simulations are under way to optimize further and finalize the detailed conceptual design.