A Prototype Amplifier-Discriminator Chip for the GLAST Silicon-Strip Tracker

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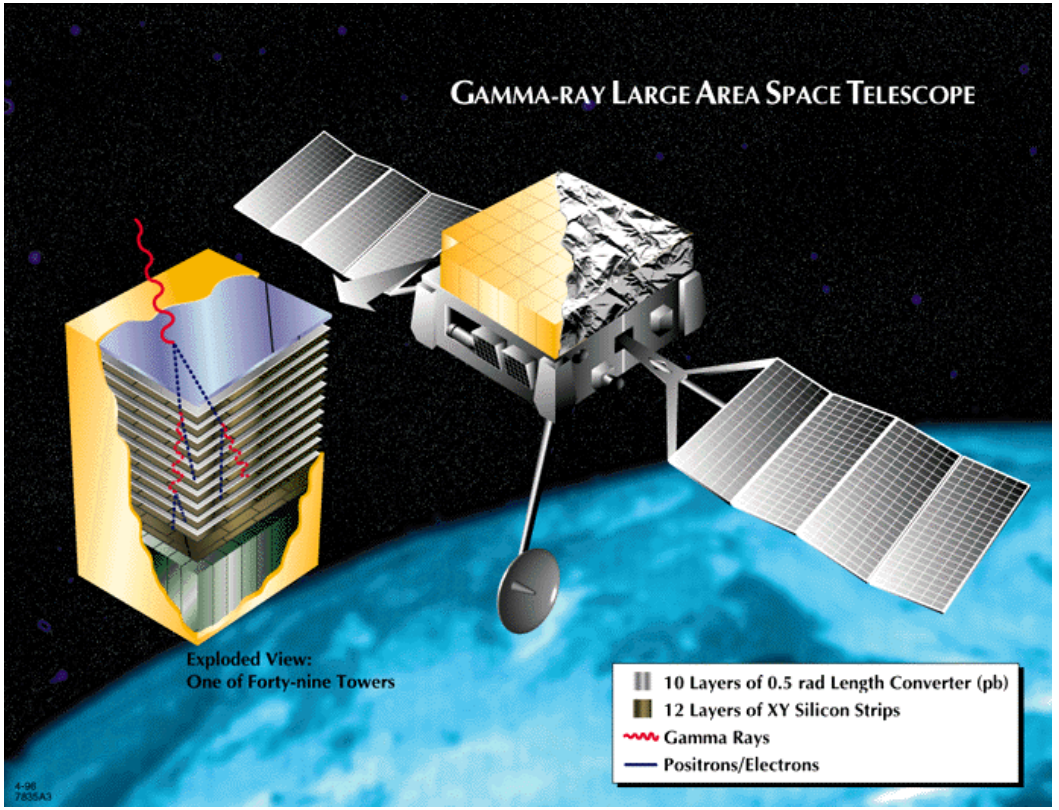


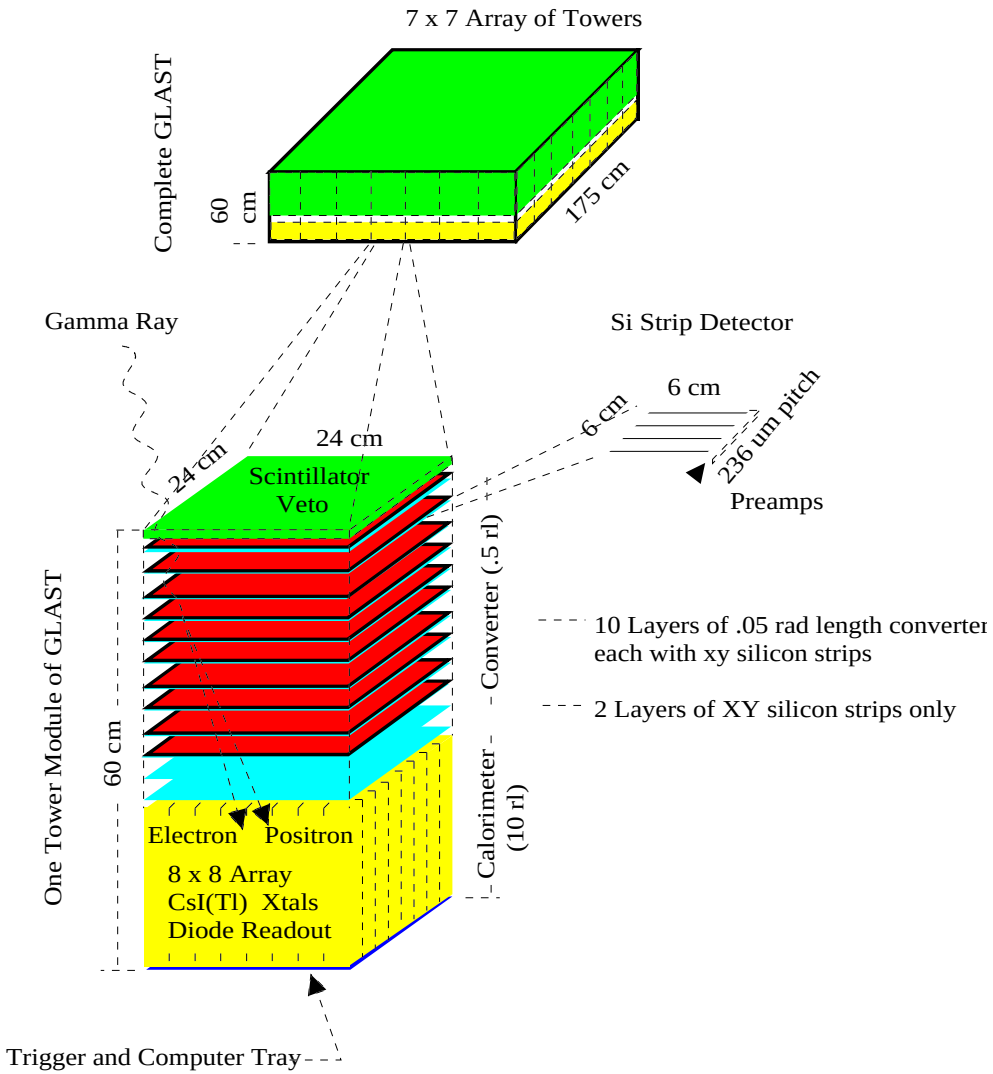
The GLAST Project

- An orbiting gamma-ray pair conversion telescope for observation of photons above 10 MeV from astronomical sources.
- GLAST will view nearly half the sky at once, with excellent sensitivity to rapidly varying sources.
- GLAST will improve by one to two orders of magnitude on the sensitivity of the highly successful EGRET experiment operating since 1991 on the Compton Gamma Ray Observatory.
- A compact silicon-strip based tracker affords a very large field of view with low dead-time, excellent pattern-recognition capability and background rejection, and optimal angular resolution.
- Plastic scintillator veto counters work together with the tracker to provide a fast trigger. Segmentation minimizes self-veto from the calorimeter back-splash.
- A highly segmented CsI calorimeter provides good energy resolution over a large dynamic range and aids in background rejection.

The GLAST Instrument Concept

GLAST conceptual design. (The current baseline design is for a 5×5 array of 32-cm square towers, each with 16 x,y layers.)

Assembly of identical modules, each with a veto shield, a silicon-strip tracker, and a calorimeter.



Tracker Electronics Requirements

Challenge: 1.3 million readout channels operating with high reliability in a space environment.

- Power less than 300 μW/channel, including amplifiers and digital readout.
- Low noise occupancy (<0.05%) and good threshold uniformity.
- Microsecond peaking time for the amplifiers.
- Self triggering.
- Radiation hard to 10 kRad with latch-up immunity.
- <1% dead-time at a 10 kHz trigger rate (must be able to acquire data while reading out previous events).
- Sparse readout and data formatting close to the front end.
- Sufficient redundancy to be immune to single-point failures.

Electronics Status

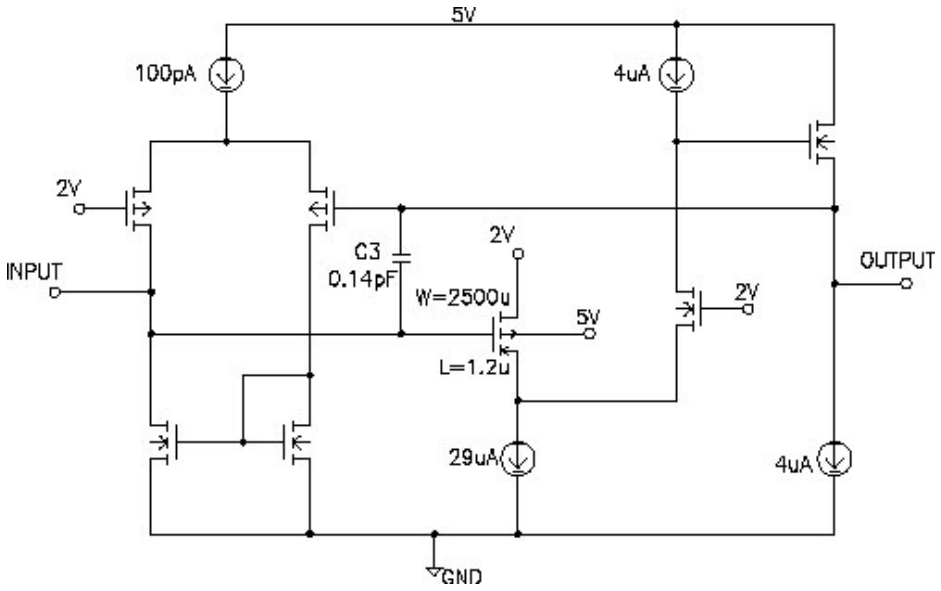
- 16-channel prototype produced on the HP 0.8μm process and tested.
- 32-channel prototype produced and 60 used in an extensive beam test last month (data analysis is in progress).
- Final 64-channel design with full digital readout capability is nearly ready for prototype production.
- Digital readout controller design is in progress.

GLAST Silicon-Strip Dectectors

- Single sided 6.4 cm square wafers 400 μm thick.
- AC coupling; polysilicon resistors for biasing.
- 195 μm strip pitch; 50 μm strip width.
- 5 detectors ganged together in series, for a total strip capacitance of ≈38 pF.

Preamplifier Design

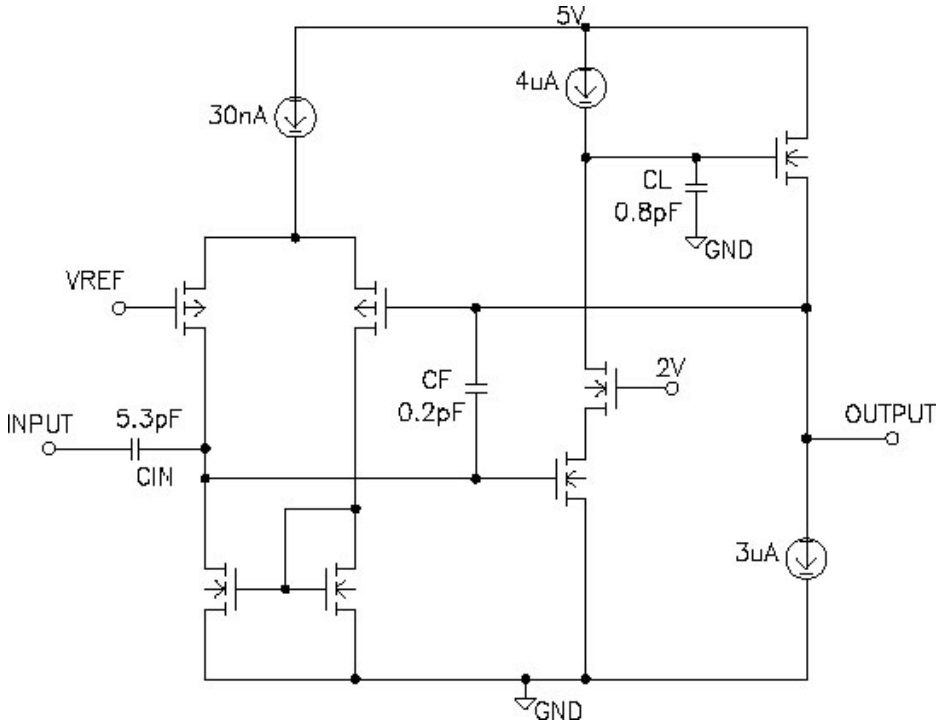
- Standard folded cascode amplifier with 2V bias for the front end, to save power.
- ≈25 μA bias current set by an external resistor.
- Slow differential amplifier stabilizes the bias point and provides a continuous reset.
- Input impedance ≈5 kΩ gives ≈200 ns time constant with GLAST 38 pF detector load.
- Open loop gain: 64 dB at 0 Hz
- Power: ≈90 μW



Preamplifier schematic.

Shaping Amplifier Design

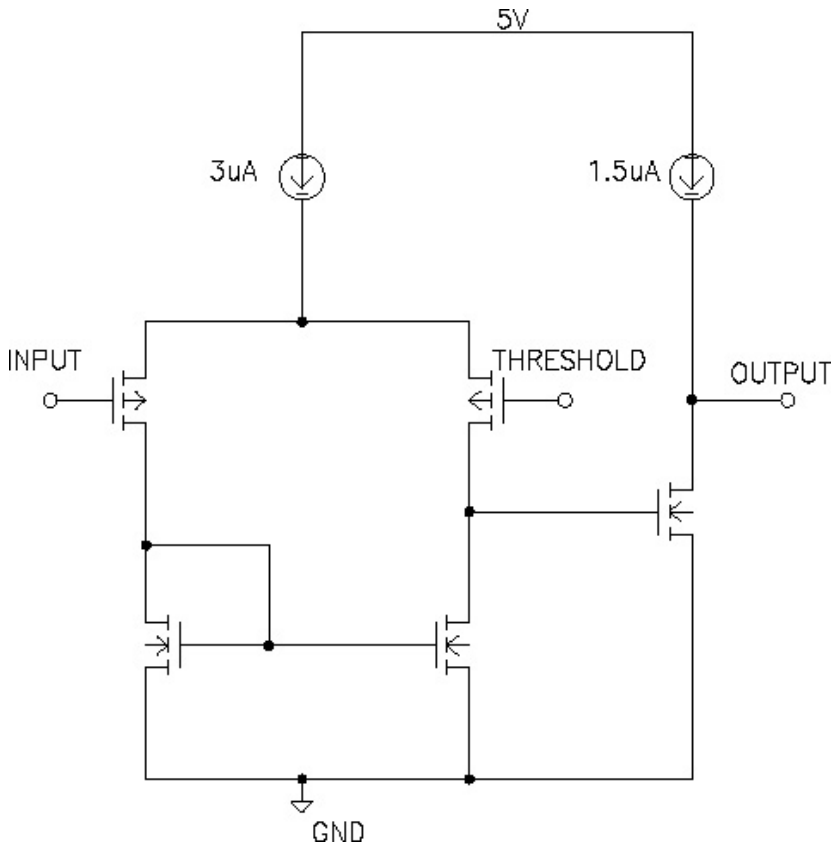
- AC coupling from the preamplifier.
- Conventional cascode amplifier with capacitive feedback.
- Slow differential amplifier in the feedback provides the "differentiation" function *and* stabilizes the output bias point. (Ref.: I. Kipnis, LBNL)
- Open loop gain: 62 dB at 0 Hz
- Voltage gain: ≈26
- Peaking time: ≈1.3 μs
- Pulse shape: reset current source makes a tail that is more linear than exponential, except at the lowest pulse heights.
- Power: ≈35 μW



Shaping Amplifier Schematic

Comparator Design

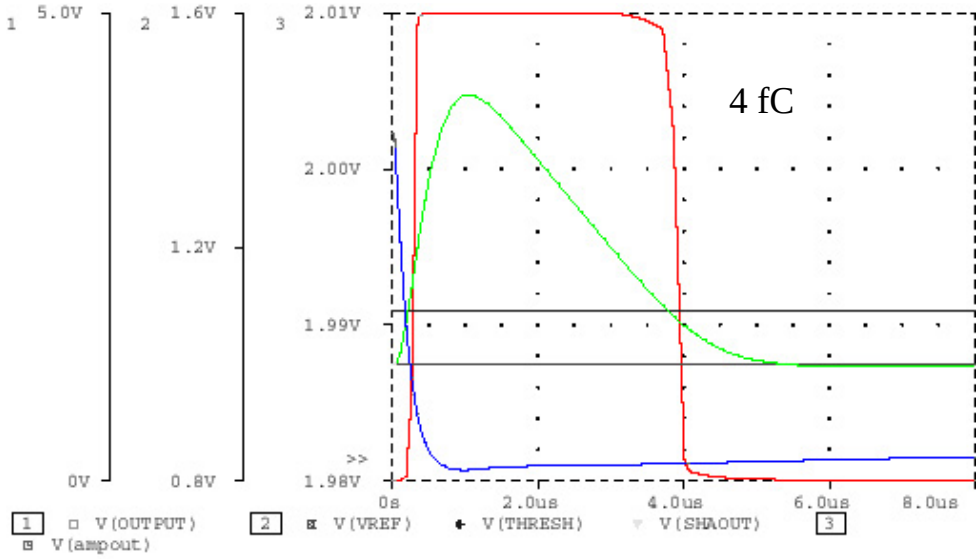
- Conventional two-stage comparator, with DC coupling from the shaper output.
- No current in the second stage in the quiescent state (with no input signals).
- Only 17μW of quiescent power.

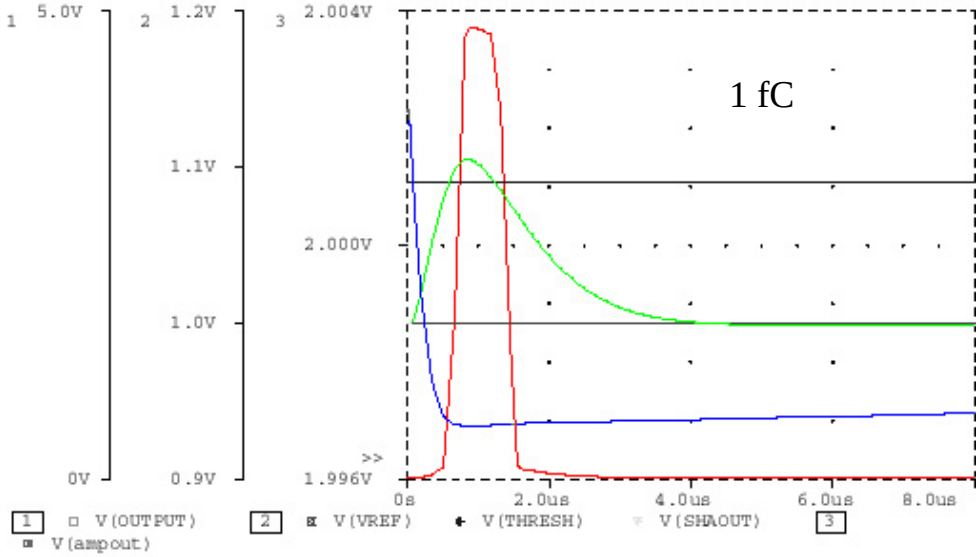


Comparator Schematic

Analog Signal Shapes

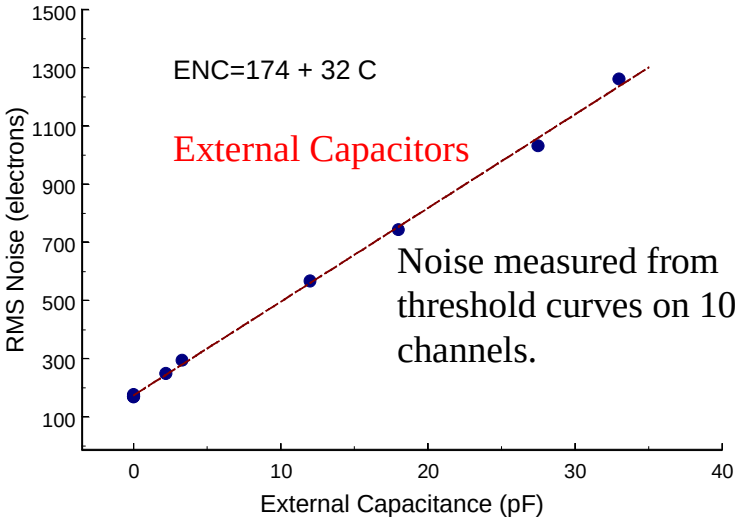
- Top: preamp, shaper, and comparator outputs for a 4 fC input charge.
- Bottom: 1 fC input charge.
- In both cases, the shaper baseline and the threshold (90 mV) are shown by solid black horizontal lines.

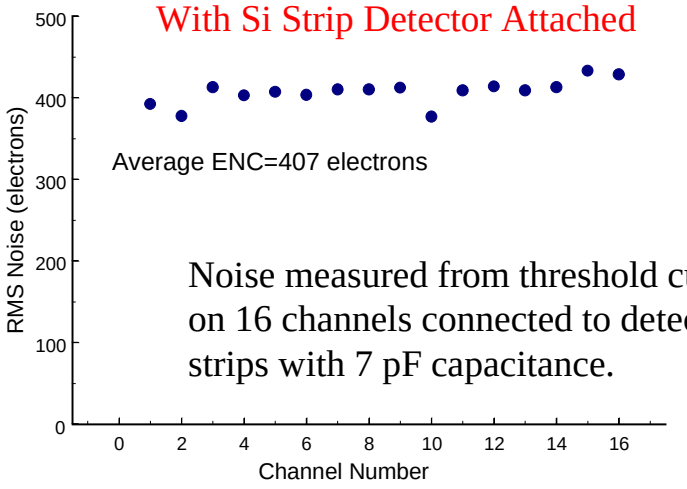


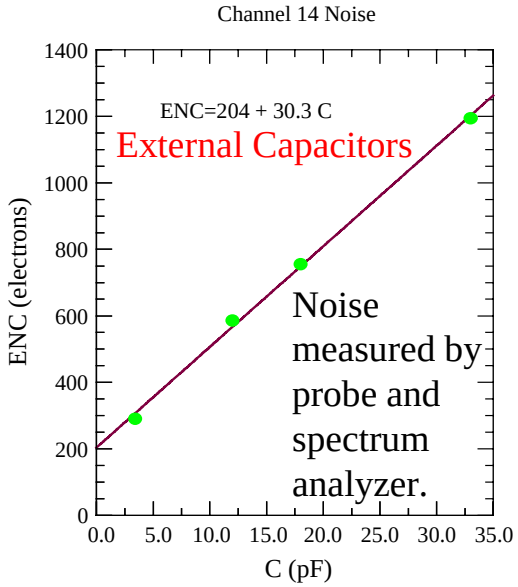


Measured Amplifier Performance

- Gain (shaper output): ≈125 mV/fC
- Peaking time: ≈1.3 μ s
- Power consumption, including bias circuitry: 150 μW/channel
- Noise: ENC=204 + 30.3×C electrons, with C in pF, measured by several methods, as shown here.

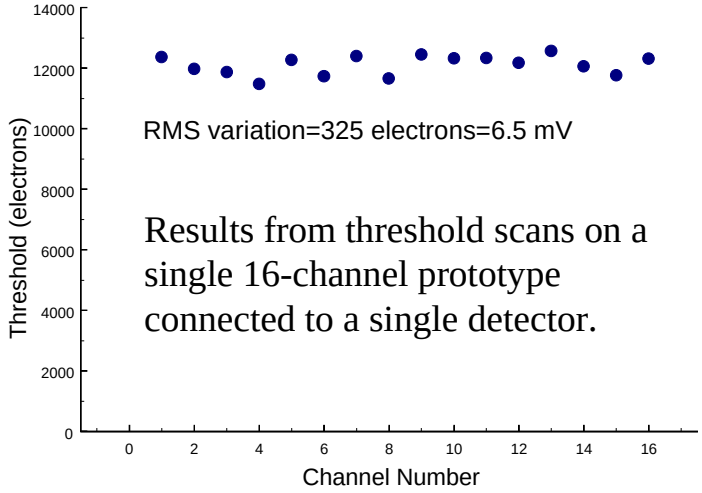




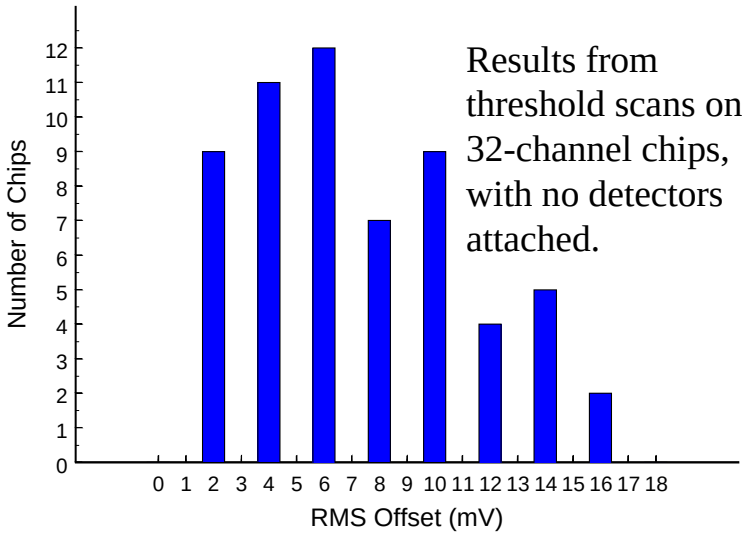


Threshold Matching

- Threshold matching from channel to channel across a given chip depends primarily on the transistor pairs in the shaper feedback.
- Most chips meet the desired upper limit of about 15 mV rms threshold variation (compared with the ≈32 mV rms noise level).
- Work is in progress to try to improve this figure further in the next prototypes.



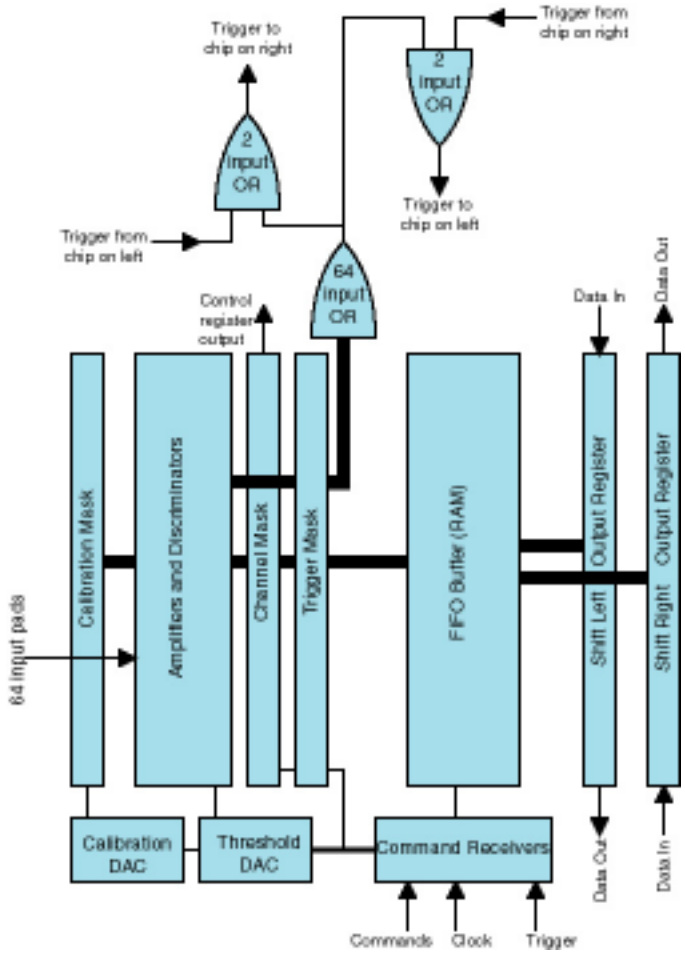
Results from threshold scans on a single 16-channel prototype connected to a single detector.



Results from threshold scans on 59 32-channel chips, with no detectors attached.

Digital Readout Design

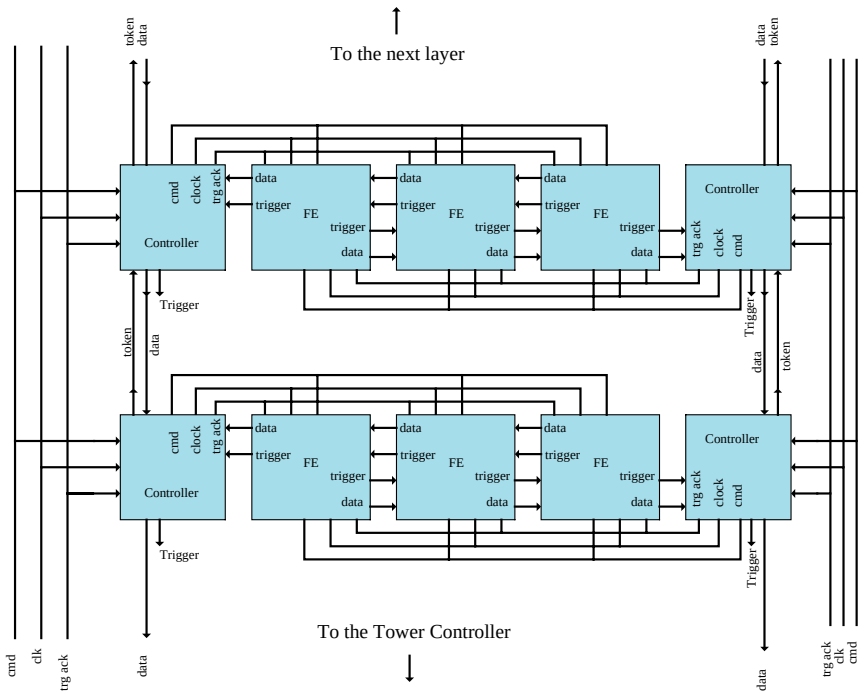
- The 64-channel chip currently being designed has the following additional features:
  - Calibration mask, to select any subset of channels to be pulsed.
  - 7 bit DACs for setting calibration and threshold levels.
  - Separate masks for data and trigger.
  - 8-deep FIFO event buffer.
  - Dual redundant serial command decoders.
  - Dual redundant output shift registers and trigger outputs.
  - Bypasses to avoid clocking out data from empty chips.
  - External communication via low-voltage-swing differential signals.



Simplified block diagram of a readout chip.

Digital Readout Design

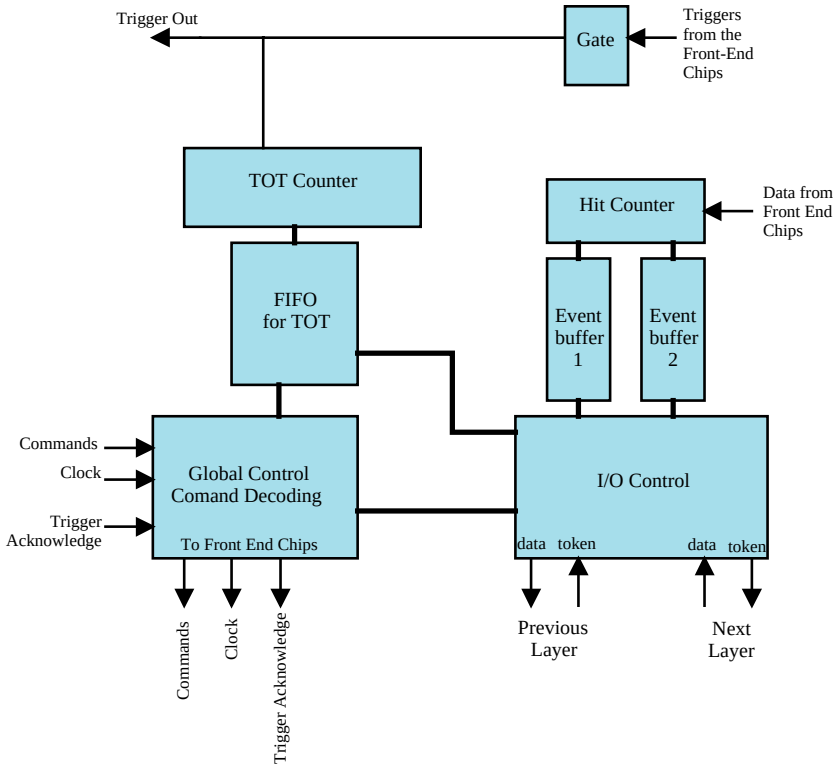
- 25 64-channel readout chips handle a single detector layer.
- Data can shift out left or right, or in both directions, with a readout-controller chip at each end of the chain.
- Trigger signals also move left or right, or in both directions.
- Either readout controller chip can reprogram the readout direction of any of the front-end readout chips, so a single dead chip can be bypassed without losing data from any other chips.
- The readout controller chips pass data down the tower in a token-controlled protocol.



Simplified block diagram of the readout of a GLAST tower, showing only 2 of 16 layers and only 3 of 25 readout chips on each layer.

Readout Controller Chip

- Control initialization, calibration, and readout of the front-end readout chips.
- Sparse readout—build list of hit-strip addresses.
- Calculate the time-over-threshold of the prompt trigger output.
- Build events and coordinate the readout with neighboring layers via a serial data line and a token.
- External communication via low-voltage-swing differential lines.
- Currently being designed for the HP 0.8 μm process using the CMOSX standard cells.



Simplified block diagram of the readout controller chip.

Conclusions

- The basic amplifier-discriminator requirements of the GLAST silicon-strip tracker have been met and demonstrated with prototypes.
- A month-long beam test with electrons and tagged-photons has just been completed. (See another poster in this session with preliminary results.)
- Design of a complete readout system meeting the GLAST flight requirements is in progress.
- A complete prototype GLAST tower, utilizing this readout system for the tracker, will be fabricated and tested during the next two years.
- The electronics design will continue to be improved (and must migrate away from the HP 0.8 μm process), leading up to a GLAST construction start projected for the year 2000.