# Overview of the Baseline Design

- 16 towers, each with 37 cm $\times$ 37 cm of Si
- 18 *x,y* planes per tower
  - 19 "tray" structures
    - 12 with 2.5% X_0 Pb on bottom
    - 4 with 25% X_0 Pb on bottom
    - 2 with no converter
  - Every other tray rotated by 90°, so each Pb foil is followed immediately by an *x,y* plane
    - 2mm gap between *x* and *y*
- Electronics on the sides of trays
  - Minimize gap between towers
  - 9 readout modules on each of 4 sides
- Trays stack and align at their corners
- The bottom tray has a flange to mount on the grid
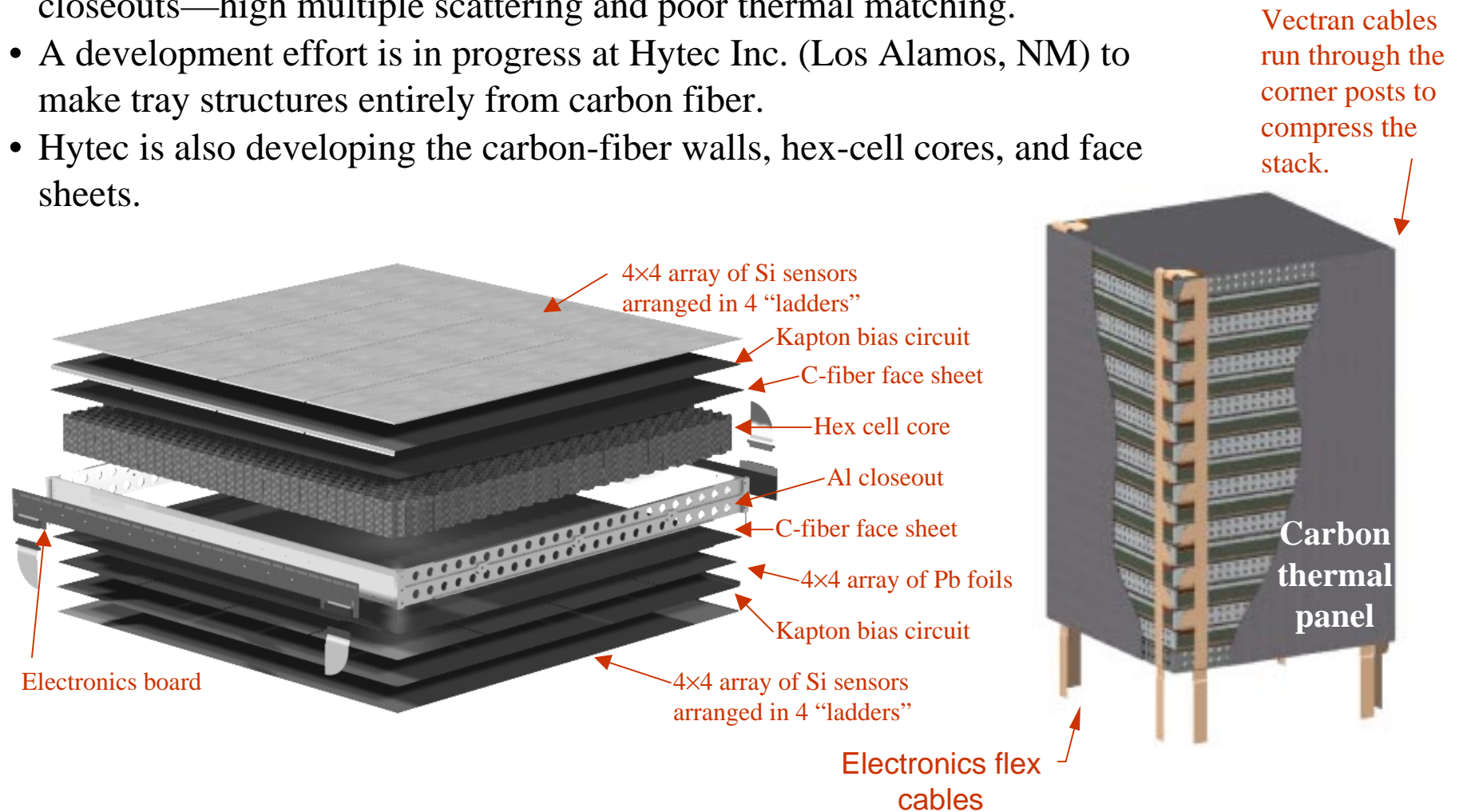- Carbon-fiber walls provide stiffness and the thermal pathway to the grid
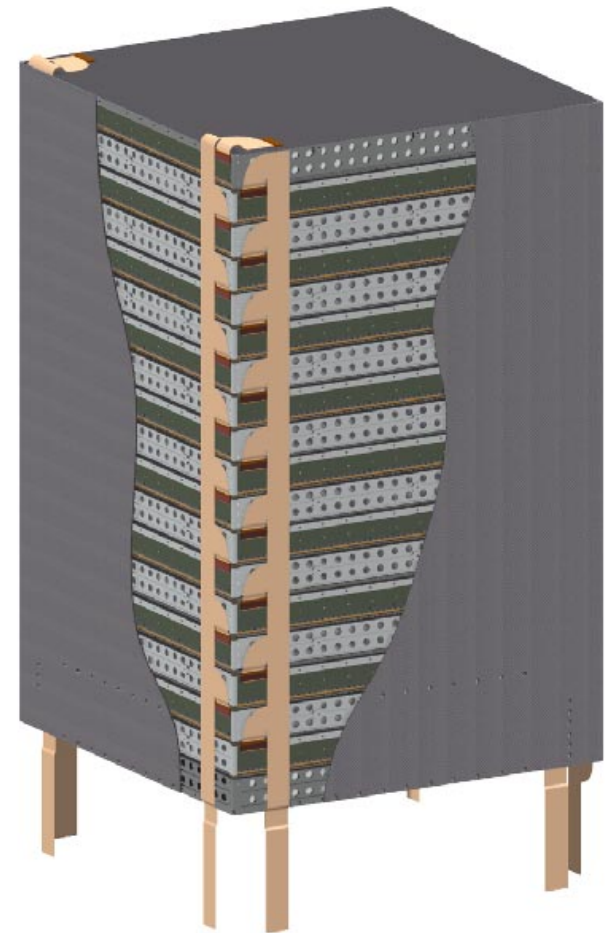
One Tracker Tower Module

February 23, 2000

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Tracker Module Mechanical Design

- The tray must be very stiff to avoid collisions ($f_0 > 500$ Hz).
- All prototypes to date have been made with machined aluminum closeouts—high multiple scattering and poor thermal matching.
- A development effort is in progress at Hytec Inc. (Los Alamos, NM) to make tray structures entirely from carbon fiber.
- Hytec is also developing the carbon-fiber walls, hex-cell cores, and face sheets.

Vectran cables run through the corner posts to compress the stack.

4×4 array of Si sensors arranged in 4 "ladders"

Kapton bias circuit

C-fiber face sheet

Hex cell core

Al closeout

C-fiber face sheet

4×4 array of Pb foils

Kapton bias circuit

Electronics board

4×4 array of Si sensors arranged in 4 "ladders"

Carbon thermal panel

Electronics flex cables

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Carbon-Composite Tray

- Honey-comb core
  - we have a supplier, but price is still an issue (much higher cost than aluminum)
- Face sheets
  - C-fiber already used in beam-test tower
  - C-fiber is essential here for strength and for thermal matching with silicon
  - Hytec has a new idea to mold in spacers on the surface for the converter foils
- Closeouts
  - Simple carbon-fiber C channels on 4 sides
  - Additional piece on the 2 electronics sides, machined from a 3-D resin-impregnated fiber
  - Metal inserts for screws
- This is currently being prototyped, but one major remaining issue is how to treat the surface, especially in the machined areas.

Mount and thermal conductor for electronics

C channel

Points for mounting side walls

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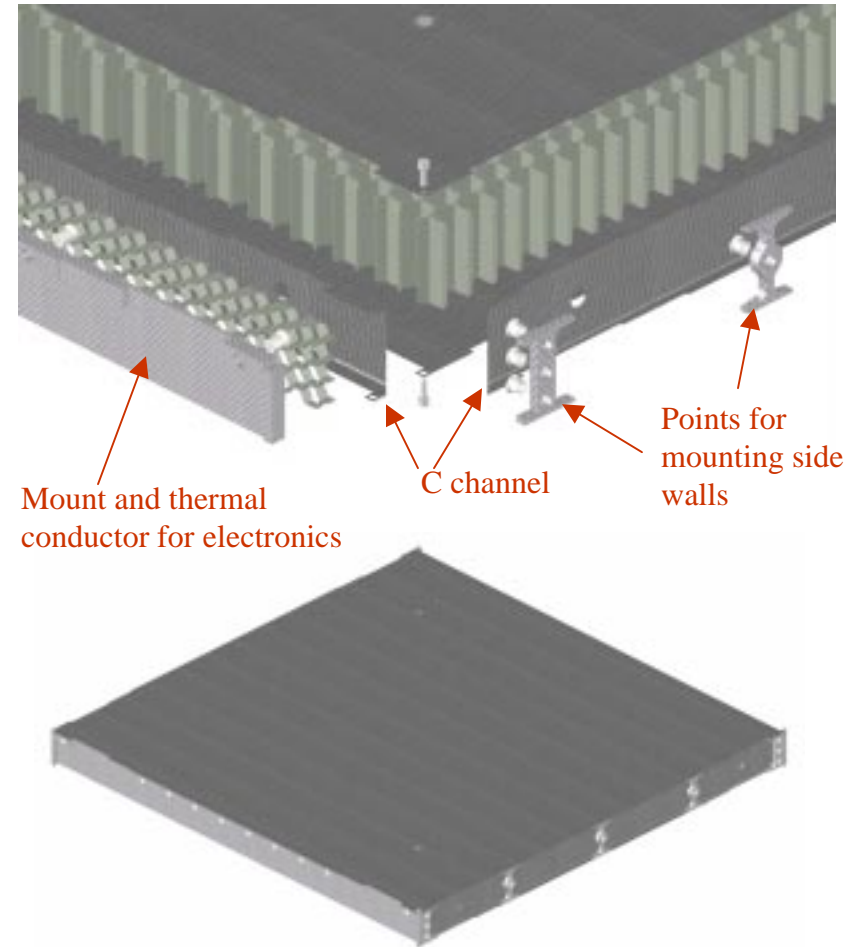
Silicon-Strip Detectors

- 400 μm thick, single sided
- 9.2 cm × 9.2 cm (still to be reviewed)
- Strip pitch is not finalized:
  - 194 μm pitch in beam test module
  - 201 μm in the NASA proposal
  - May have to increase to 235 μm or 282 μm, depending on power allocation
- AC coupled with polysilicon bias (~60MΩ)
- Beamtest module: 296 detectors from 4" wafers and 251 from 6" wafers from HPK, plus 5 of the large size from Micron.
  - Typical leakage: 300 nA/detector (HPK)
  - Bad strips: about 1 in 5000
- 35 9.5-cm square detectors from HPK
- Prototypes on order from STM
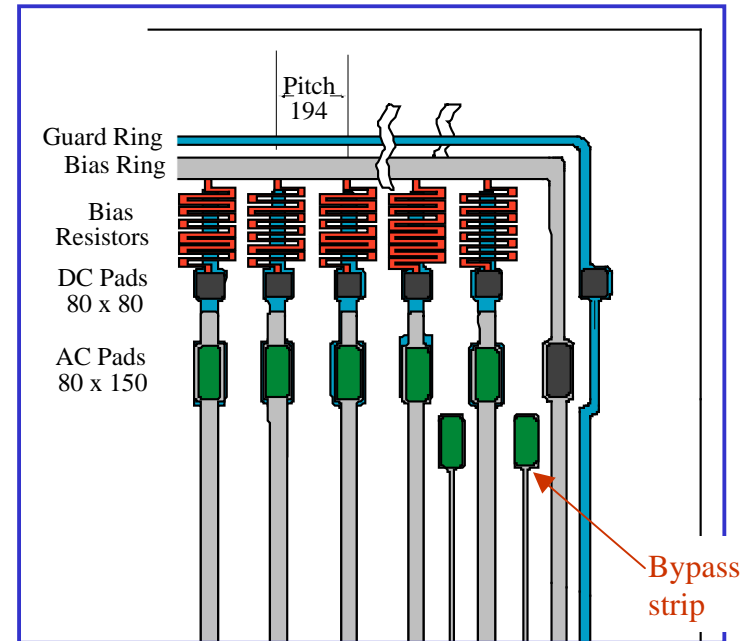
Schematic layout of the proto detectors.
- Bypass strips will not be used.
- DC pads will increase in size.
- A second AC pad will be added on each strip, for probing and for a second chance at wire bonding.
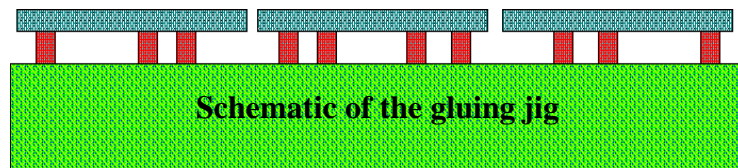
Si Detector Ladders

- Detectors were edge bonded at SLAC by hand, using a simple alignment jig.
  - Some problems with vertical steps on the larger detectors.
  - Not ideal control of the amount of epoxy in the joint (a few joints failed during later handling).
  - Bond-line thickness set by hand and amount of adhesive.
  - Alignment in the plane: ~30 μm typ.
- Wire bonding is straightforward.
- Wire bonds were encapsulated with a hard curing epoxy.
  - Epoxy was sprayed onto the bonds through a slit.
  - Control was by hand and eye (tedious).
  - There was some overspray.
  - More efficient methods need to be investigated. Or is it even needed?

Edge joint and wire bonds before encapsulation
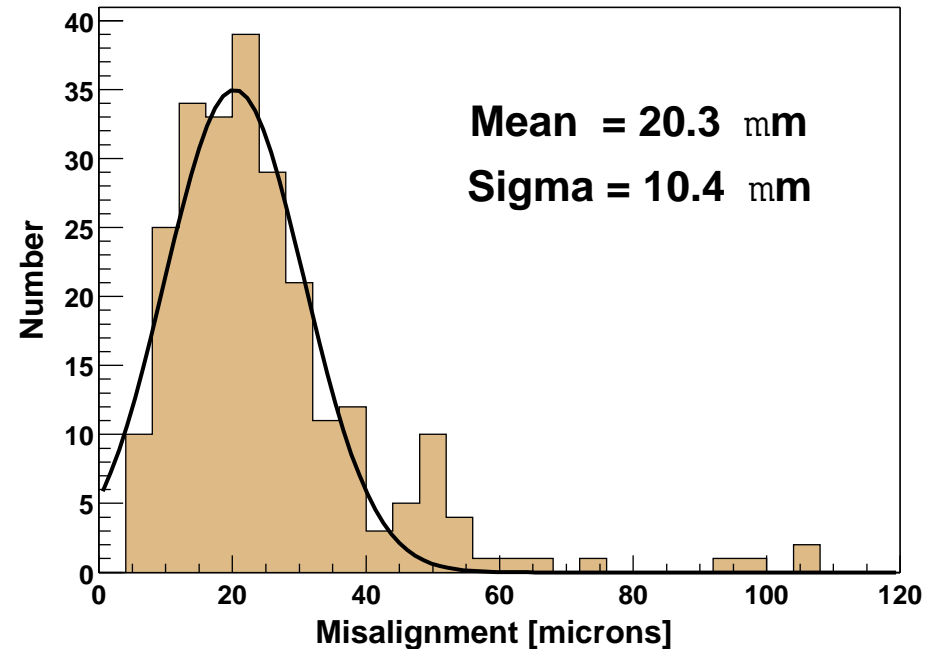

Encapsulated wire bonds

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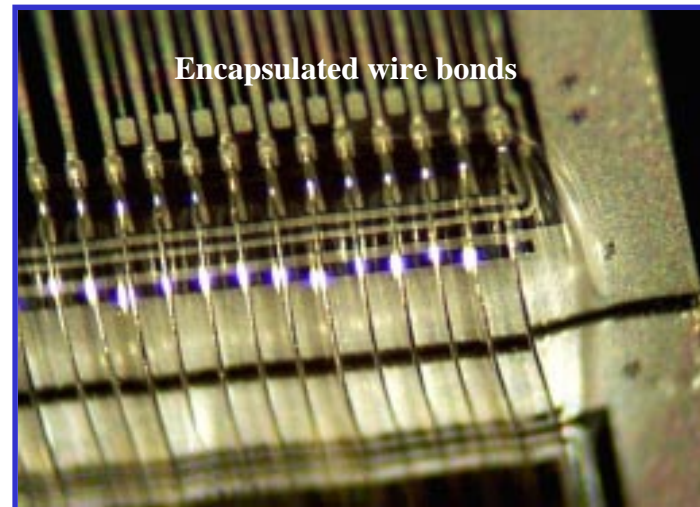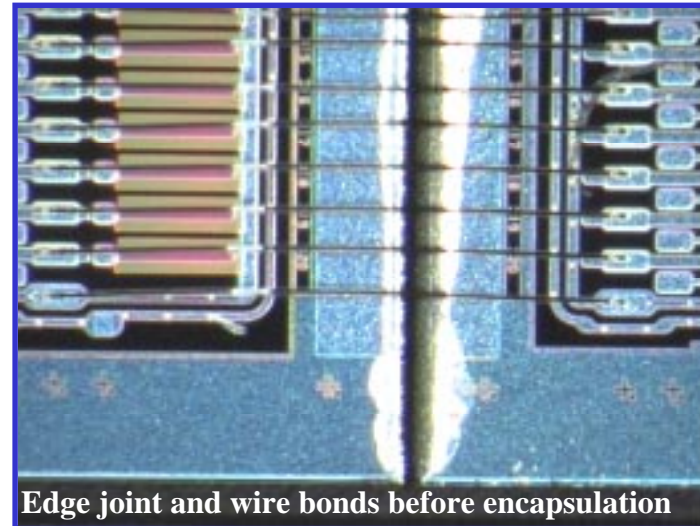
Ladder Survey for the Beam-test Tracker

- The ladders all were surveyed on an automated optical measuring stage.

- Most of the ladders were adequate, but we are not satisfied with those with >50 μm deviations.

Mean = 20.3 μm

Sigma = 10.4 μm

Misalignment [microns]

For each ladder, the maximum deviation of the fiducial marks from a straight-line fit is entered into this histogram.

Schematic of the gluing jig

The gluing jig was built for ladders made from 5 small detectors. The larger detectors were not optimally supported, such that any deviation from flatness results in z steps.

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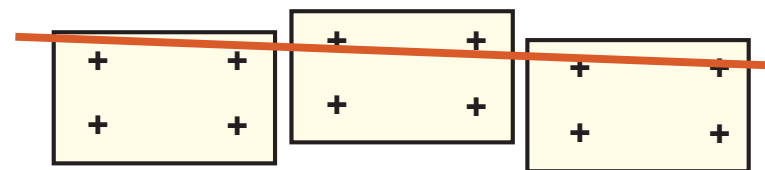
# Ladder Placement on Trays

- Ladders were aligned with respect to the holes in the corner posts, by pressing against a straight edge.
- Shims set the spacing between ladders.
- Silver-loaded epoxy was used to bond detectors to the bias circuit.
- 50 µm thick tape set the adhesive bond thickness.

- *This procedure relies upon accurate dicing of the detector wafers.*
- *Lots of issues with adhesives still need to be worked out.*

Alignment jig

Handle attached to the closeout for handling during assembly.

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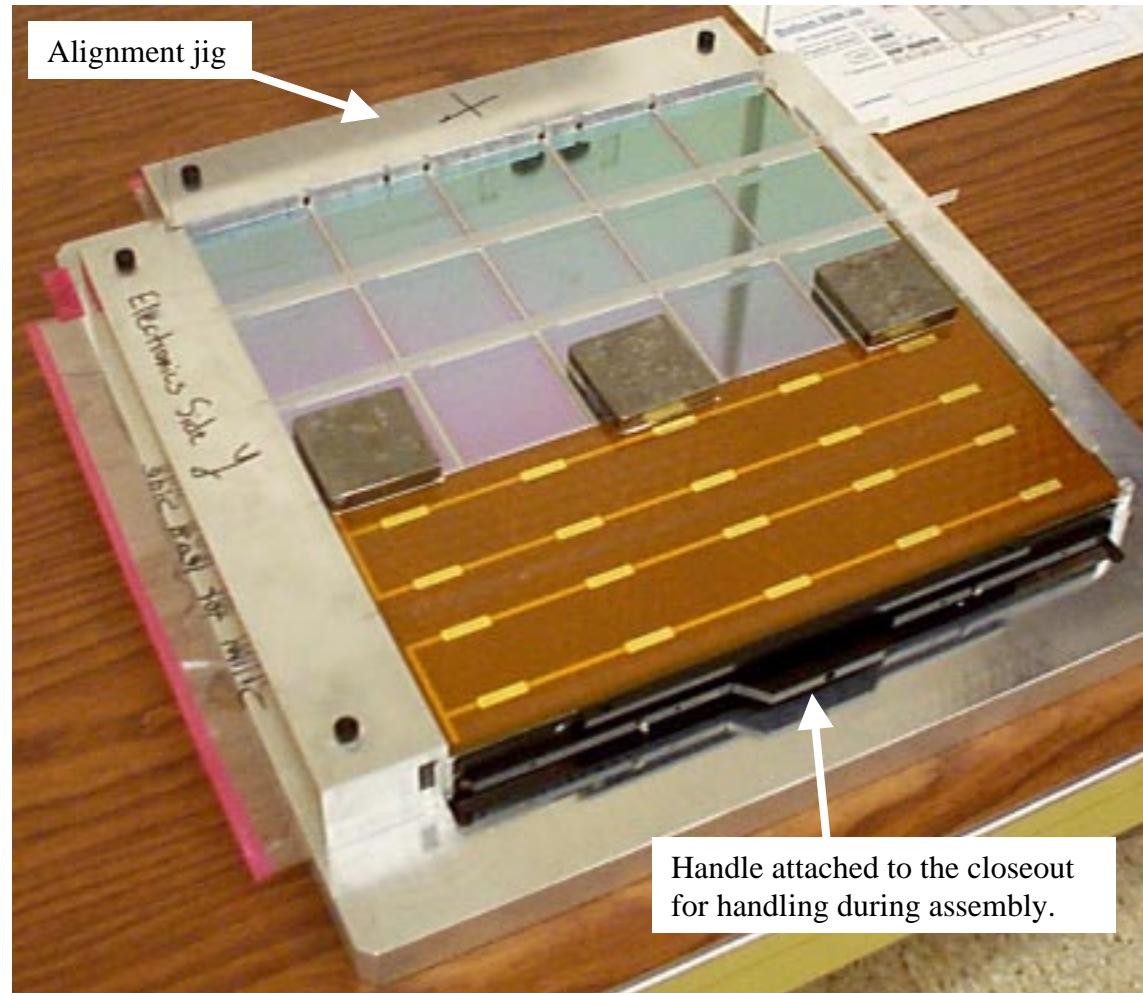
- All 17 beam-test trays were optically surveyed on the automated measuring stage.

- Lines were fit to the detector fiducial marks in a ladder and the angle measured with respect to a line between the centers of the corner posts.

TRAY

corner
post

Mean = 0.009
Sigma = 0.0154

0.04°=220μm
over a 32-cm
ladder.

Number

Angle [deg]
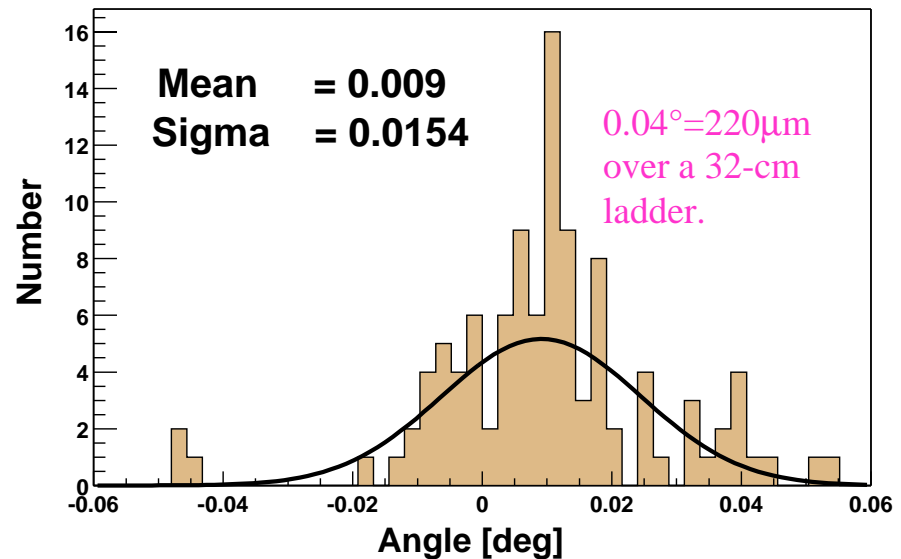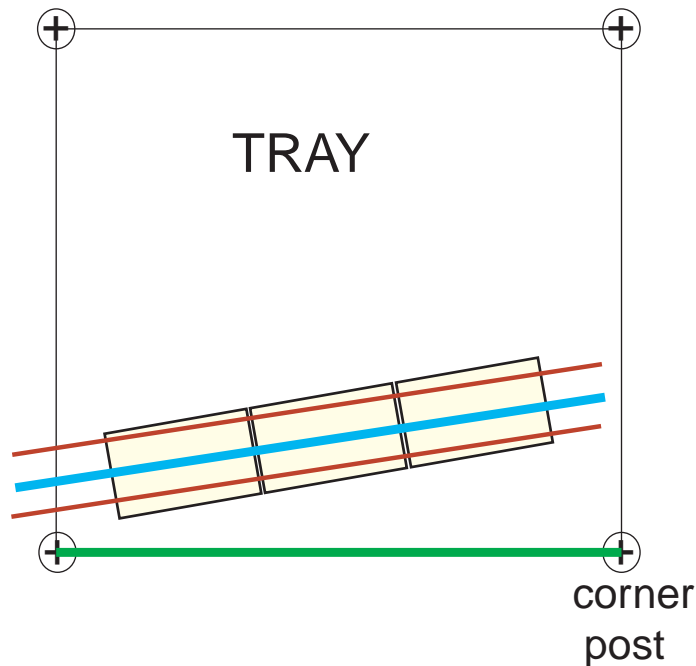
- The results, shown above, are not as good as desired (<0.02°), indicating improvements needed in the jigs and procedures.

- 3 ladders are off by >0.04° due to a known mistake on one tray (a shim slipped out), but it is not yet understood why others are off by similar amounts (partly due to slippage on the surveying stage).

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Electrical Design

- Detector bias: 2-layer Kapton flex circuit
  - Top layer: pads for conductive adhesive, to carry the bias current to the detectors.
  - Bottom layer: hatched ground plane, to isolate the detector bias from the conductive tray structure.
  - Standard space-qualified industrial processes are adequate for this.

>1600 fine traces bend around the corner.

Old bias circuit layout (1st prototype)
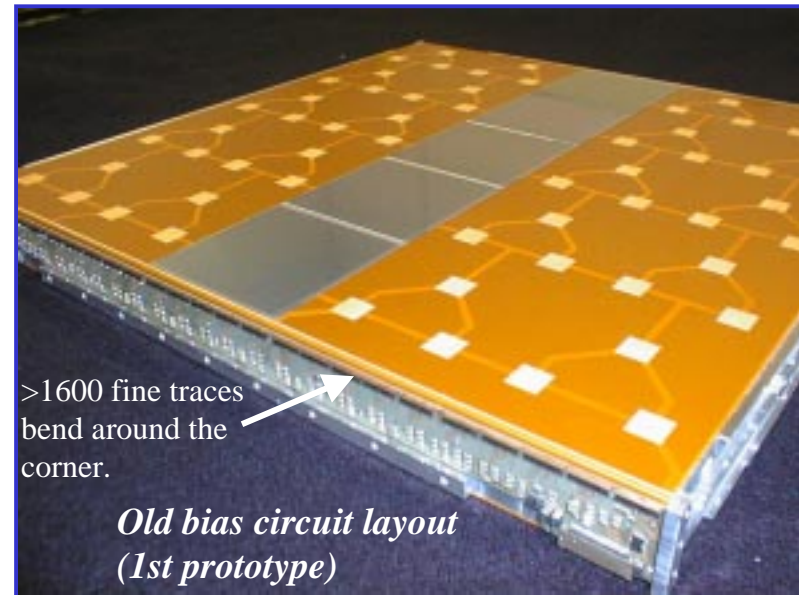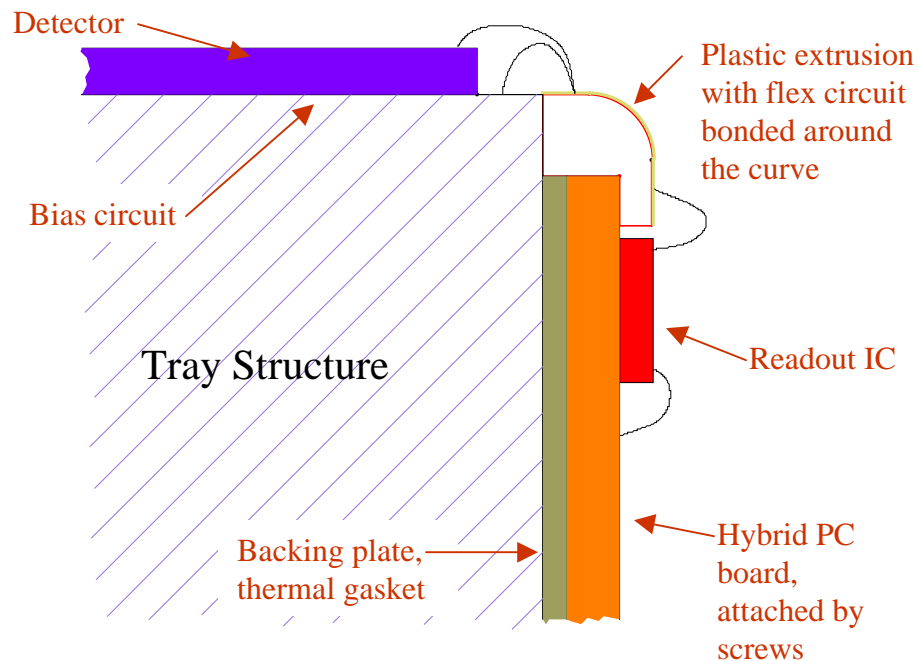
New concepts under development:

- The bias circuit HV and ground plane are divided into 4 separate circuits. We need to reevaluate the gluing pattern.
- The flex circuit for wrapping around the corner is separate from the bias circuit and is part of the hybrid assembly. It has 1 trace for each detector strip, plus bias and ground connections for each ladder.

Detector

Plastic extrusion with flex circuit bonded around the curve

Bias circuit

Tray Structure

Readout IC

Backing plate, thermal gasket

Hybrid PC board, attached by screws

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Tracker Readout Concept

2 readout controller chips for each layer

25 64-channel amplifier-discriminator chips for each detector layer

Data flow

GTFE

GTFE

GTRC

GTRC

Control signal flow

Control signal flow

Control signal flow

GTRC

GTRC

Eight detector layers are read out on each side of each tower.

GTRC

GTRC

Data flow to FPGA on DAQ TEM board.

Data flow to FPGA on DAQ TEM board.
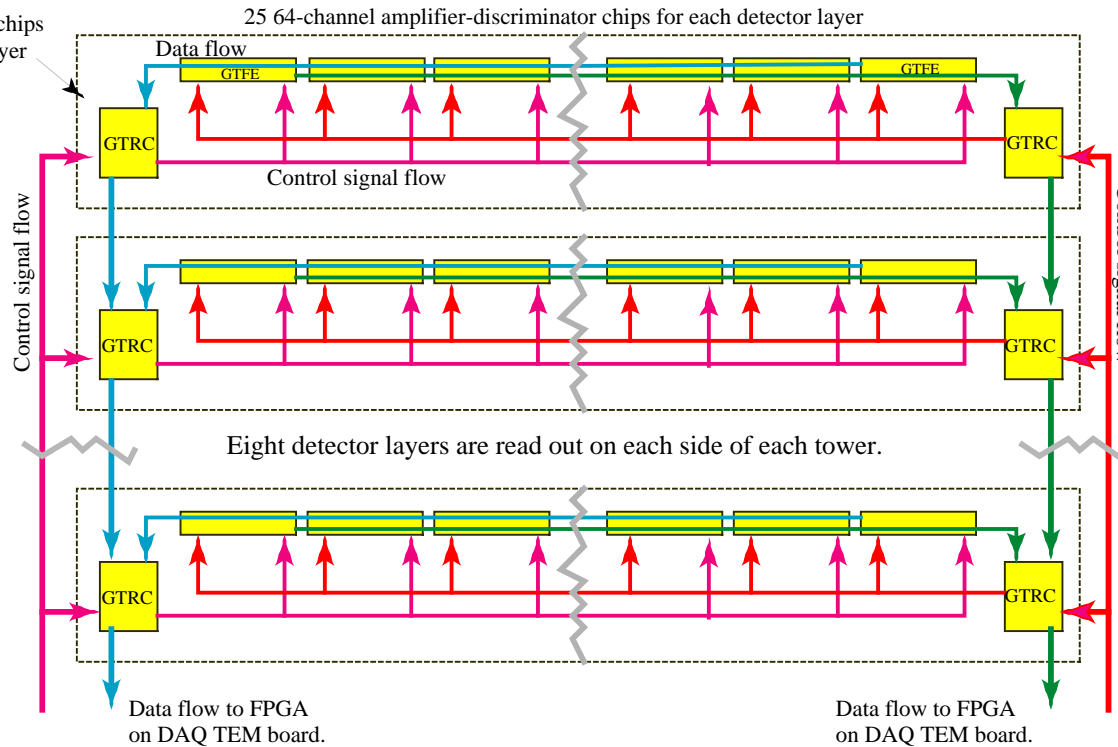
GLAST tracker front-end readout scheme, as implemented in the beam-test module.

- Two redundant paths for control signals, trigger information, and data output.
- Any single chip or cable can go bad without affecting the readout of the remaining chips.
- Zero-suppressed data from the entire tower flows out in one, or two, serial data streams.
- In the front-end chips (GTFE) zeros are suppressed only if the entire 64-channel chip has no hits.
- Complete zero suppression and formatting takes place in the digital GTRC chips.

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Hybrid PC Board

Hybrid mounted on a completed tray of the beam-test module.

Flex circuit bent around corner

Amplifier chips

Tray corner post

Boss for mechanical and thermal attachment to the wall.

HV capacitors

25-pin Nanonics connector

Digital readout controller chip

#14
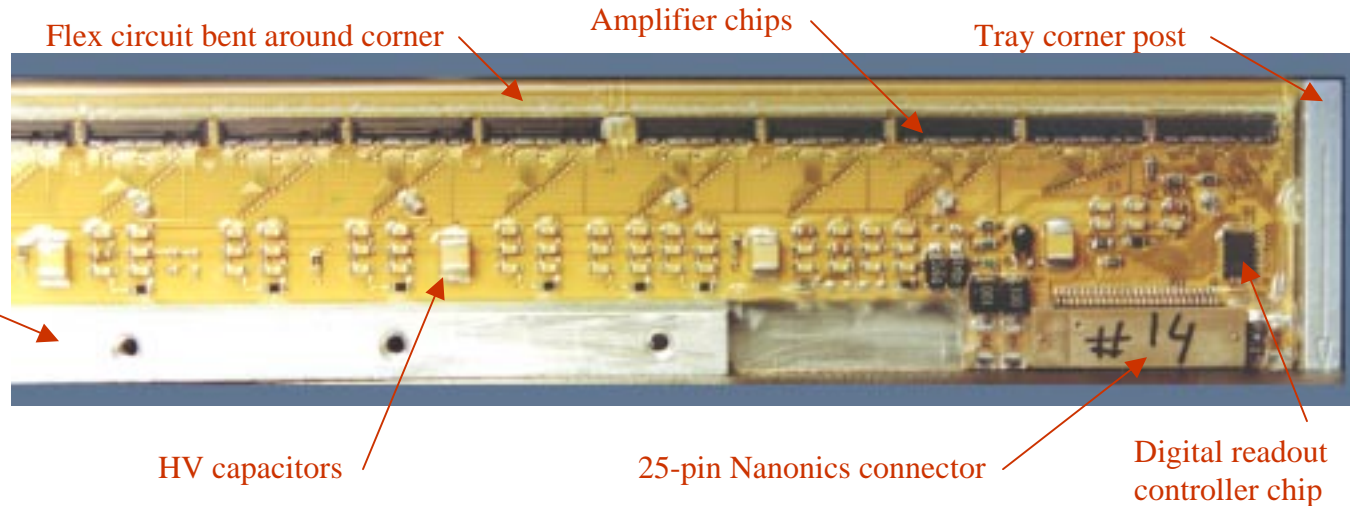
- 25 64-channel amplifier chips and 2 digital readout chips on beam-test hybrid.
- 8-layer standard FR4 PC board with minimum 100 micron traces and spaces.
- Gold body for wire bonding.
- Lots of filtering and decoupling for bias, power supplies, etc.
- Fuses on the power supplies.
- Temperature monitor.
- Careful attention to shielding between analog and digital and to maintaining clean current returns for the detector signals.
- *Still needs a lot of work to bring the design & fab up to space qualification levels.*

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Tracker Readout Cables

Lengthy run past the Calorimeter, needs shielding around cable.

TEM

4 layers of 1/2 oz copper traces and power/ground planes

Termination Resistors

Power filtering, and connection of digital and analog grounds to the shield here.
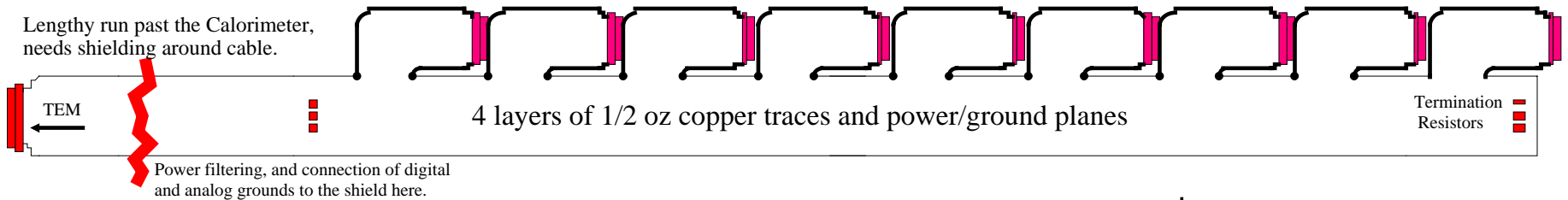
- Custom 4-layer flex circuits
- Standard processes, with Kapton and 1/2 oz copper.
- Connectors and other components are surface-mount soldered.

Cross-over into the side arms

	4
Digital 3.3V	3	Bias + Analog 3.3V
Digital Ground	2	Analog Ground
LVDS Signals	1	Analog 1.5V

Digital   Analog
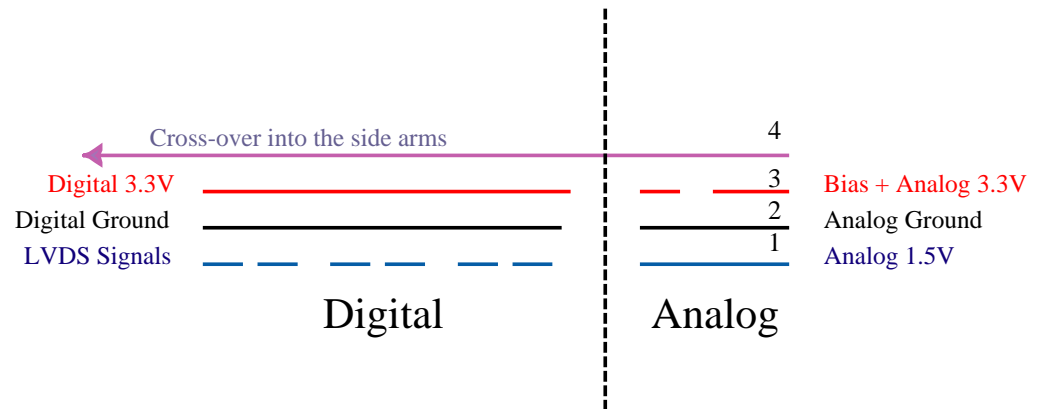
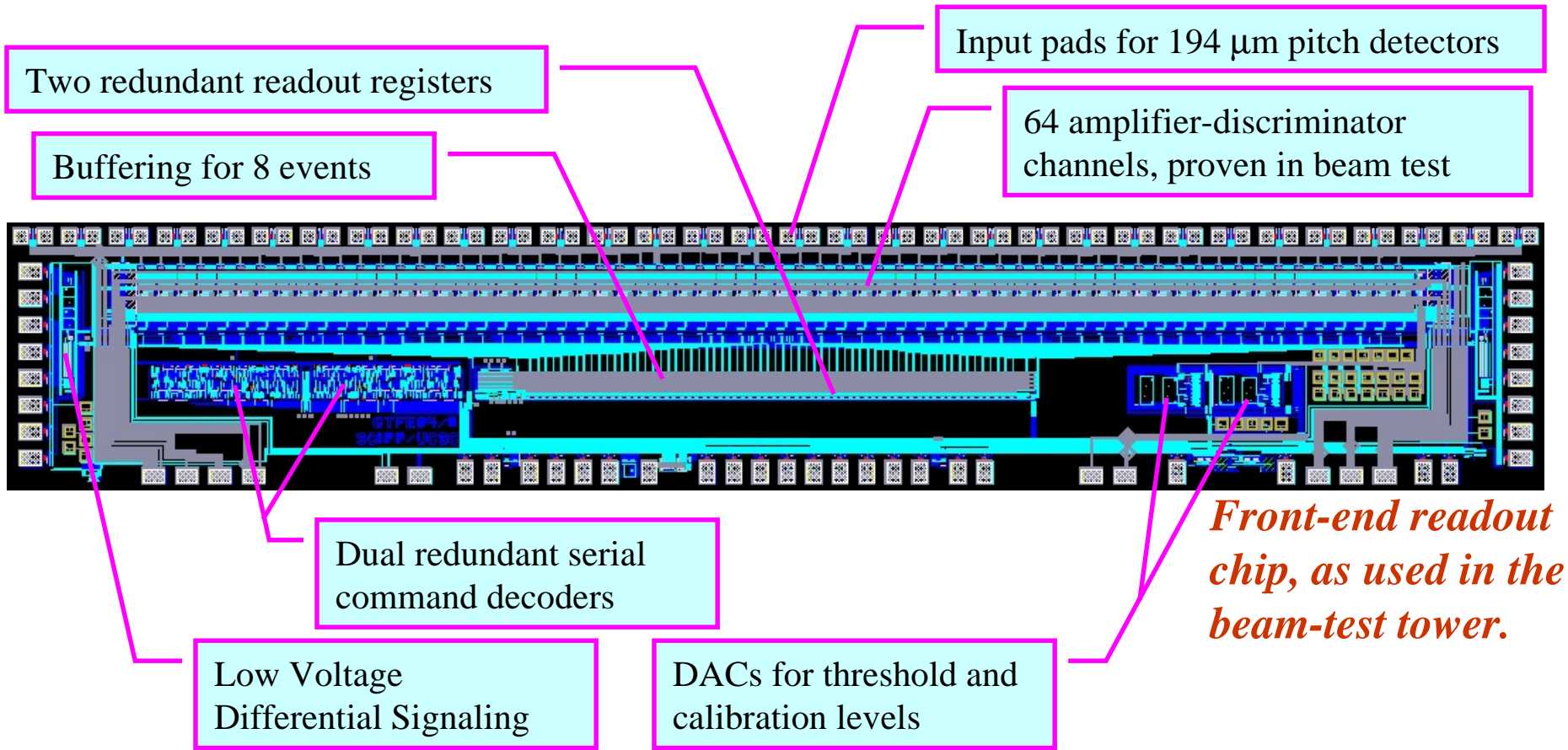*4-layer cable cross section, showing a schematic representation of the arrangement of conductors.*

Outstanding issues:
- Detailed design changes with respect to what is in the beam-test version.
- Finding a manufacturer who can do the full length (or design a splice in the center).
- Shielding while going past the calorimeter.
- Space qualification.
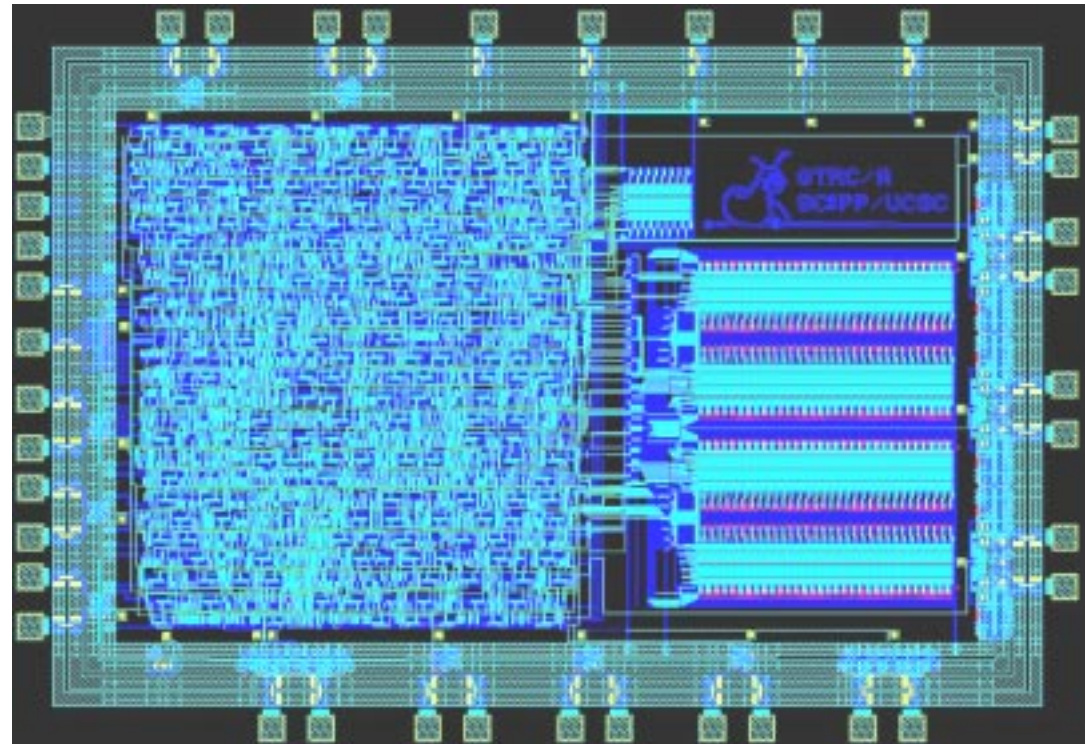
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Front-End Readout Chip (GTFE64)

- Several thousand were made in the HP 0.8 μm process for the beam-test tower and gave very good performance. This process no longer exists.
- Prototypes of just the amplifiers and discriminators fabricated in the HP 0.5 μm process are under test at UCSC and, preliminarily, appear to be working well.

Input pads for 194 μm pitch detectors

Two redundant readout registers

64 amplifier-discriminator channels, proven in beam test

Buffering for 8 events

Front-end readout chip, as used in the beam-test tower.

Dual redundant serial command decoders

Low Voltage Differential Signaling

DACs for threshold and calibration levels

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Readout Controller Chip (GTRC)

- Full custom CMOS IC, fabricated in the HP 0.8μm process for the beam-test tower.
- Logic design and layout uses DoD standard cells.
- Functions:
  – Zero suppression and formatting of the data.
  – Command and clock interface to the front-end chips.
  – Sequencing and buffering of the readout.
  – Time-over-threshold of the Fast-OR trigger output.
  – Communication via low-voltage differential signaling (LVDS).
- Functioned reliably in the beam test.
- Next version will be done in the HP 0.5 μm process.

Cadence layout of the GLAST Tracker Readout Controller chip (GTRC). The left half is logic made from standard cells, while the right half is memory for buffering.

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ASIC Issues

- A number of detailed design mods are being considered (pending a formal review of the tracker electronics design)
  - New detector pitch
  - Output information to allow buffer management to be verified
  - Larger wire bonding pads
  - Metalize back of chip
  - Separate thresholds for data and trigger?
  - etc.
- Engineering manpower: it isn't clear that we have an engineer to redo the GTRC chip design, simulation, and layout, including the new design modifications.

- Radiation hardness:
  - Total dose is very unlikely to be a problem (less than 10 kRad).
  - Single-event latchup: published measurements on the HP 0.5 μm process appear to exceed requirements. How to test?
  - Single-event upset: we are working to implement SEU-safe flip flops for the configuration register.
- Space qualification:
  - This needs to be researched. We do not yet understand all of the requirements that might be imposed.
- Time is short: final prototypes need to be ready for the engineering model by mid 2001.

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Beam-Test Engineering Model Tracker

- 16 x,y planes

- 51,200 amplifier-discriminator channels, with 41,600 connected to detector strips.

- 130 32-cm detector ladders (out of 160 needed for the complete device), for 2.6 m^2 of silicon.

- VME-base DAQ card with 2 FPGAs, one for readout and one for the trigger.

- Aluminum tray closeouts and cores, with 75 μm thick carbon-composite face sheets.

- 11 x,y planes with 3.5% Pb foils

- 3 x,y planes with 25% Pb foils

Single completed tray, detectors top & bottom
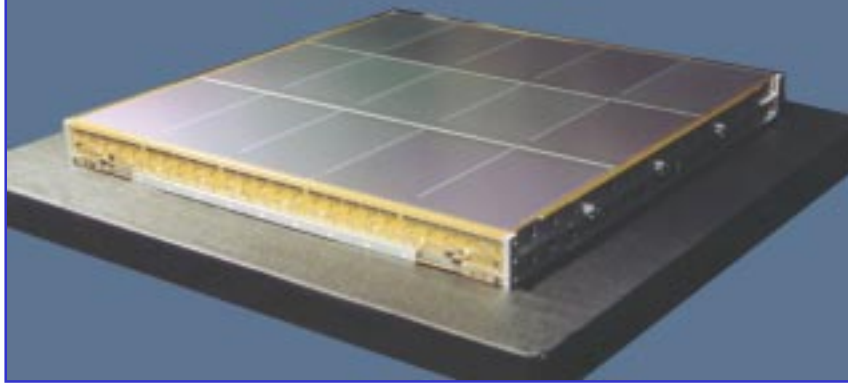
The completed beam-test tracker, with 2 side panels removed.

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Beam-Test Tracker QC

Some of the Testing Done:

- Detectors tested by manufacturer (IV and coupling cap) and visually scanned by us.

- IV curves taken again after edge bonding, wire bonding, and before mounting on the tray.

- Capacitance measured on an automatic probe station for each strip after wire bonding to detect broken caps, broken metal, missing wire bonds, and shorts. *Only 18 bad strips found and isolated by removing wire bonds.*

- ICs thoroughly tested on the wafer by an automatic probe station.

- Hybrids tested and burned in before mounting on trays.

- The result is only a handful of dead or noisy channels, plus one noisy ladder (unknown reason).

Setup used to test 8 trays at a time with cosmic-rays and the actual DAQ. The trays are still in protective plastic enclosures and have aluminum handles attached to the sides.

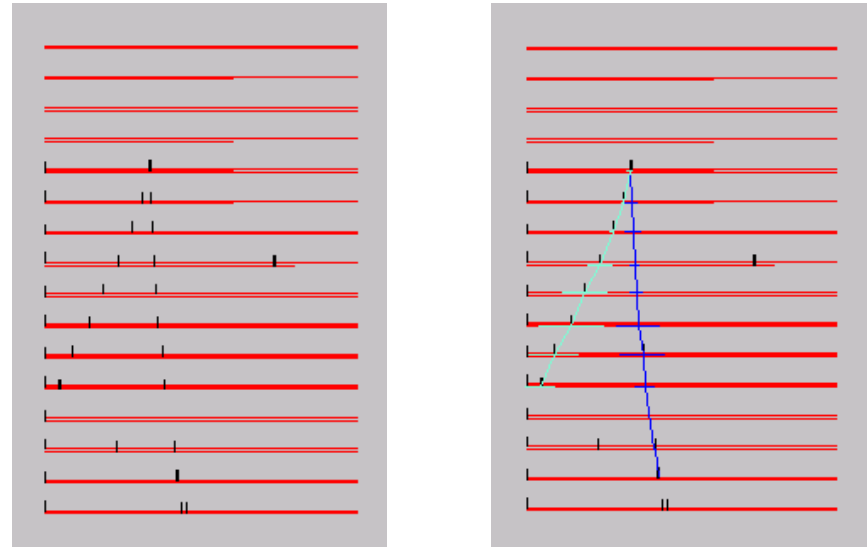*GLAST*

Beam-Test Tracker Performance

No real analysis of the PSF for photon conversions is done yet, but good progress has been made on putting together the reconstruction software.

Data were taken for
– cosmic rays
– positrons at various energies
– tagged photons
– mixture of hadrons and positrons

A single photon conversion from beam-test data, before and after track finding and fitting with a Kalman-Filter algorithm.
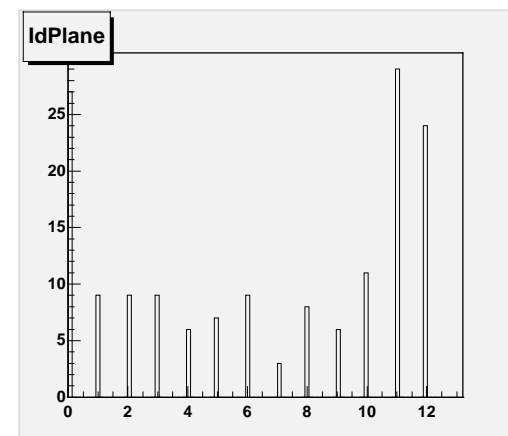
The tracker ran reliably for 2 months with no changed needed in threshold settings or masks (no channels were masked) and no change in leakage.

Distribution of photon-conversions per tracker plane.

The self trigger worked well, but most data were taken with a beam trigger.

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Tracker Tower Alignment

- Tray-to-tray alignment has been looked at in cosmic-ray and positron data and appears to be within our goal of 50 micron rms.

- More analysis is in progress with a position scan of hadron data, to get uniform coverage and enough sensitivity to study rotations.

sigma=60 microns
mean=-18 microns

Residual on Layer 12x

sigma=66 microns
mean=-25 microns

Residual on Layer 12y
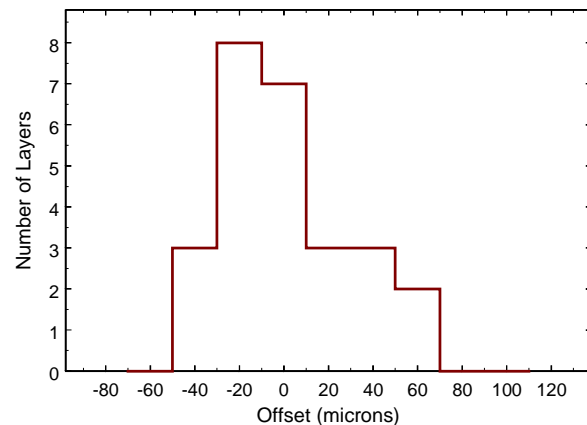
Offsets from 26 of the 32 layers, as obtained from 20-GeV positrons.
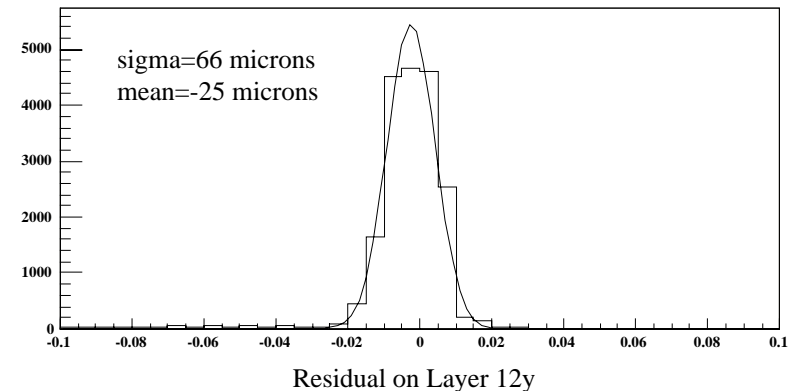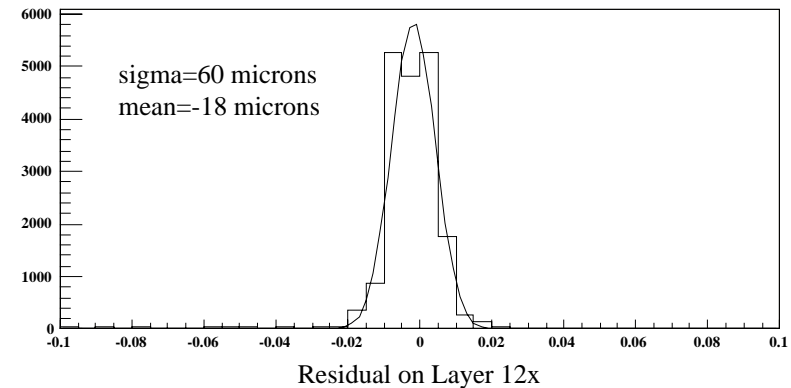
Residual distributions on Layer 12, from fitting 20-GeV positron tracks to straight lines in layers above and below. The width is as expected for 194 μm pitch.

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Tracker Noise and Efficiency

- Noise occupancy was obtained by inducing triggers, followed by readout, at random times.
- Hit efficiency was measured using single electron tracks and cosmic muons.
- The requirements were met: 99% efficiency with $<<10^{-4}$ noise occupancy.
- However, this was with no live trigger during the readout. We are now measuring occupancy during digital activity.
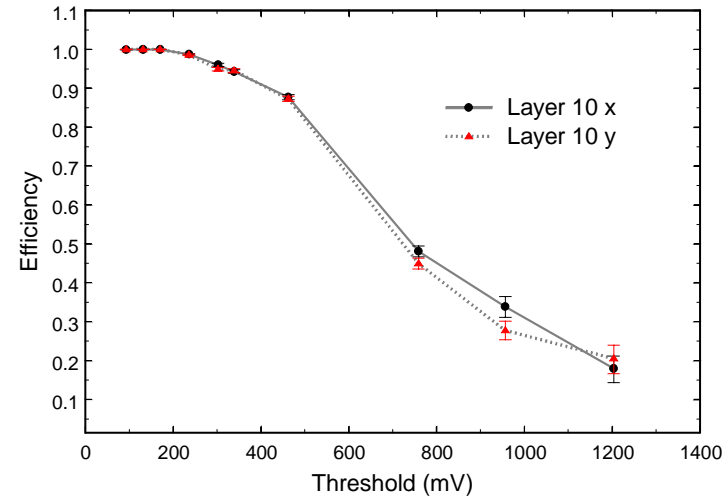
Hit efficiency versus threshold for 5 GeV positrons.
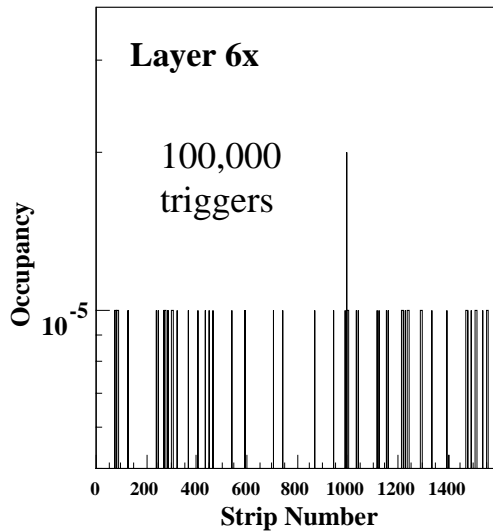
Noise occupancy and hit efficiency for Layer 6x, using in both cases a threshold of 170 mV. No channels were masked.

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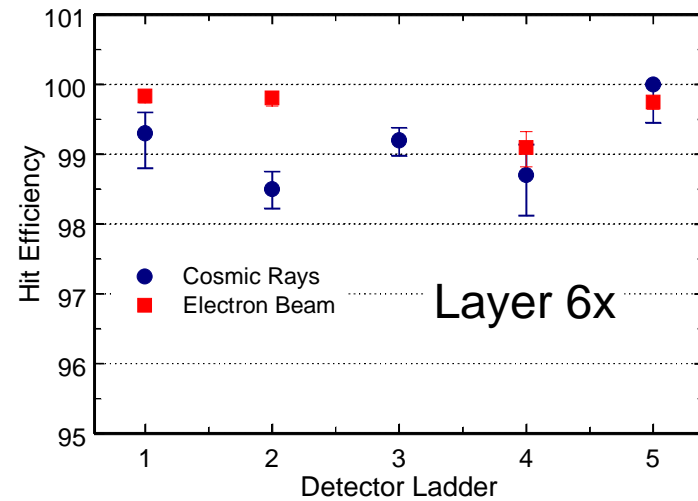
Schedule

Formulation Phase: through 9/30/01

- Design must be finalized
- Culminates in Instrument PDR
- Si procurement begins 9/1/00! Start building ladders asap
- Balloon test, April 01?

Implementation Phase:

- Build engineering model before CDR
- Instrument CDR on 7/1/02
- Start tray assembly on 2/10/03
- 1st tower done by 8/20/03
- Final tower done by 1/14/04

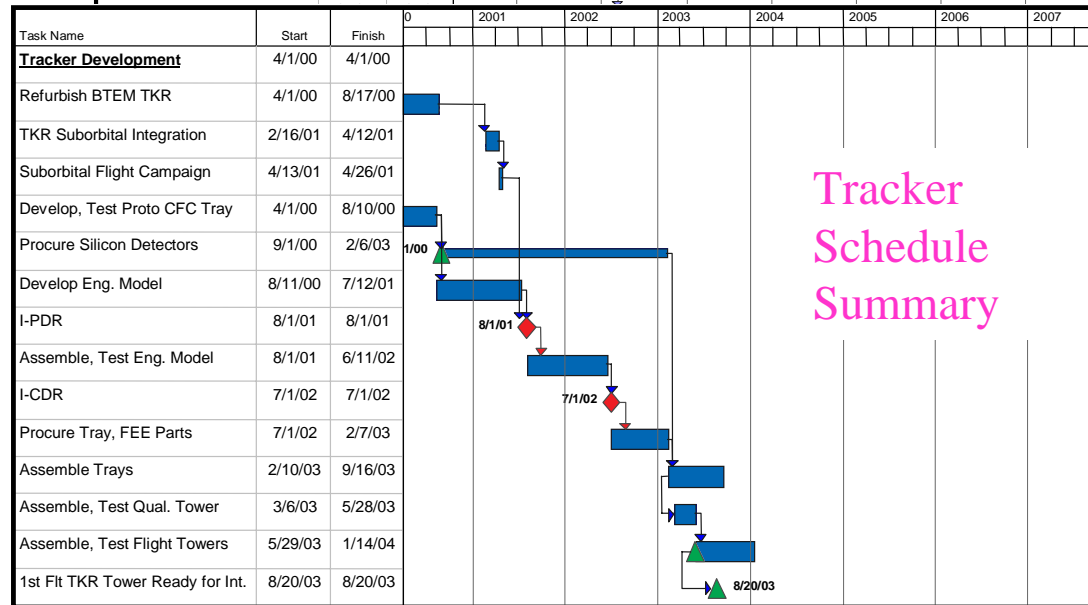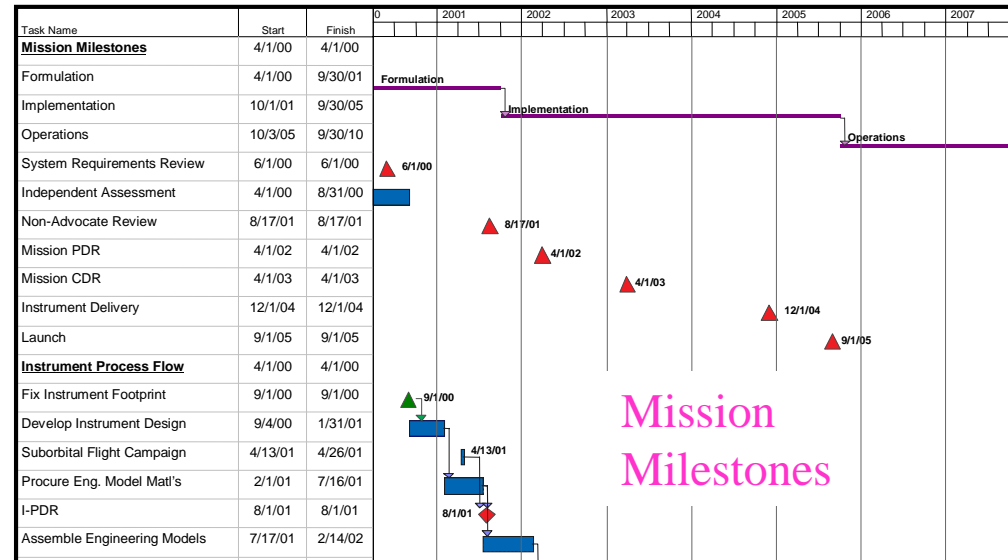| Task Name	Start	Finish
Mission Milestones	4/1/00	4/1/00
Formulation	4/1/00	9/30/01
Implementation	10/1/01	9/30/05
Operations	10/3/05	9/30/10
System Requirements Review	6/1/00	6/1/00
Independent Assessment	4/1/00	8/31/00
Non-Advocate Review	8/17/01	8/17/01
Mission PDR	4/1/02	4/1/02
Mission CDR	4/1/03	4/1/03
Instrument Delivery	12/1/04	12/1/04
Launch	9/1/05	9/1/05
Instrument Process Flow	4/1/00	4/1/00
Fix Instrument Footprint	9/1/00	9/1/00
Develop Instrument Design	9/4/00	1/31/01
Suborbital Flight Campaign	4/13/01	4/26/01
Procure Eng. Model Matl's	2/1/01	7/16/01
I-PDR	8/1/01	8/1/01
Assemble Engineering Models	7/17/01	2/14/02

Mission Milestones

Task Name	Start	Finish
Tracker Development	4/1/00	4/1/00
Refurbish BTEM TKR	4/1/00	8/17/00
TKR Suborbital Integration	2/16/01	4/12/01
Suborbital Flight Campaign	4/13/01	4/26/01
Develop, Test Proto CFC Tray	4/1/00	8/10/00
Procure Silicon Detectors	9/1/00	2/6/03
Develop Eng. Model	8/11/00	7/12/01
I-PDR	8/1/01	8/1/01
Assemble, Test Eng. Model	8/1/01	6/11/02
I-CDR	7/1/02	7/1/02
Procure Tray, FEE Parts	7/1/02	2/7/03
Assemble Trays	2/10/03	9/16/03
Assemble, Test Qual. Tower	3/6/03	5/28/03
Assemble, Test Flight Towers	5/29/03	1/14/04
1st Flt TKR Tower Ready for Int.	8/20/03	8/20/03

Tracker Schedule Summary

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Summary of Work in Progress

- Settle on final parameters: size, pitch, number of layers, Pb converter distribution.
- Budgets, schedules, and system engineering.
- Construction of fabrication facilities at SLAC.
- Carbon-composite tray structure design and prototyping.
- Review tracker electronics and then redo all of the designs:
  - Front-end readout chip
  - Readout controller chip
  - Hybrid, including the new scheme to bend around the corner
  - Bias circuit
  - Kapton cables

- Prefabrication runs of the detectors.
- Long term testing of detectors, including effects of adhesives.
- Thermal testing of detector ladders on face sheets + Pb (strain and IV).
- Further development of tray assembly procedures
  - Ladder construction & encapsulation
  - Ladder placement
  - Hybrid attachment and encapsulation
  - QC & documentation (ISO9000)
- Analysis of beam-test data.
- Further testing of the beam-test tracker electronics.
- Reconstruction and Monte-Carlo software development.
- Balloon test preparations.

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