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- Simulations.
- Tray Design and Construction.
- Detector Mounting and Wire Bonding.
- Detector Fabrication and Testing.
- Readout Electronics Status.
- Schedule for Prototype Tower.





Background Simulations

Bill Atwood has repeated the GLAST background rejection analysis using the current baseline design.

GLAST was zenith pointing.

The CREME'97 program was used to generate cosmic rays, with a uniform illumination down to 112°.

The first 50,000 events were used to determine a suitable cut on the ACD signals.

Then, 2×10^6 events were generated and kept for analysis only if

- there was ≥ 1 track, and the
- distance to the center of the nearest hit tile ≥30 cm.

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Track Projections into Veto System



Distance of closest approach to the center of the nearest hit ACD tile.

Background Rejection, ACD

Track Projections into the Veto System



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Background Rejection, Calorimeter

Track-Calorimeter Tracker Match to Cal. Energy Centriod Tracker Match to Cal. Energy Centriod Matching 666 100 100 MeV Gammas 100 MeV Gammas 200 On Axis 50 All Sky Events / 0.5 bin Events / 0.5 bin 100 Eff. > 99% Eff. = 87% Require that each found track 20 points at an energy centroid in 24 10 the CsI Calorimeter. Normalize this distance so as to be independent of the 5 10 15 20 Energy Normized DOCA (cm) 25 5 10 15 20 Energy Normized DOCA (cm) 25 measured energy. Tracker Match to Cal. Energy Centriod 200 100 Cosmic Rays Results: > 87% (99%) of the gammas are kept 60 All Sky Events / 0.5 bin Eff. = 1/14.4 = 7% cosmics are rejected 14:1 20 Signal : Noise $\sim 1.8:1$

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5 10 15 20 Energy Normized DOCA (cm)

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Background Rejection, Calorimeter



The measured energy + γ trajectory predicts the number of hit CsI Xtals. For cosmic rays this works poorly.

Results: 95-100% gammas kept; Only 60% of cosmics kept.

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Background Rejection, Tracker

The number of hits per layer can distinguish e^+e^- pairs from single cosmic ray tracks.



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Background Rejection, Results

Out of 2×10^6 cosmic rays generated, only 2 survive.

The signal-to-noise after all cuts is 49 : 1.

The two remaining background events share the following characteristics:

- 1) They enter GLAST horizontally and therefore leave little evidence of a "track".
- 2) Side ACD tiles fire, but no track points back to them.



Example Background Event.

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Tray Design





At the last mechanical TIM, the Hytec modifications to the tray design were adopted:

- Corner posts with compression cables and alignment pins.
- Carbon thermal panels covering the entire surface of all 4 sides.

The first trays for the prototype tower will be constructed from

- Machined aluminum closeouts.
- Carbon foam core.
- Carbon composite face sheets.

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- Work is in progress to understand how to assemble the detectors and electronics onto a tray.
- This tray will be assembled with currently available prototypes and dummy detectors and wire-bonded.
- Sequence:
 - Completely load, wire bond, test, and burn in the hybrid.
 - Glue the kapton to the tray and hybid.
 - Load the detectors and complete the wire bonding.
 - Bend around the corner.

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First SLAC prototype tray, with Pb foils glued on top of the face sheet. The UCSC gluing jig, for the kapton and readout electronics, is bolted onto the tray.





Tray Assembly

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Detector Mounting and Wire Bonding

New concept under study: edge glue 5 detectors into a ladder, wire bond, test, and pot before mounting onto a tray.

- More manageable assembly for working in the wire bonder.
- Simple straight-edge alignment of detectors within a ladder.
- Only fully tested ladders are glued onto a tray.
- Only 5 elements (rather than 25) need to be aligned onto the tray.
- It may eventually be possible to obtain finished ladders from a commercial vendor, possibly with TAB rather than wire bonding.

Status:

- SLAC is preparing a jig for gluing and wire bonding of the ladders.
- UCSC is testing the gluing, wirebonding, potting procedure with some mechanical samples.

Issues:

- What glues should be used? (UV curing?)
- What potting compound should be used?
- Can detectors be removed from the ladder if damaged?
- Testing of glues in contact with Si

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Wire Bonding

• Wire bonding at Promex last summer caused a lot of damage to our beam test module.

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- A large-area automatic bonder has been acquired at UCSC.
- Learning process for bonding detectors:
 - 3 beam test detectors were bonded together.
 - 5 GLAST detectors were bonded together and to kapton in a fully functional ladder.
- "Dummy" detectors are needed in order to increase our experience:
 - Finish the remaining old dummies.
 - Purchase Hamamatsu rejects.



The large-area automated wire bonder at UCSC.



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Wire Bonding

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Problems

- If the wire is lost, the wedge may break a capacitor before the machine stops.
 - We need statistics on how often the wire breaks.
 - The capacitor may break up to 30% of the time this occurs.
- Optimum bonder settings have not yet been found:
 - 1st set of ~50 bonds in 5-detector module were too high power and broke some capacitors.
 - In the remaining bonds there were a lot of failures that required tedious rework.

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Detector Production and Testing

- 60 detectors, out the initial order of • 300, were tested at Hamamatsu and delivered to UCSC.
- Quality is very high ۲
 - 2 with a bad capacitor
 - 1 with open aluminum
 - overall dead channel rate less than 2 in 10,000.
- A few detectors have been completely characterized (capacitance, resistance, depletion voltage, etc.) at UCSC and meet all specifications.
- Concerns about the delivery rate of ۲ the remaining detectors.

- Dimensions of 56 detectors were measured at UCSC.
- Tolerances exceed specifications and indicate that alignment can be done using the mechanical edge.

Rotation of active area relative to cut edge.







Readout Electronics–Front-End Chip

- First prototype: fully functional, except that the command decoder needs an external reset before loading the configuration register.
- Second prototype, due this week: we fixed the command decoder bug, but the main objective was to obtain 25 good chips for one complete readout section, to instrument the first prototype tray.
- Third prototype: work in progress to reduce coupling of the digital activity into the amplifiers. Should be in hand in mid September.



Layout of the GTFE64 Chip

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Front-End Chip, Performance



Noise Performance:

- Ladder of five 6.4 cm detectors and five GTFE64 chips.
- Measured from the observed noise occupancy versus threshold.
- To give a varying load, not all channels had all five detectors bonded.
- (Assume C=1.2 pF/cm)
- Roughly 1400 *e* noise (0.044 MIP) for a full-length channel.



Preliminary data from June 12, 1998. Outlying channels have not yet been investigated.

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Front-End Chip, Performance

- Threshold Matching:
 - Fix the threshold and scan the injected input charge to find the point where the efficiency for firing the comparator is 50%.
 - The measured dispersion of 0.07 fC is comfortably less than the rms noise charge of about 0.22 fC (ENC).





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Front-End Chip, Work in Progress

- Amplifiers and discriminators respond when the clock for the readout sequence is started and halted.
 - Modify layout to bring the digital ground out separately from the substrate.
 - Improve shielding around the digital sections.
 - If that does not solve the problem, then the trigger will have to be disabled for a short time at the beginning and end of each readout sequence.

- Fast-OR inputs at the beginning of the 25-chip chain are not biased.
 - Add logic to turn off those inputs for chip addresses 0 and 24.
- Calibration system is too noisy for detailed amplifier noise measurements.
 - Add LVDS differential input for a quiet external pulse, to be used only in bench testing.

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Readout Controller Chip

- The GTRC chip design is complete, and 25 copies of the first prototype are due to arrive this week.
- Only one small bug is known at this time—the external RESET works oppositely from that of the GTFE64 chip!
- This version will be used in the first prototype tray, assuming that it functions sufficiently well.
- A full-length hybrid PCB is in fab for testing the GTRC and GTFE64 chips together.



Cadence layout of the GLAST Tracker Readout Controller chip (GTRC). The left half is logic made from standard cells, while the right half is memory for buffering.

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Readout Electronics Testing

- Test stations are being constructed for the GTFE64 and GTRC chips.
 - Probe cards have been made for both chips.
 - An automated probe station has been acquired, so that wafers can be quickly tested before dicing.
 - Work is in progress to interface a test system to the probe card and write sequences of test vectors.

- Completed hybrids, with 25
 GTFE64 chips and 2 GTRC
 chips, will be tested and burned
 in before gluing to the kapton
 flex circuit.
 - Should most of the bonds be potted at this point?
 - Slight complication that a few of the chip-to-chip bonds (for Fast-OR) cannot be made until the wire bonding to the kapton is done.



Schedule for the Prototype Tracker

The First Complete Tray

- June 12—first tests of a full ladder of detectors.
- July 15 —first tests of a full front-end readout section.
- July 29 —all parts in hand for building the first tray.
- Aug. 31 —detectors and electronics mounted on one side of the first tray.

This first tray will be used to validate the design and assembly procedures, to test the detectors and electronics, to carry out vibration and thermal testing, and to report on in the ATD basic contract report at year's end.

Tracker for the Tower

- July 24 —order remaining silicon-strip detectors.
- Aug. 26 —order materials and components for the 17 trays.
- Sept. 29 —submit production run of the front-end chips.
- Nov. 18 —begin production tray assembly.
- Mar. 26, 99 —trays completed.
- Aug. 27, 99 —begin tower assembly.

(The date for completion of the trays could slip several months with no problem if the August date for tower assembly is correct.)