# The GLAST Silicon-Strip Tracker
## Detectors and Electronics

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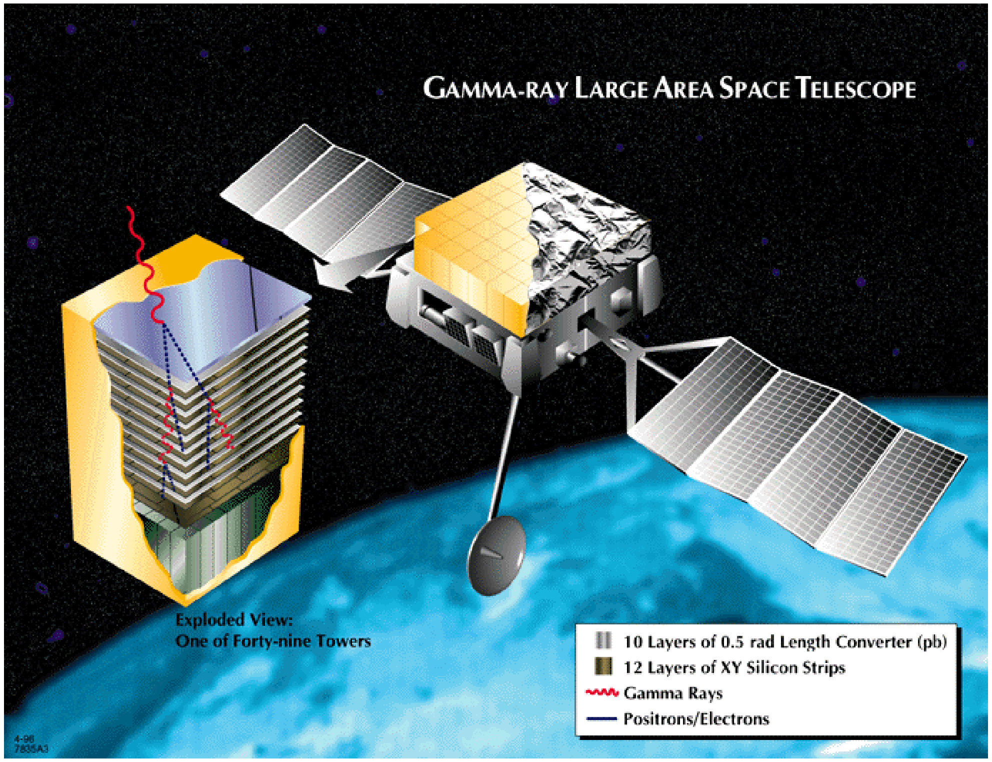
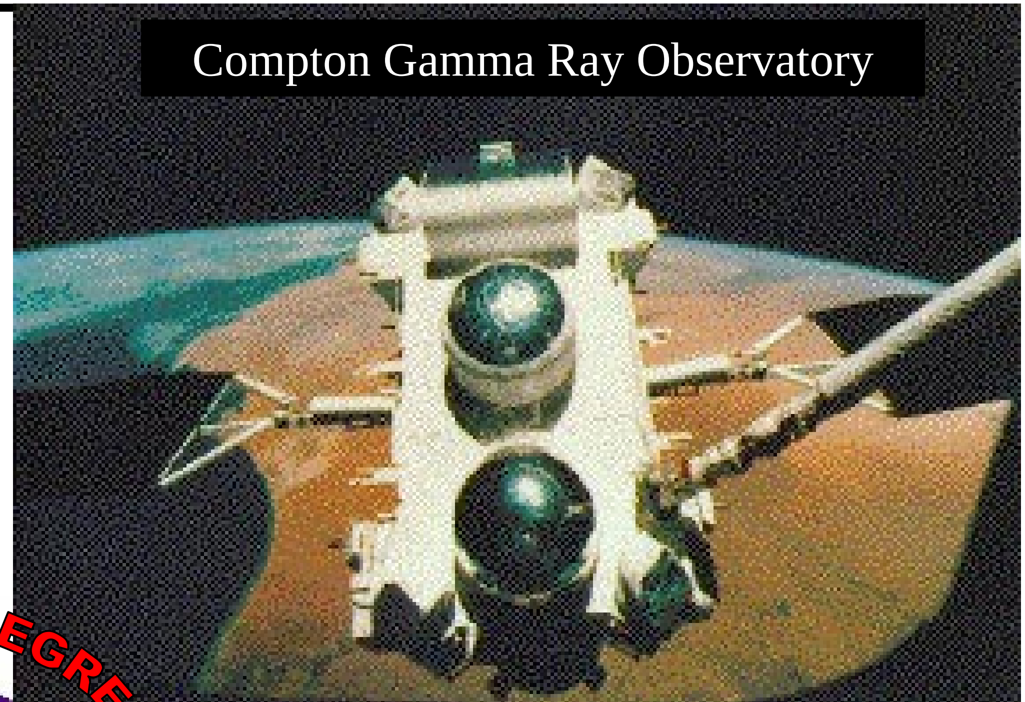
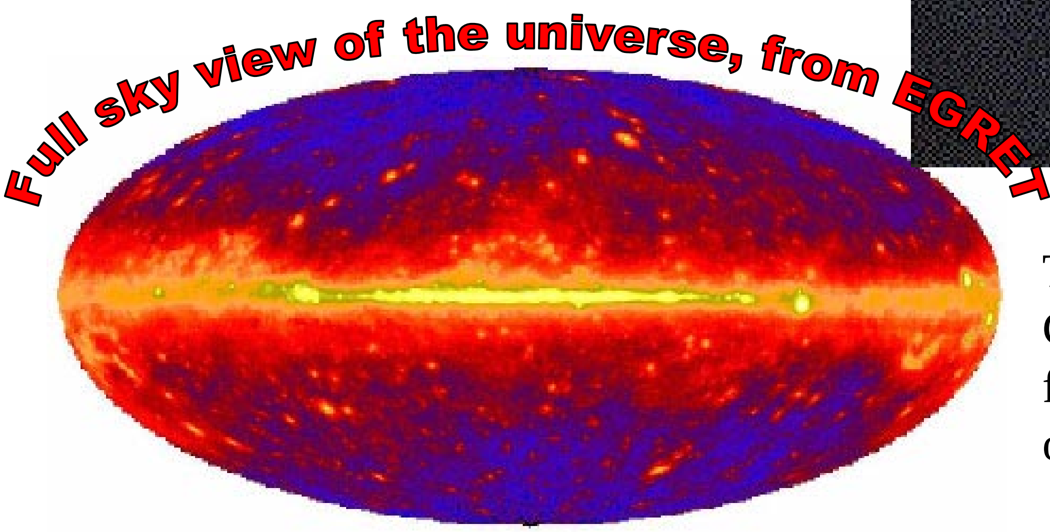
- Introduction to GLAST.
- GLAST Tracker Electronics Requirements.
- Detectors.
- Amplifiers and Discriminators.
- 1997 Beam Test.
- Readout Architecture and ASIC development.
- Mechanical Issues.
- Conclusions.



# Pair Conversion Telescopes

- We detect gamma-rays in the energy range 10 MeV to tens of GeV by tracking and measuring the pair-conversion electrons.
- This energy range is inaccessible from the ground.



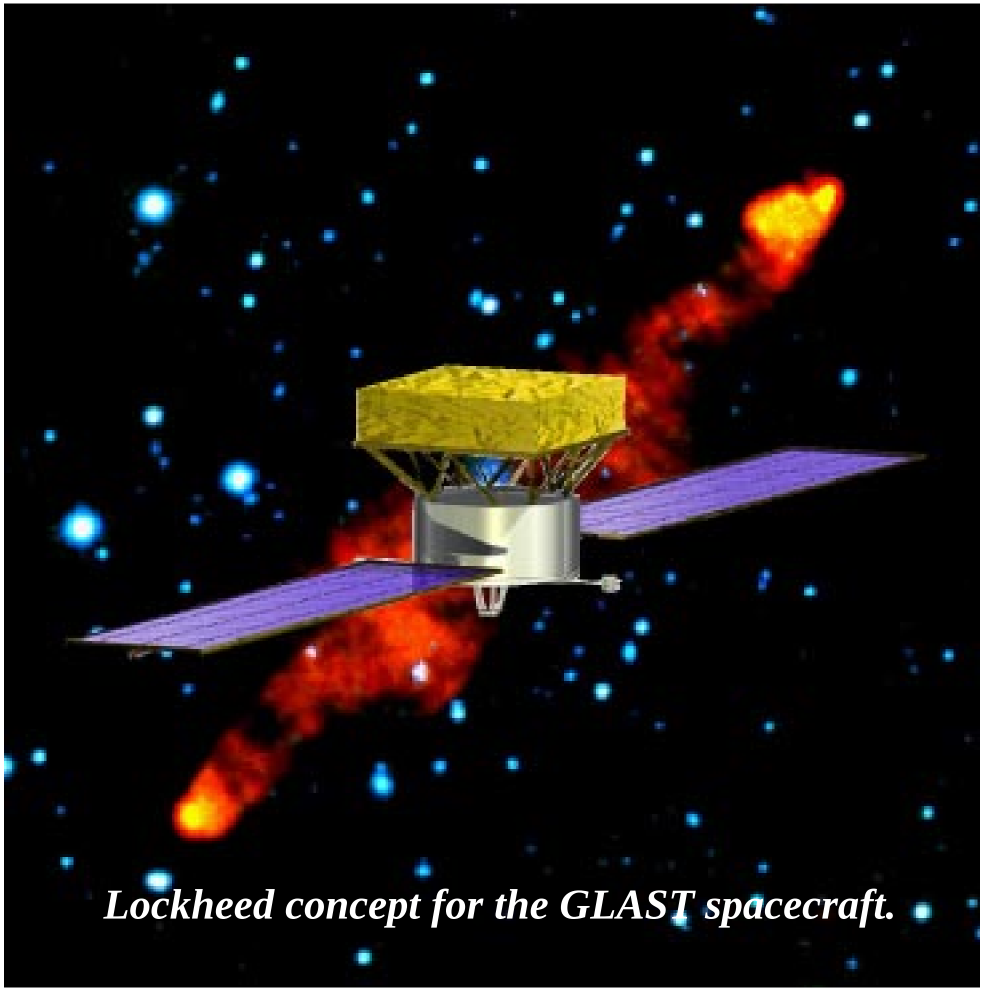




The present EGRET experiment on the CGRO satellite has revolutionized this field of astrophysics but has nearly run out of *spark-chamber* gas.

# The Next Generation

- The use of 1990's tracking technology can produce factors of 10 to 100 improvement over EGRET's sensitivity while still keeping within a moderate budget.
- Self-triggering tracking allows one to dispense with the time-of-flight system—the resulting flat instrument provides a nearly full-sky field of view.

GLAST will provide nearly continuous monitoring of the characteristically transient sources of the gamma-ray sky.


*Lockheed concept for the GLAST spacecraft.*

# Why Silicon-Strip Detectors?

- Mature, proven, reliable, and robust technology.
- The ultimate vertex-detector resolution is not needed, but the relatively fine pitch provides excellent tracking for optimal
  - angular resolution,
  - 2-track separation,
  - and background rejection.
- High efficiency, with very low noise occupancy.
- No consumables, such as gas.
- Relatively low voltage.
- Fast—negligible dead time, self triggering.
- Cost—small part of the overall mission price, even for 100 sq m.

Alternative tracking technologies proposed by other groups:

- Gas Microstrips:
  - Tall, narrow cells track efficiently only at 90° incidence, at best.
  - Not proven to be a reliable technology (crucial in space!).
- Scintillating fibers:
  - Photoelectron yield is marginal, even with 1 mm fibers.
  - Only viable readout system (image intensifier + CCD) is unwieldy, slow, and needs very high voltage.

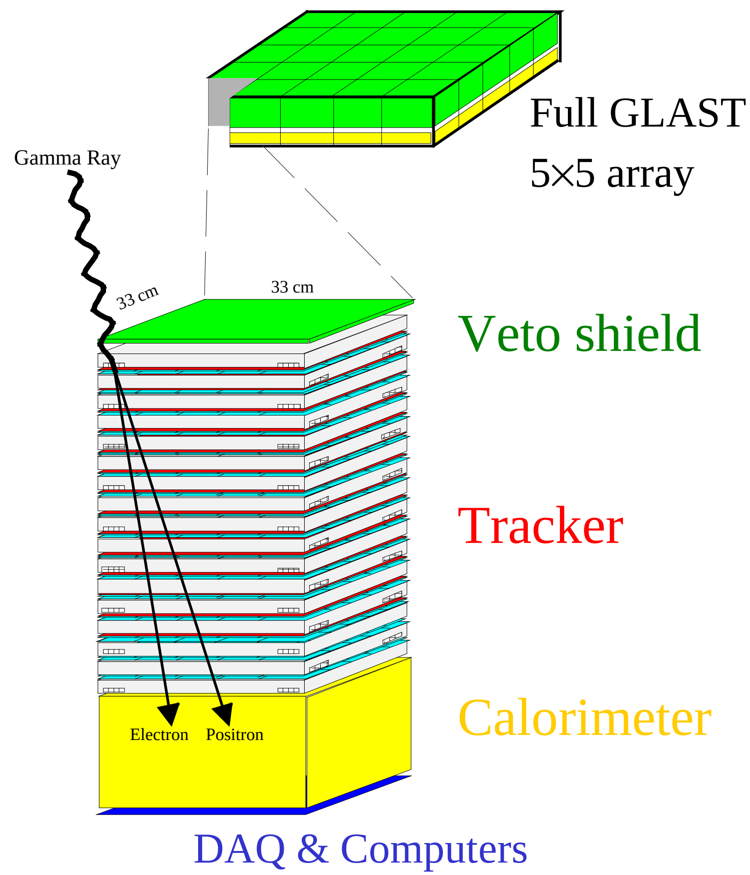
# The GLAST Instrument Concept

GLAST is an assembly of identical modules, each with a plastic scintillator veto shield, a silicon-strip tracker, and a cesium iodide calorimeter.

Each tracker module has 16 tracking layers, each with an *x,y* pair of single-sided silicon-strip detector planes. Each of the top 13 layers has a ~3.5% lead converter foil.

The current tracker baseline design calls for 32 cm square detector planes, each with a 5×5 array of 6.4-cm detectors.

GLAST Baseline Conceptual Design



# Electronics Requirements & Goals

Challenge: 1.3 million readout channels operating with high reliability in a space environment.

- Power less than ≈250 μW/channel, including amplifiers and digital readout.
- Low noise occupancy (<0.05%) and good threshold uniformity.
  - Expected detector loading is about 1.2 pF/cm × 32 cm = 38 pF.
  - Detector thickness is 400 μm, for about 5.3 fC/MIP.
- Microsecond peaking time for the amplifiers.
- Sufficient redundancy to be immune to single-point failures.
- Self triggering.
- Radiation hard to 10 kRad with latch-up immunity.
- <1% dead-time at a 10 kHz trigger rate.
- Sparse readout and data formatting close to the front end.

# GLAST Detectors

**1997 Beam Test**

- Hamamatsu Photonics
- AC coupled.
- Punch-through biasing.
- 236 μm strip pitch.
- 57 μm strip width.
- 500 μm thick.

Some measured properties:
Full depletion: ~140 V.
Punch-through voltage: ~9 V.
Strip Capacitance: ~1.2 pF/cm.
Radiation damage: ~15 nA/strip after 10 kRad dose at 20°C.

**Prototype Tower Module**

(under construction)

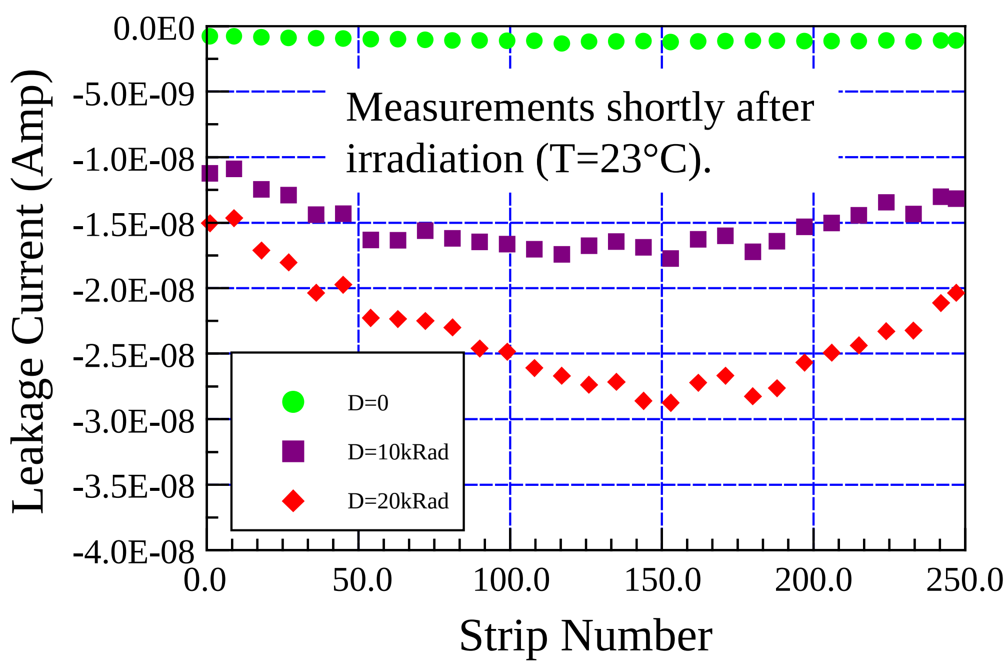
- Hamamatsu Photonics
- AC coupled.
- Polysilicon biasing (30-80 MΩ).
- 194 μm strip pitch.
- 50 μm strip width.
- 400 μm thick.

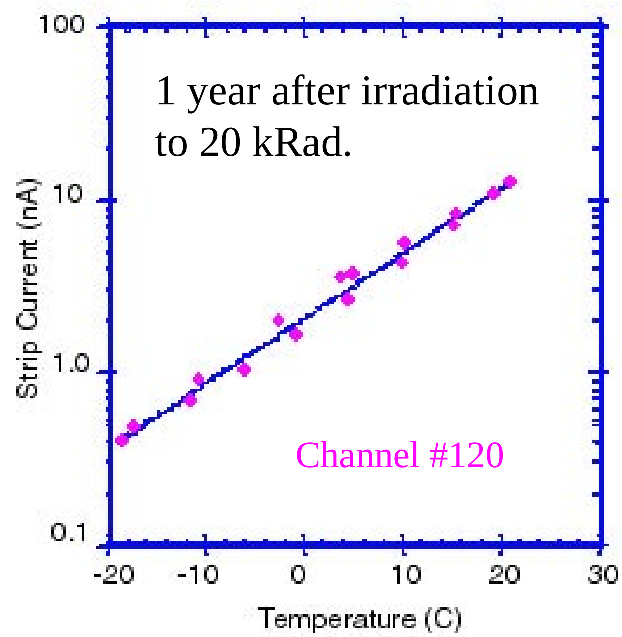
Five detectors will be connected in series, to give 32-cm strips, each with ~38 pF capacitance.

# Beam Test Detectors

The expected radiation dose for GLAST is relatively small (5 to 10 kRad), but measured effects on our prototype detectors indicate that some caution is needed.

- The new detector design employs polysilicon bias resistors, rather than punch-through structures.
- The amplifier time constant will be kept below about 1.5 μs.

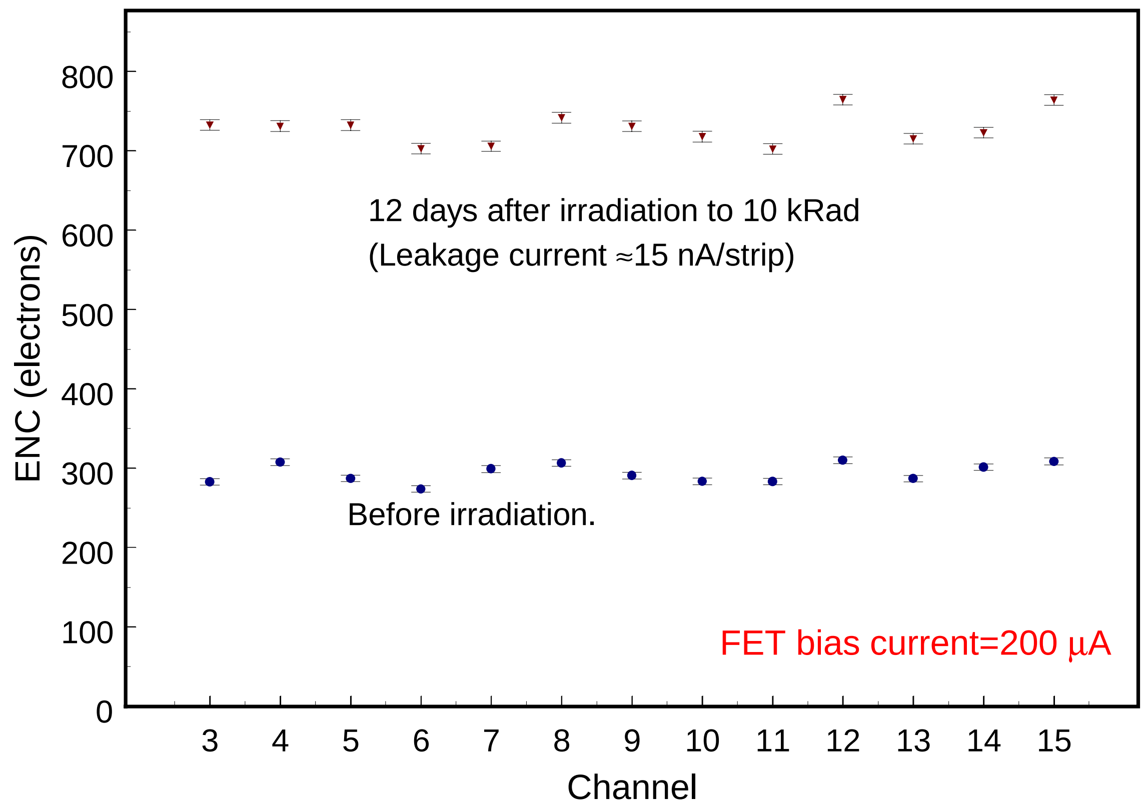


# Beam Test Detectors

The effect of radiation damage on noise was measured directly using a 16-channel prototype chip connected to a prototype detector.

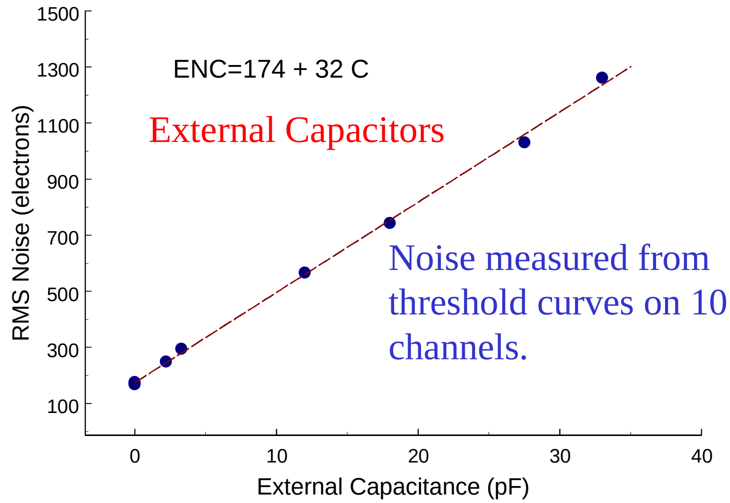
The measured noise is about 25% greater than what is naïvely expected from shot noise due to the measured 15 nA leakage current.

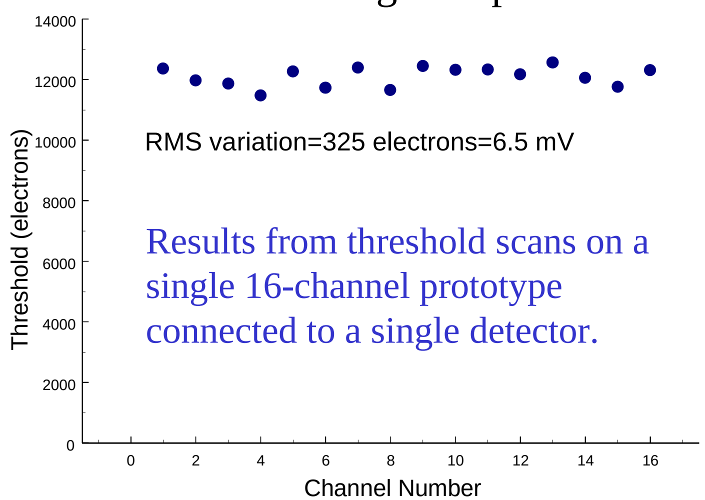


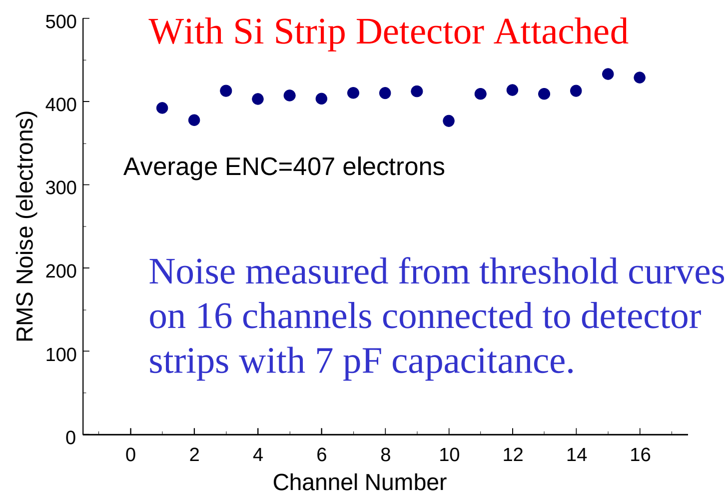
# Amplifiers and Discriminators

## 16-Channel Prototype

- Gain (shaper output): ≈150 mV/fC.
- Peaking time: ≈1.6 μs.
- Power consumption, including bias circuitry: 150 μW/channel
- Noise: ENC=174 + 32×C electrons, with C in pF.
- RMS threshold variation: typically 6 to 10 mV across a single chip.

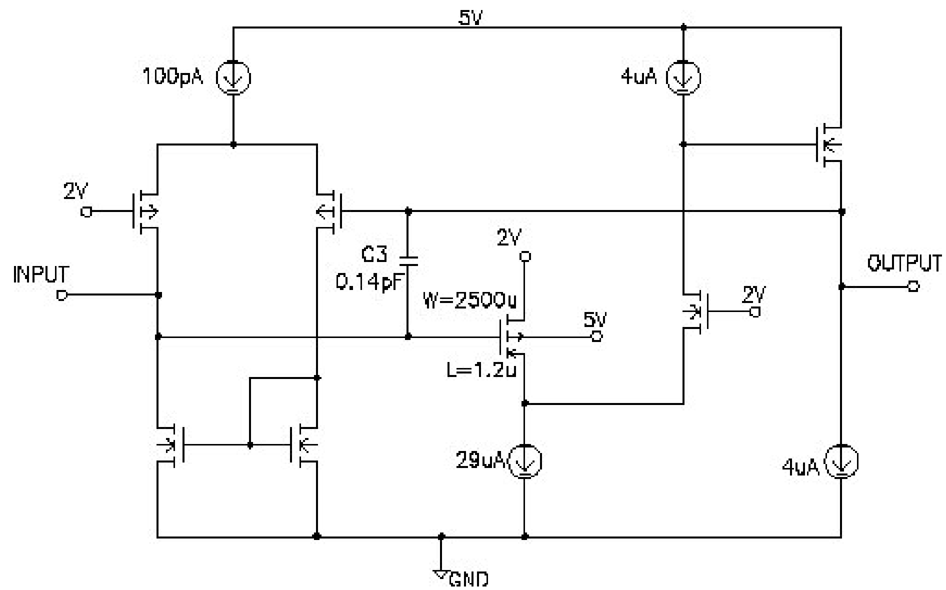


# Preamplifier Design

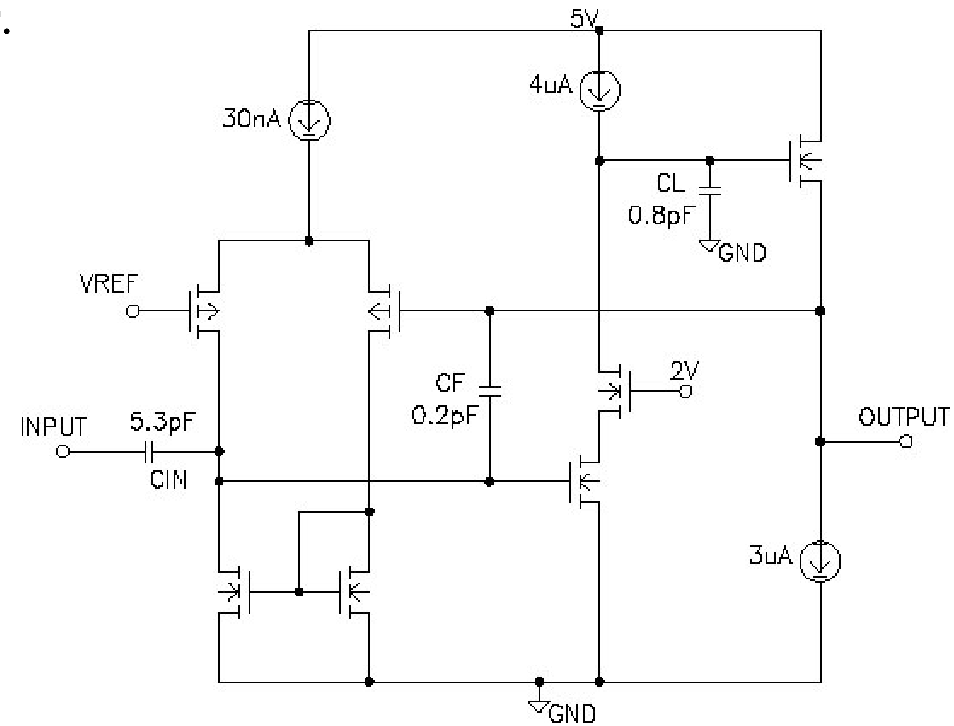
- Standard folded cascode amplifier with 2V bias for the front end, to save power.
- ≈25 μA bias current set by an external resistor.
- Slow differential amplifier stabilizes the bias point and provides a continuous reset.
- Input impedance ≈5 kΩ gives ≈200 ns time constant with GLAST 38 pF detector load.
- Open loop gain: 64 dB at 0 Hz
- Power: ≈90 μW




*Preamplifier schematic.*

# Shaping Amplifier Design

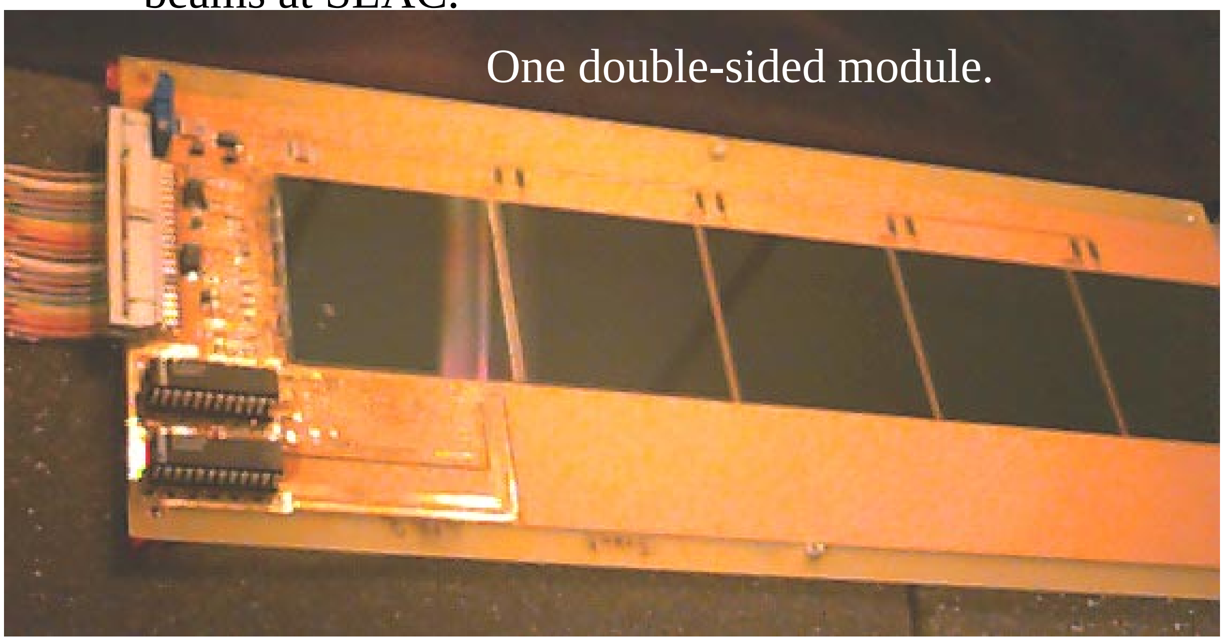
- AC coupling from the preamplifier.
- Conventional cascode amplifier with capacitive feedback.
- Slow differential amplifier in the feedback provides the “differentiation” function *and* stabilizes the output bias point. (Ref.: I. Kipnis, LBNL)
- Open loop gain: 62 dB at 0 Hz
- Voltage gain: ≈26
- Peaking time: ≈1.3 μs
- Pulse shape: reset current source makes a tail that is more linear than exponential, except at the lowest pulse heights.
- Power: ≈35 μW



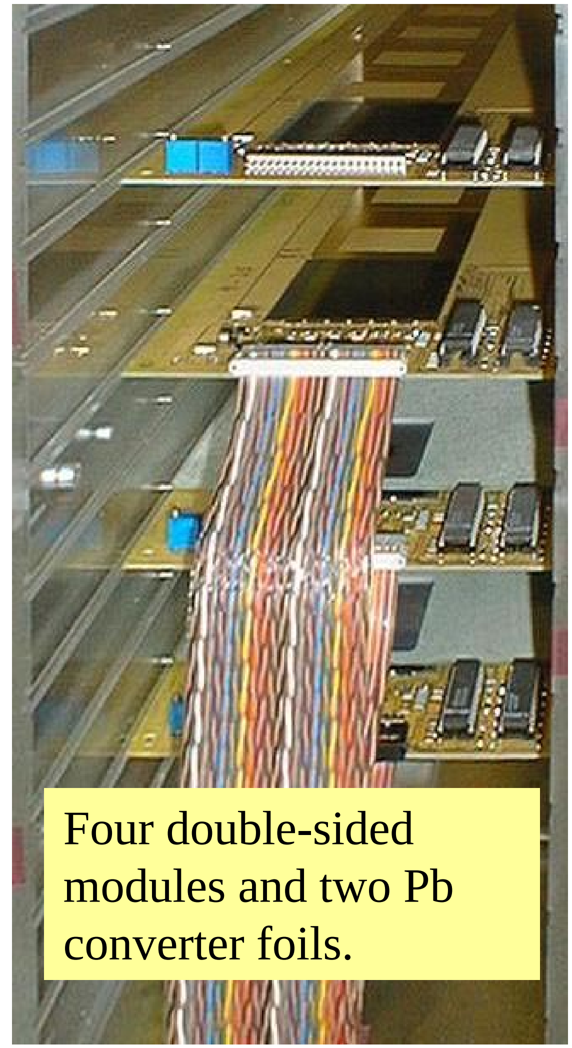

*Shaping Amplifier Schematic*

# October 1997 Beam Test

- 12 planes of detectors (6*x* and 6*y*) read out by 72 32-channel 2nd generation amplifier-discriminator chips. (Plus CsI calorimeter & anti-coinc. syst.)
- Interchangeable Pb converter foils of various thicknesses.
- One month of running in electron and tagged photon beams at SLAC.



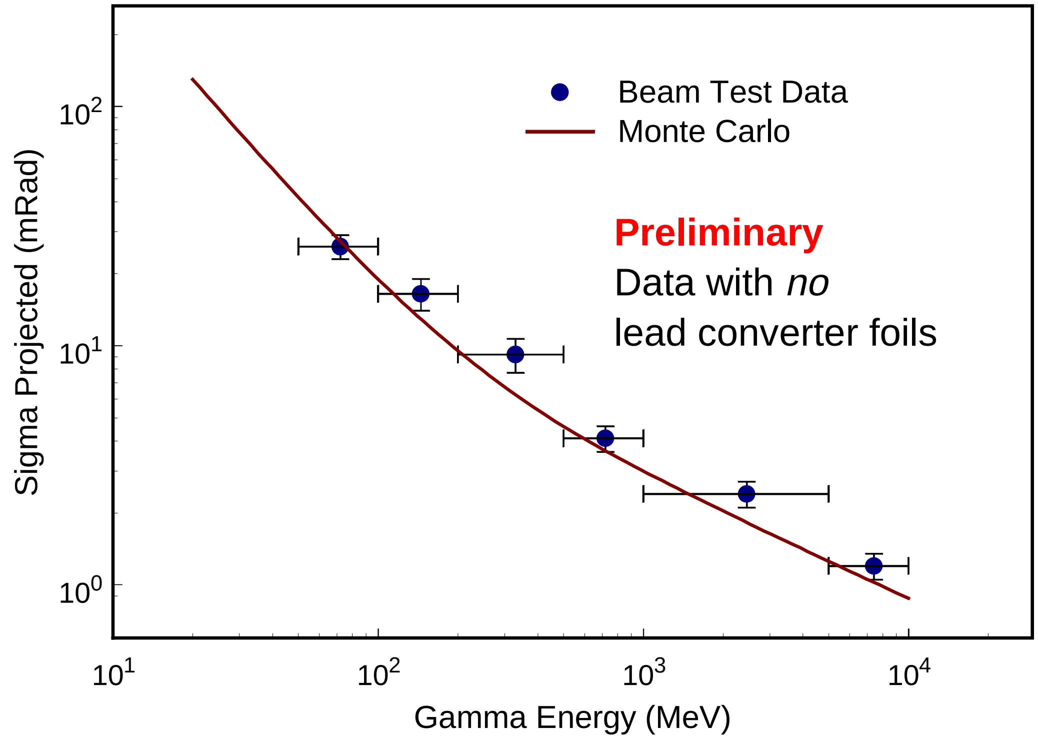
One double-sided module.

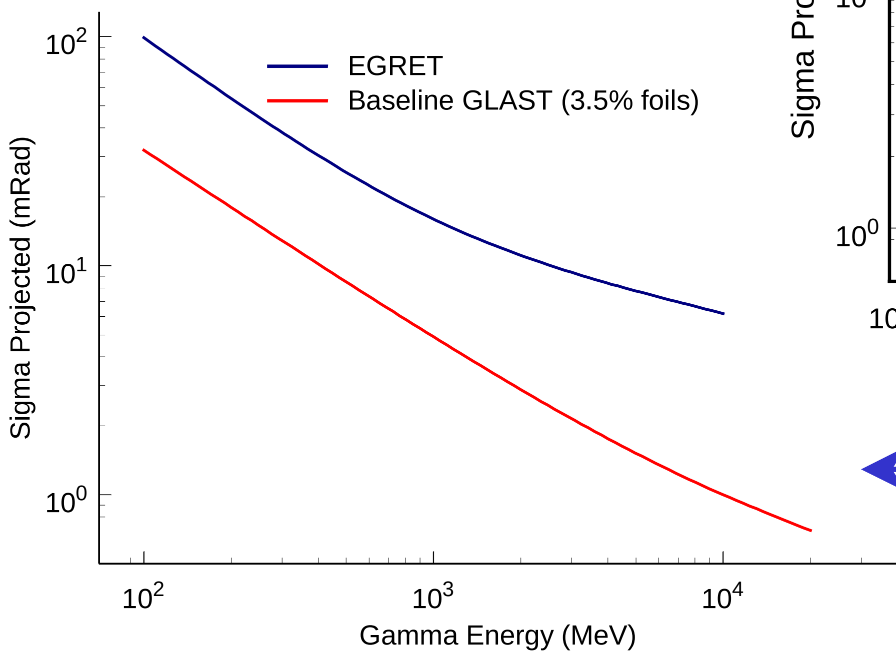


Four double-sided modules and two Pb converter foils.

# October 1997 Beam Test

Angular Resolution: a preliminary look at our data indicates good agreement with the Monte Carlo prediction.



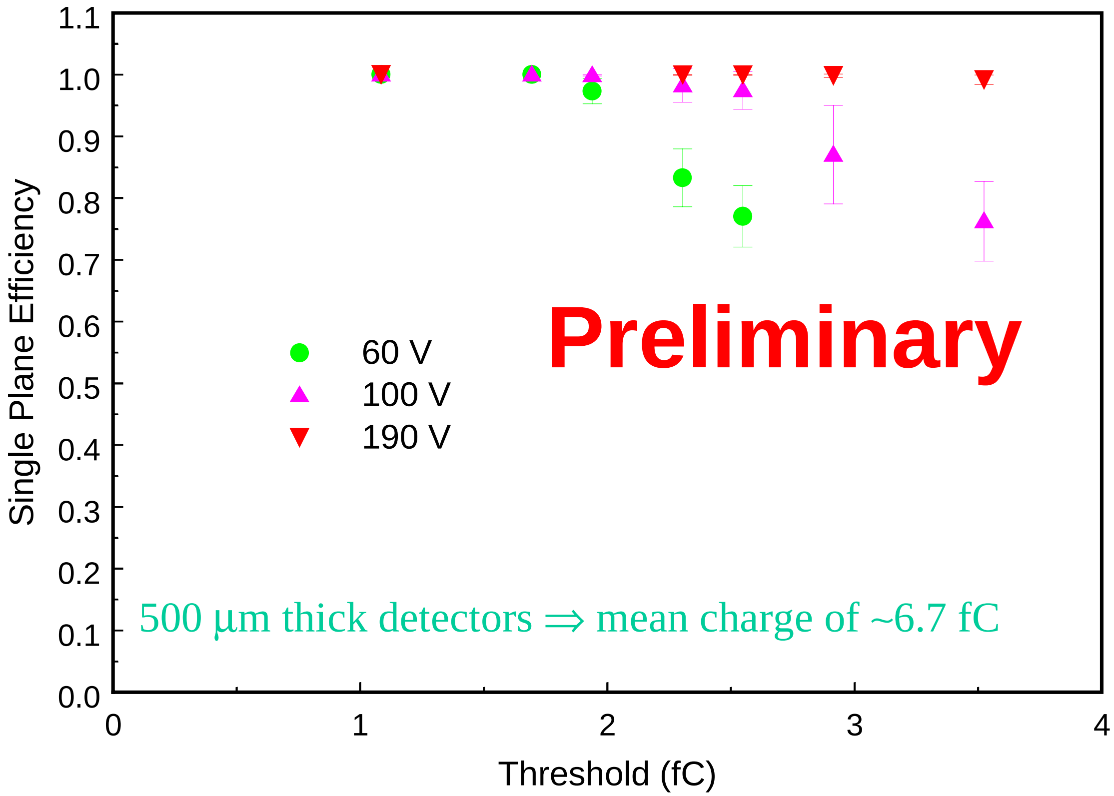




*Expected angular resolution in GLAST with 3.5% rad. length Pb converter foils.*

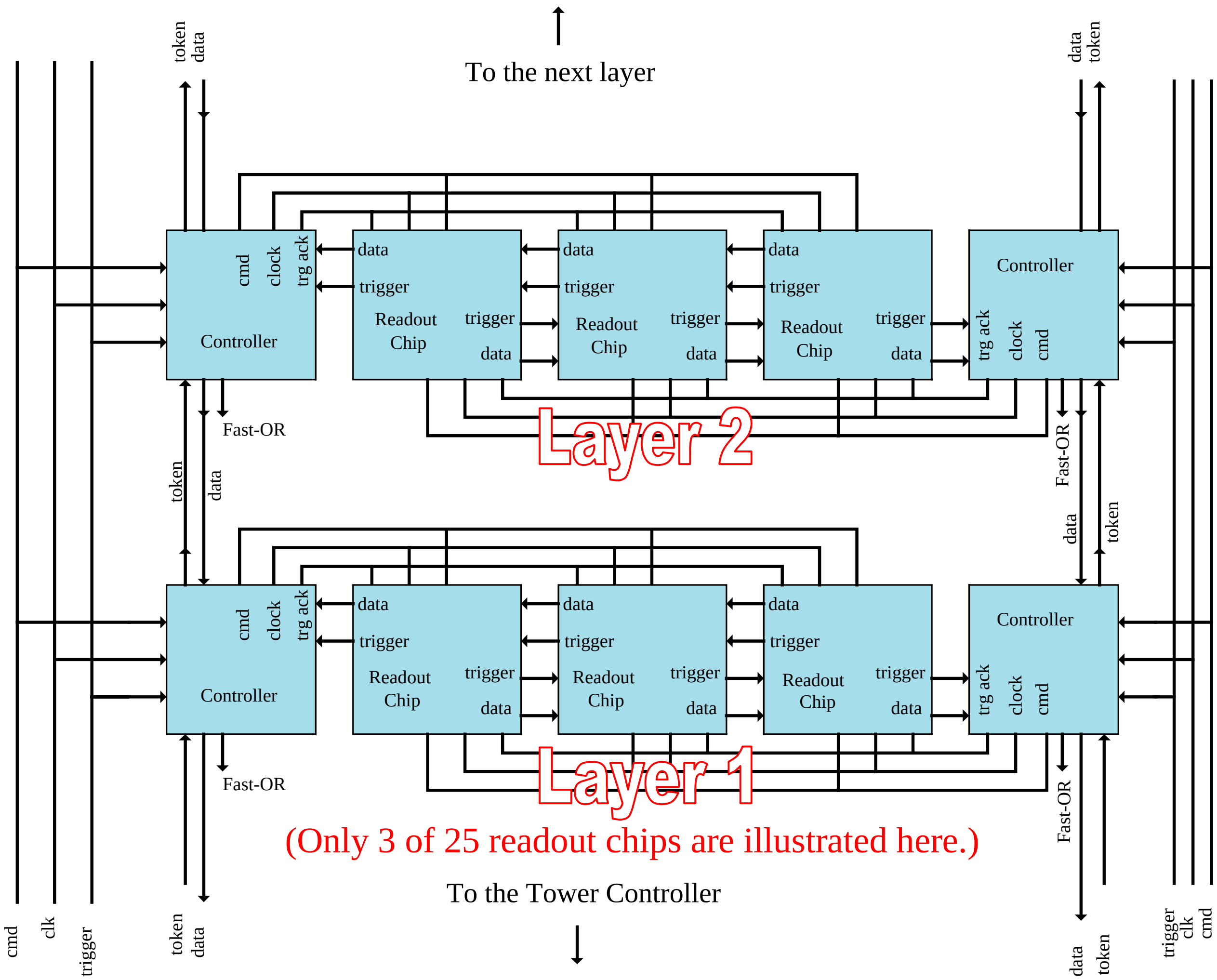
# October 1997 Beam Test

Several runs were taken at various detector bias voltages and various discriminator thresholds. With full depletion (V≥140 V), the efficiency is essentially 100% even well above the 1.5 fC threshold used during normal running.

- High energy electrons.
- CsI calorimeter was used to reject events with more than one electron.
- Normal incidence.
- Only detector planes with no dead or noisy channels were included.
- Tracks were required to have hits in planes both before and after the plane under test.



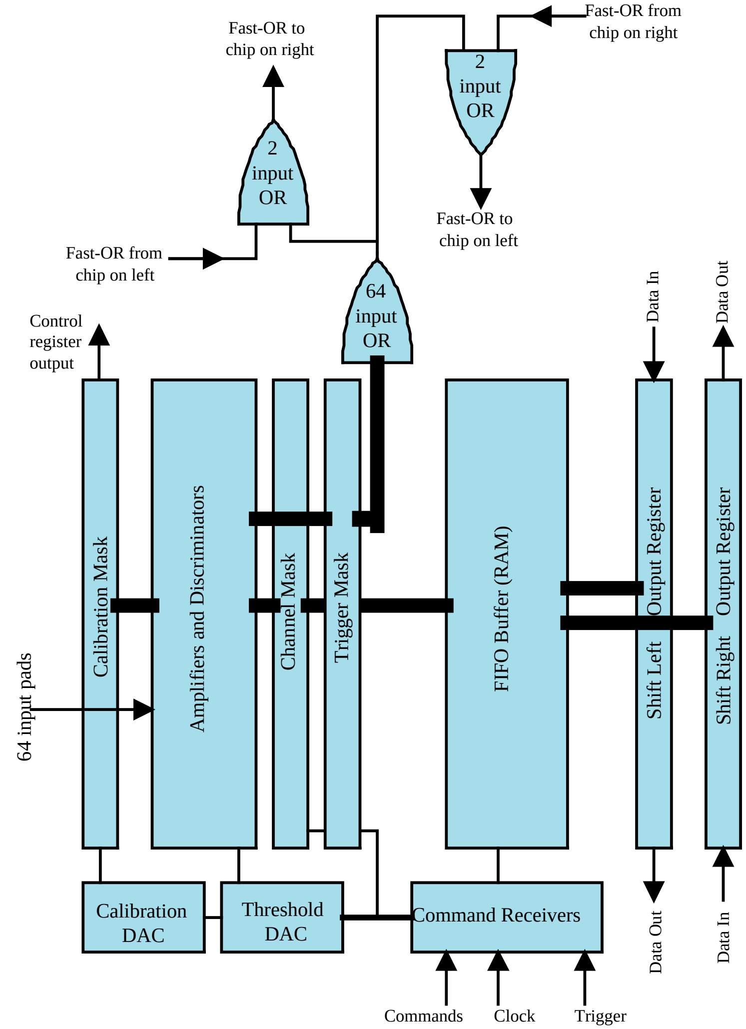
# Readout Architecture




- 25 readout chips per layer.
- Two redundant digital readout-controller chips on each layer, one at each end.
- Data and Fast-OR (for trigger) move from chip to chip in either direction.
- Any readout chip can be reprogrammed and controlled by either controller chip, so if any single chip is bad, all others can still be read.
- All communication and control is via serial lines.
- Formatted hit lists are read from the controller chips in a token-controlled daisy chain.

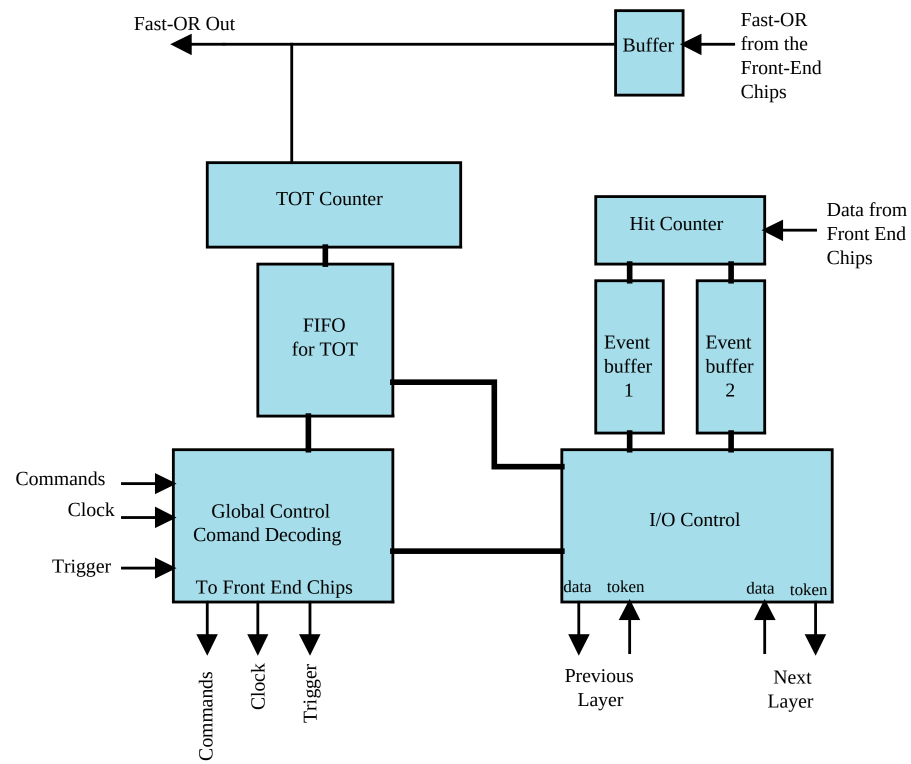
# Front-End Readout Chip

- The 64-channel chip submitted this week to MOSIS includes the following features:
  - Calibration mask, to select any subset of channels to be pulsed.
  - Two 7 bit DACs, for setting calibration and threshold levels.
  - Separate masks for data and trigger output (Fast-OR).
  - 8-deep FIFO event buffer.
  - Dual redundant serial command decoders.
  - Dual redundant output shift registers and trigger outputs.
  - Bypasses of output registers, to avoid clocking out data from empty chips.
  - External communication via low-voltage-swing differential signals.



# Readout Controller Chip

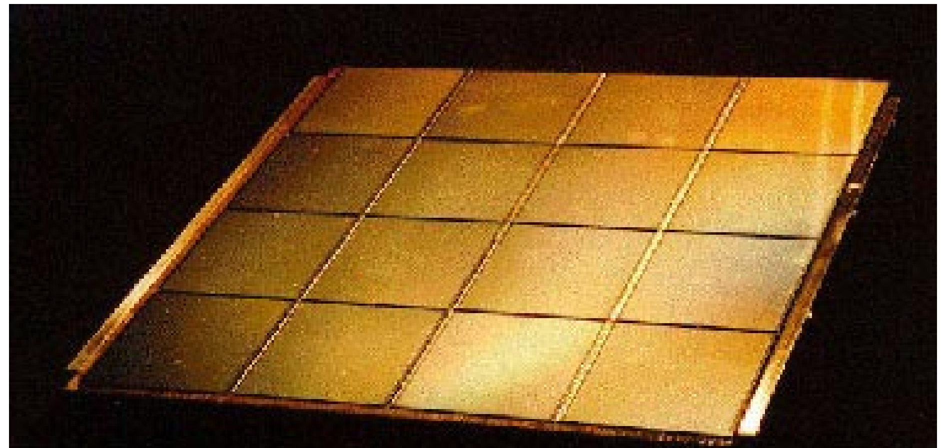
- Control initialization, calibration, and readout of the front-end readout chips.
- Sparse readout—build list of hit-strip addresses.
- Calculate the time-over-threshold of the prompt trigger output.
- Build events and coordinate the readout with neighboring layers via a serial data line and a token.
- External communication via low-voltage-swing differential lines.
- Currently being designed for the HP 0.8 µm process using the CMOSX standard cells. The logic design is synthesized from Verilog code.



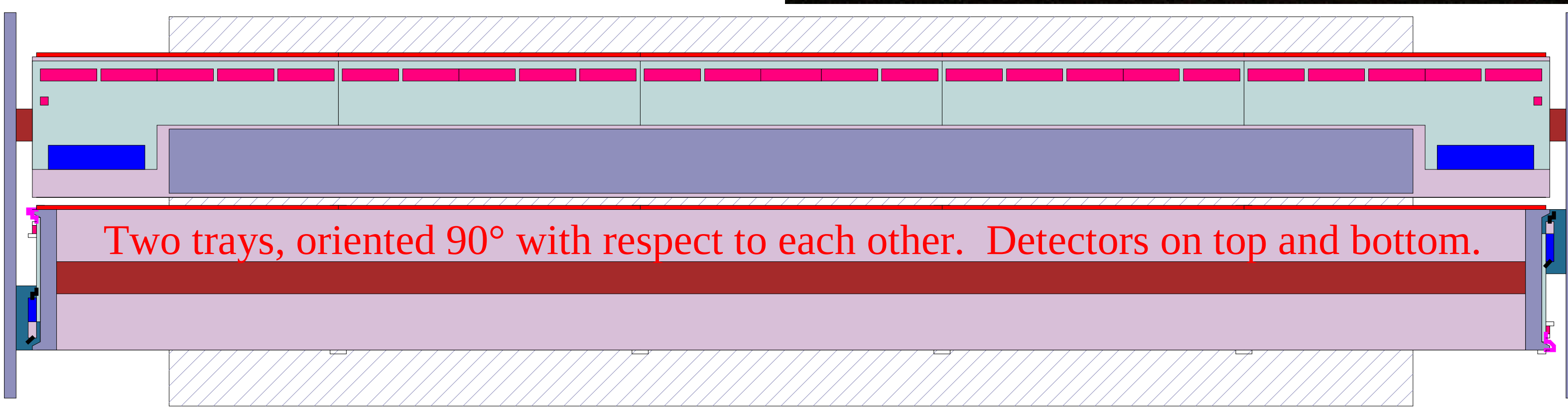

*Simplified block diagram of the readout controller chip.*

# Mechanical-Thermal Issues

- Rigid, low-mass supports for the detector planes ⇒ composite "trays."
- Minimum gap between trays, to keep the *x*,*y* detector pairs as close as possible to the converter foils.
- Electronics on the sides of the trays, to minimize dead area.
- Flex circuits to connect the detectors to the electronics.
- Passive cooling via the tower walls.

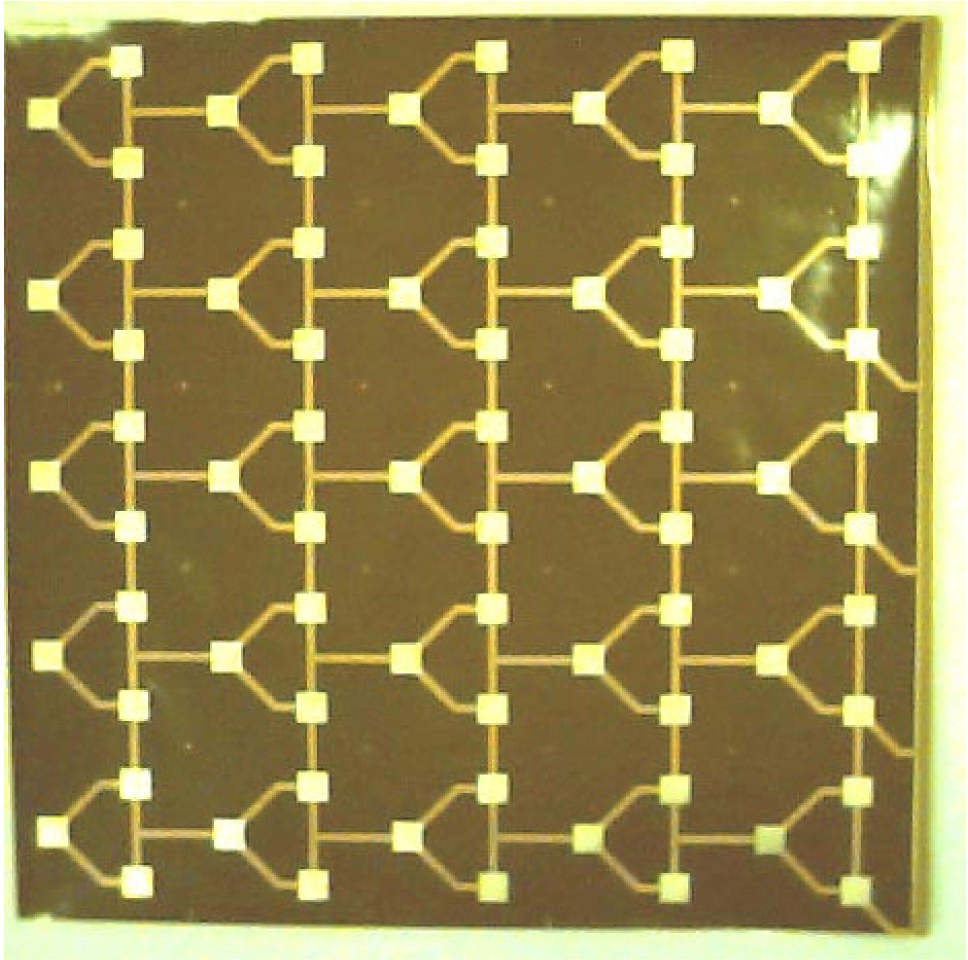


Prototype 4×4 tray for mechanical testing.
It was tested under vibration and thermal/vacuum at the Loral Corp.

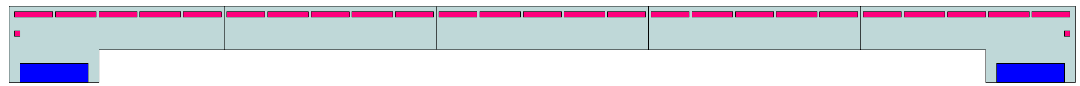


# Flex Circuit Detector Interconnect

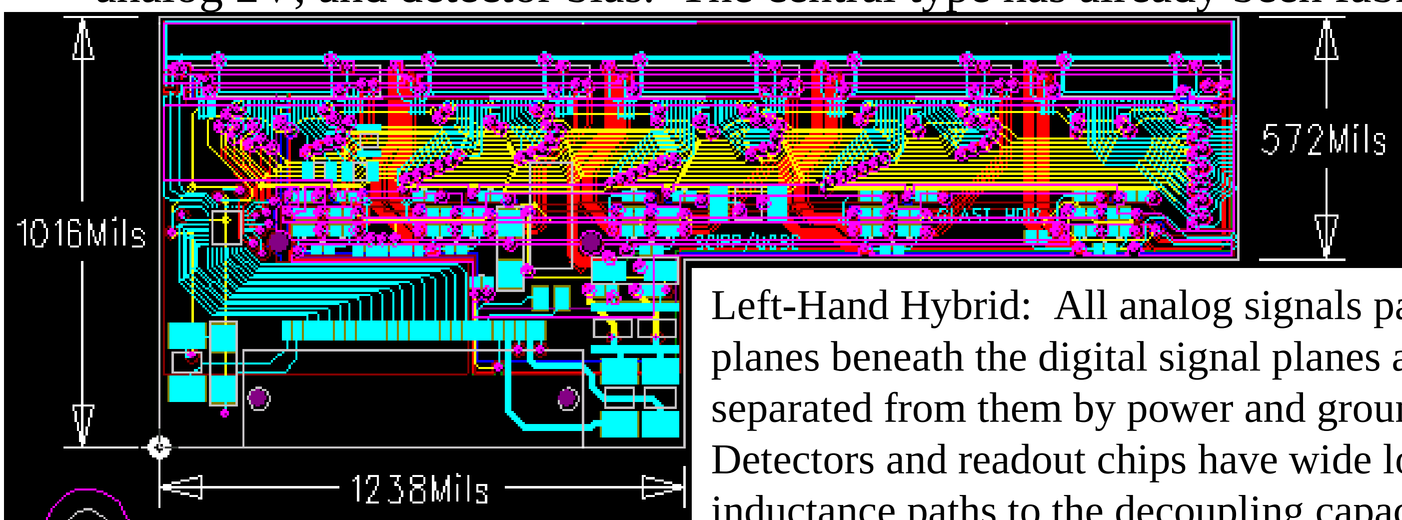
- Glued to the surface of the tray.
- Contacts the back of each of 25 detectors at 3 points to supply the bias potential.
- Copper shield layer connected to ground to prevent noise pickup from the tray structure.
- 1610 fine gold traces on one edge, to carry signals, bias, and ground around the corner of the tray to the electronics.



# Hybrid Circuits



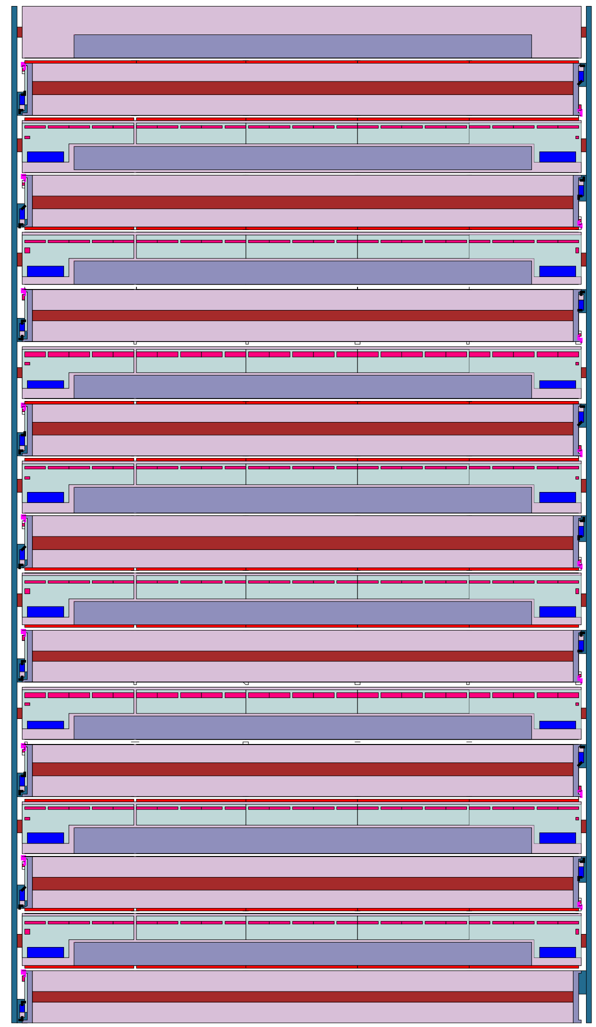
- The hybrid circuits include
  - bypass capacitors for each readout chip and the detector bias,
  - resistors to set the front-end bias current, and termination resistors for the digital signal lines.
  - Power supply filtering and fuses.
  - Temperature monitors.
- Eight layers are used in the layout, including entire planes for power, ground, analog 2V, and detector bias. The central type has already been fabricated.




Left-Hand Hybrid: All analog signals pass along planes beneath the digital signal planes and are separated from them by power and ground planes. Detectors and readout chips have wide low-inductance paths to the decoupling capacitors.

# Engineering Prototype Tower

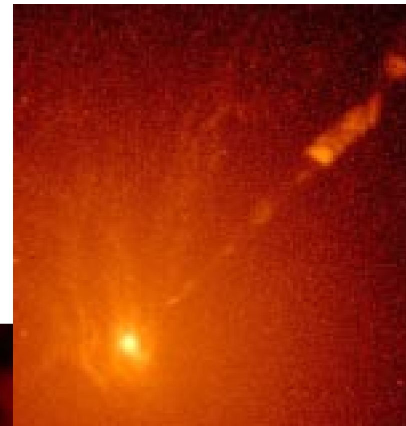
- A single GLAST tower is now being built:
  - complete by early 1999,
  - verify engineering and develop assembly procedures,
  - subject to environmental testing,
  - beam test in electron, photon, and hadron beams,
  - and possibly fly in a balloon.
- Current NASA strategic plan:
  - New start for construction of GLAST in FY 2000. *All R&D must be finished by then!*
  - Launch in mid 2004.

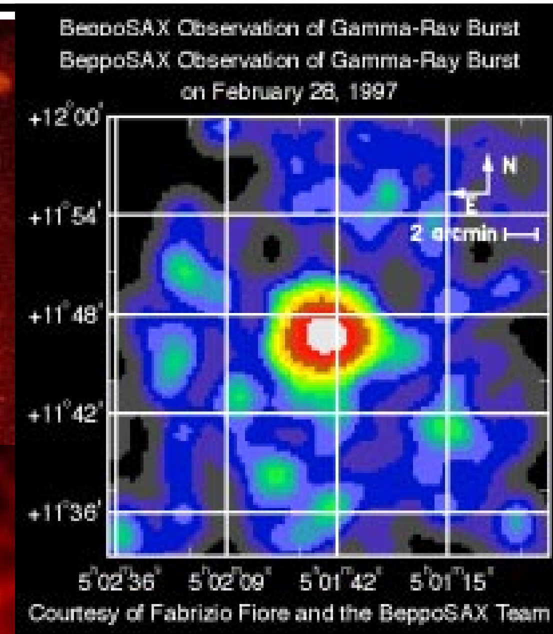


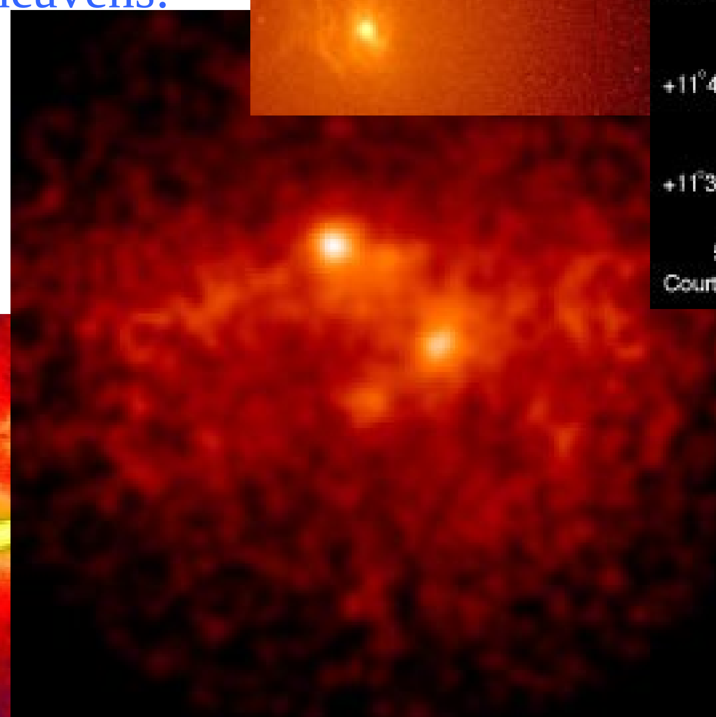
# Conclusion

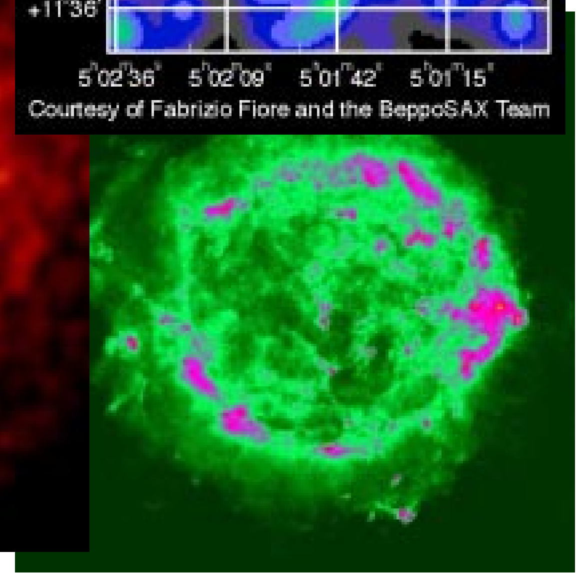
During the next decade, silicon-strip technology will be greatly expanding our knowledge of the surprisingly many enigmatic gamma-ray sources in the heavens:

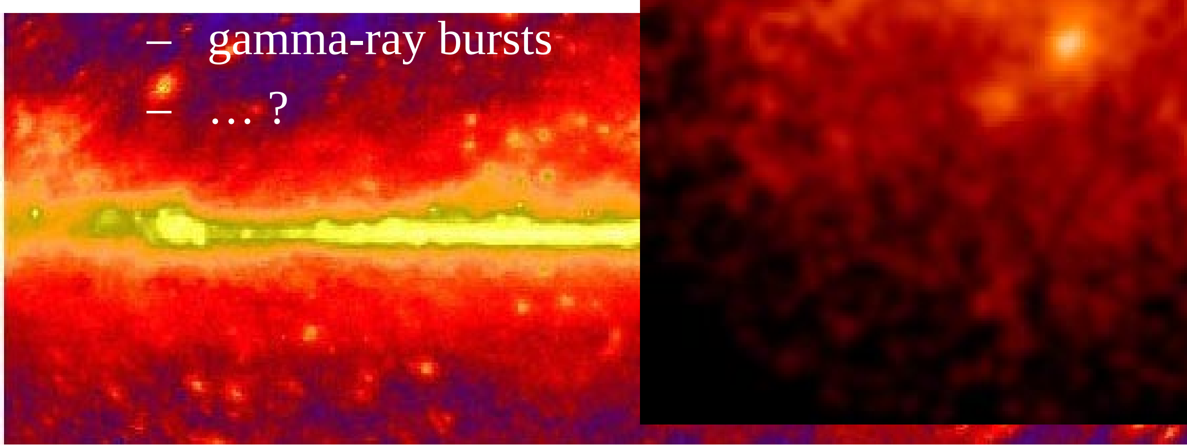
- galactic core
- pulsars
- supernova remnants
- active galactic nuclei
- gamma-ray bursts
- … ?









# GLAST Collaboration

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International Center for Theoretical
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Kanagawa University-Japan,
Lockheed-Martin Research Laboratory,
Max Planck Institut für
Extraterrestrische Physik-Germany,

Naval Research Laboratory,
SACLAY-France,
Sonoma State University,
Stanford University: HEPL & SLAC,
University of California Santa Cruz,
University of Chicago,
University of Rome- Italy,
University of Tokyo-Japan,
University of Washington

**10 Astronomy/Astrophysics (black) + 10 HEP (red) Institutions**
**(About 90 Collaborators)**