The GLAST Silicon-Strip Tracker
Detectors and Electronics

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Abstract

A silicon-strip detector system with more than a million channels is being developed as the tracker/converter element of a new gamma-ray telescope. While the silicon-strip technology appears to be ideal for space applications, there are challenges to be met in order to launch such a large system and operate it for long duration in orbit. This paper describes the detectors and readout electronics under development and shows how prototypes operated in a test beam have demonstrated the needed signal-to-noise performance and expected angular resolution on a power budget of 150 μW per channel.

I. Introduction

The Gamma Large Area Space Telescope [1] is a satellite mission that is currently in its research and development phase, with a construction phase projected to begin around the end of the year 2001. GLAST is a gamma-ray pair conversion telescope that operates in much the same way as the EGRET experiment on the Compton Gamma Ray Observatory [2]. As a successor to EGRET, however, GLAST is intended to improve upon EGRET's sensitivity to astronomical point sources by factors of 10 to 100. That is accomplished primarily by taking advantage of silicon-strip detector technology developed during the past decade for applications in elementary particle physics experiments [3].

The GLAST detector consists of a square array of nearly identical tower modules, as indicated in Fig. 1. Each tower has a scintillator veto counter on the top (and on the sides for the edge towers), followed by a multilayer silicon-strip tracker and, finally, a cesium iodide calorimeter. Each of the tracking layers has two planes of single-sided silicon-strip detectors with strips oriented at 90 degrees with respect to each other. All but the bottom few layers have a thin lead foil preceding the detector planes, to convert the incident gamma-ray photons into electron-positron pairs, which are subsequently tracked by the remaining detector layers to determine the photon direction. Finally, the calorimeter absorbs the electrons and thereby measures the photon energy.

Besides providing optimal angular resolution for this type of device, the silicon-strip technology is fast, yielding a system with very little dead time, provides excellent multi-track separation, which is important for background rejection, and can be made self triggering. The latter two points eliminate the need for a time-of-flight system, such as used by EGRET for triggering, and thereby result in a very compact instrument with a wide, almost 2π steradian, field of view. The silicon-strip technology is by now well developed, is known to be robust, requires no consumables, such as gas, and operates at a relatively low voltage, compared with spark or drift chambers. It therefore appears to be ideally suited for space applications.

The GLAST instrument design has more than a million silicon-strip channels. Two clear limitations on operating such a system in space are the availability of power for the electronics and the difficulty of dissipating the resulting heat. Previous silicon-strip systems, designed for operation in ground-based experiments, or in space with a relatively small number of readout channels, have not needed to contend with such severe power limitations [4, 5]. For those reasons, a major goal of the research and development effort within the GLAST collaboration has been to design and test readout electronics that can meet the signal-to-noise requirements with minimal power dissipation.

II. Tracker Electronics Requirements

The silicon strip detectors used by GLAST are single sided, with integrated AC coupling capacitors. Simulations show that the use of double sided detectors would improve the performance by 5% to 10%, because of reduced material and better localization of the measurement planes with respect to the converter foils. Such a minor improvement does not, however, justify the extra expense and the considerable mechanical and electrical complications that would arise from the use of double-sided detectors.

The strip pitch has been chosen to be 200 μm, which gives a good balance between the low-energy performance, for which the angular resolution is dominated by multiple

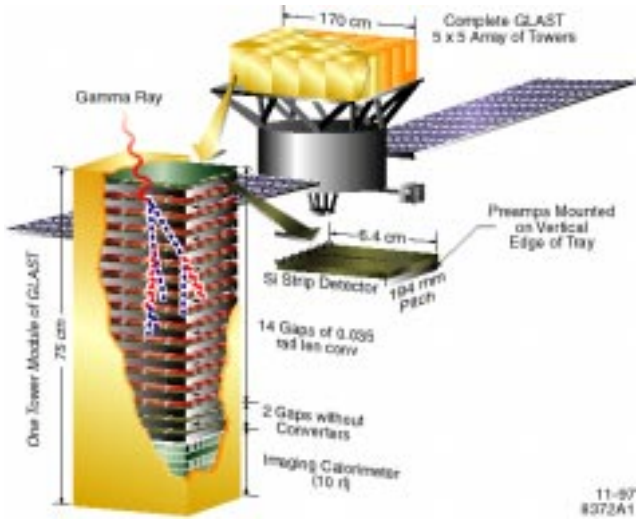

Figure 1: The GLAST detector concept.

scattering, and the high-energy performance, which is determined by the ratio of the strip pitch to the gap between measurement planes. Because of the presence of the lead converter foils, the angular resolution does not depend as strongly on the detector thickness as it does in typical high-energy physics applications. We have chosen 400 μm thick detectors, which gives a good match between the pitch and the thickness and provides better signal-to-noise performance than the more standard 300 μm thickness. The minimum signal corresponds to 200 μm of ionization both for tracks at normal incidence, for which the charge can be split between two strips, and for highly inclined tracks that pass sideways through one cell.

The detector strip capacitance has been measured to be about 1.2 pF/cm. Five 6.4 cm square detectors are connected in series, yielding 32 cm long strips with 38 pF of capacitance. That figure plus the expected minimum charge deposition determine the principal requirements for the readout preamplifier.

The limited power levels available from solar panels, together with the necessity of transporting heat from the instrument interior to radiators on the satellite periphery, dictate that the tracker readout electronics should not consume more than about 200 μW of power per channel. That includes the digital processing and data transmission as well as the amplifiers and discriminators.

Pulse-size analysis is not needed for GLAST, so the power restrictions naturally lead to a binary readout, with a simple single-threshold discriminator for each channel. The tracker must be self-triggering, however, so the electronics must produce a fast logical-OR of each entire detector plane, to be used as input to the trigger logic. It is desired that the readout system be able to accommodate trigger rates as high as 10 kHz with minimal dead time. This necessitates clocking out of data from the chips while the amplifier inputs are active.

The noise occupancy for an instrument of so many channels must be low, 0.01% or less, to avoid overloading the data stream and trigger with noise hits. For the detectors proposed for GLAST, that roughly translates into the requirement that the equivalent noise charge (ENC) not be more than about ¼ fC (1560 electrons). Also, since the discriminator threshold can realistically only be adjusted at one common level for each 64-channel chip, the channel-to-channel variation in threshold across a chip must be commensurate with the size of the stochastic noise.

The radiation exposure in the GLAST orbit will be modest compared with the environment of detectors in contemporary accelerator beams, with only about 1 kRad per year predicted. We expect to be able to demonstrate that standard CMOS processes can, with sufficient care taken in the design, withstand that level of radiation with no degradation in performance. The biggest impact of the radiation will likely be on the detectors. Our prototypes (500 μm thickness, 236 μm strip pitch, 55 μm width, and 6 cm length) show leakage currents from 10 to 15 nA per strip after 10 kRad of irradiation in a ^{60}Co source. To avoid being dominated by shot noise, the electronics should have a pulse peaking time of not much more than 1 μs. The triggering requirements lead to a similar upper bound on the time constant.

The readout electronics must be designed to fit into a very narrow space along the edge of a detector plane, to minimize the dead area within the instrument, and the number of wires running up and down the tower should be minimized. Finally, it is important that redundancy be built into the readout system, to avoid the possibility of catastrophic single-point failures.

III. The Readout Electronics

A 64-channel ASIC is being developed to read out the GLAST silicon-strip detectors. Each channel includes a charge sensitive preamplifier, followed by an RC/CR shaping amplifier, a comparator, a digital mask, an 8-event deep FIFO buffer, and a latch. The latches are arranged as a shift register, such that the latched data can be read out serially. In addition, there is a logical OR of the comparator outputs after the mask, to be used as a fast trigger, and there is an internal pulse generator, together with a 64-bit mask, to allow an adjustable charge to be injected into the inputs of any subset of channels.

The comparator thresholds are set in common by a 7-bit DAC. A second DAC is used to set the calibration pulse size.

The mask that follows the comparators is actually divided into two separate 64-bit masks, one for the fast trigger OR and the other for the data. That will allow us to remove slightly noisy channels from the trigger without necessarily losing data from them.

The output shift register is also made up of two separate registers, one that shifts from left to right and another that shifts in the opposite sense. Twenty-five chips are lined up along the edge of a detector plane and connected together to form two 1600-channel shift registers. The chain may be configured, by loading the control registers, such that it is divided between any pair of chips, with all chips to one side shifting data out in one direction while the others shift data in the opposite direction. That allows any single dead chip to be bypassed in the readout without losing data from any other chips.

The fast trigger OR can also be passed to the chip on the left or the one on the right. It makes its way from chip to chip, such that in the end we have an OR of all 1600 channels in the detector plane. The event trigger will probably be a simple coincidence between 6 consecutive detector planes (3 in the *x* view and 3 in the *y* view). Assuming that the coincidence window is about 1 μs, the single-channel occupancy must be less than 10^{-4} in order to keep the noise trigger rate of the overall instrument well below the cosmic ray rate. We are considering having two comparators for each channel, one for the trigger and one for the data, in order to be better able to control the trigger rate without impacting the tracking efficiency (but at the cost of increased power consumption).

The chips have a simple sparse readout in the sense that if no channel within a given chip registers a hit, then only a single bit, a zero, is shifted out for that chip (followed by the data of the next chip in line). If one or more channels register hits, then a one is shifted out, followed by the 64 bits

corresponding to the channel contents. Since in a typical GLAST event a given detector plane should contain hits in only a few chips, this feature greatly increases the average readout rate.

At each end of a set of 25 front-end readout chips is an ASIC digital readout controller that is currently under design. Besides acting as an interface between the data acquisition system and the front-end chips, the readout controllers also serve to format the data by turning the digital hit pattern into a list of addresses of hit strips. All signal transmission between the controller chips and front-end chips, as well as between the controller chips and the data acquisition system, is by low-voltage balanced differential lines, to avoid inducing digital noise into the sensitive front-end amplifiers.

The principal issues in the amplifier design were power, noise, and threshold uniformity and stability. Because of the binary nature of the readout, there were no stringent requirements on linearity and dynamic range, and the speed requirements were modest. The architecture was roughly modeled after the front-end amplifiers of the BaBar SVT readout chip [6]. However, to save power and to match the GLAST bandwidth requirements, the active cascodes were replaced by simple cascodes, and the number of amplifier stages was reduced to two.

The first stage integrates the charge with a time constant that is determined by the input-impedance requirements and is short relative to that of the second stage. The second stage has roughly equal integration and differentiation time constants of about 1 μs. Its output pulse is unipolar, although the long reset time constant of the first stage results in some undershoot.

We expected a threshold variation of about 10 to 15 mV rms, so the overall amplifier gain was chosen to be 125 mV/fC. The noise goal then translates into 32 mV rms at the comparator input. If we require that the threshold be at least 4σ above the noise for 99% of the channels, then a threshold range of 160±30 mV (1.0 to 1.5 fC) is safe. On the other hand, even a 1.8 fC threshold ensures essentially 100% efficiency, assuming a signal from a minimum of 200 μm of silicon (2.6 fC) and taking into account Landau fluctuations.

The preamplifier must operate asynchronously, so a continuous baseline restoration with a 20 μs time constant is used. The preamplifier is AC coupled to the shaping amplifier, which has a peaking time of about 1 μs. The shaper feedback scheme is modeled on that used in previous chips, such as the Kipnis-Zimmermann design for the SVX-II preamplifier [7]. A relatively slow differential amplifier serves to adjust the bias point of the input transistor such that the output baseline (which is the comparator input) is fixed at the reference voltage. Transistor mismatch in this amplifier is the main contributor to the threshold dispersion, and its low current density makes the matching potentially problematic. We chose the transistor sizes to ensure an rms variation of less than 15 mV at the shaper output, using the measurements of Ref. [8] for guidance.

The DC feedback network also provides the differentiation function of the shaping amplifier. However, for input charges greater than about 1 fC the baseline restoration tends to be current limited, rather than having the exponential decay that would be characteristic of a linear network. Therefore, the output looks like the result of a true RC/CR filter only for small pulse heights.

The shaper is DC coupled to the comparator, which is a conventional two-stage design—a differential amplifier followed by an inverting amplifier. The tail current of the first stage is about 3 μA. Judging from the data of Ref. [8], the contribution to the threshold dispersion from the transistor pairs in the comparator is negligible compared with that from the shaper feedback network.

IV. Electronics Performance

Two successive prototype chips, the first with 16 channels and the second with 32, were fabricated in the Hewlett-Packard CMOS26G process (0.8 μm minimum feature size and 3 levels of metal interconnect) via the MOSIS VLSI fabrication service [9]. Those prototypes contained only the amplifier and comparator circuitry, plus a minimal digital readout for testing purposes. The digital readout was not designed to be operated simultaneously with the acquisition of data by the amplifiers. See Ref. 10 for more details on the design of those chips and their performance. A 64-channel prototype with the full digital functionality has also been designed and is presently being manufactured.

In summary, for a peaking time of 1.3 μs and a power consumption of 140 μW per channel, the noise of the prototypes was measured to be under 1600 *e* for the anticipated GLAST detector load of 38 pF per strip. The overall gain, up to the comparator input, is 115 mV/fC, which is close to the desired value. Threshold scans made on all channels of 59 32-channel chips gave a 6 mV threshold variation per chip on average, but with a few chips showing variations as large as 16 mV rms. All of these results satisfy the GLAST requirements. Figure 2 shows a measurement of the noise occupancy versus threshold for a channel connected to a 30 cm long silicon strip (five 6 cm detectors bonded in series) with a total capacitance of about 36 pF.

Figure 3 shows some measurements of the shaping amplifier output waveform with no load on the preamplifier input. With the input bonded to a 38 pF capacitor the peaking time increases by about 20%. However, we are not able to make a reliable measurement of the pulse shape in that condition, due to coupling between the probe tip and the nearby bond wire.

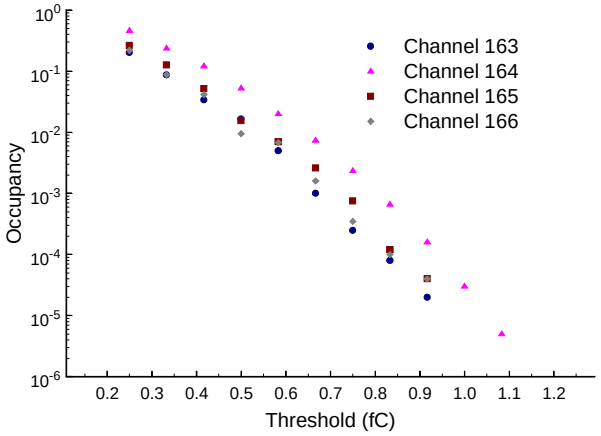

Figure 2. Measurements of the noise occupancy in four channels of a 32-channel prototype amplifier-discriminator chip, versus the threshold. The channel is connected to a 30 cm long strip with a capacitance of 36 pF. The trigger window is 1 μs.

The shaping amplifier output saturates for input charges greater than about 20 fC, or 4 minimum ionizing particles at normal incidence. Nevertheless, the output still recovers gracefully at a rate dictated by the 30 nA current source in the feedback network. Except for input charges less than about 1 fC, the time-over-threshold of the shaping amplifier output is approximately a linear function of the input charge. The slope is approximately 1 μs/fC. We plan to take advantage of this feature by digitizing the time-over-threshold of the fast-OR output of each detector plane (not the individual channels) to obtain some information on the level of ionization. That will enhance the gamma-ray background rejection and may also be of interest for studies in cosmic-ray physics.

A prototype tracker was operated in an electron and tagged photon test beam at the Stanford Linear Accelerator Center during October of 1997, together with a prototype CsI calorimeter and a scintillator veto system. The tracker consisted of 12 detector planes, each consisting of a single 6 cm square detector, with the exception of one plane, which had 5 detectors connected in series. The detectors were arranged in *x,y* pairs, with each pair preceded by an interchangeable lead foil. The spacing between pairs was adjustable in steps of about 3 cm. The detectors had a strip pitch of 236 μm, and 192 channels were read in each detector plane by six 32-channel chips.

The detectors performed well during the beam test, with a high efficiency. Figure 4 shows the single-plane hit inefficiency as a function of threshold and bias voltage, as

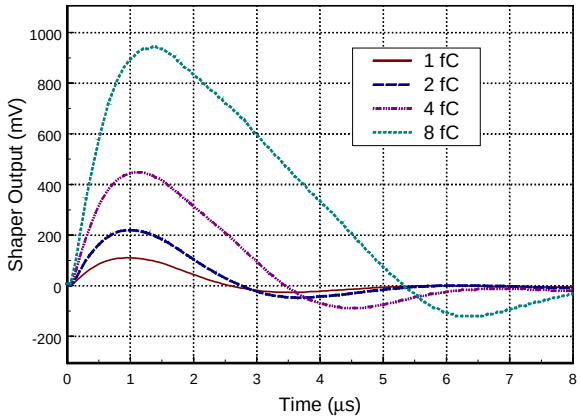

Figure 3. Measurements of the shaping amplifier output waveform for four values of injected charge. There was no load on the preamplifier inputs. The measurements were made by probing an internal pad of the 32-channel chip.

measured from the tracks of high-momentum electrons. The detectors were 500 μm thick, but the 90 V bias voltage roughly corresponds to 400 μm of depletion. The efficiency is essentially 100% for the 1 to 1.5 fC thresholds that we anticipate using in GLAST.

The tracker as a whole performed exactly as expected. Figure 5 shows the measured angular resolution for a particular configuration, compared with a detailed Monte Carlo simulation. The simulations and measurements agree very well. Note that although this configuration corresponds fairly closely to the GLAST design in terms of lead converter thickness and interplane spacing, the measured values for the angular resolution are strongly influenced by edge effects and should not be taken as a prediction of the GLAST tracker performance.

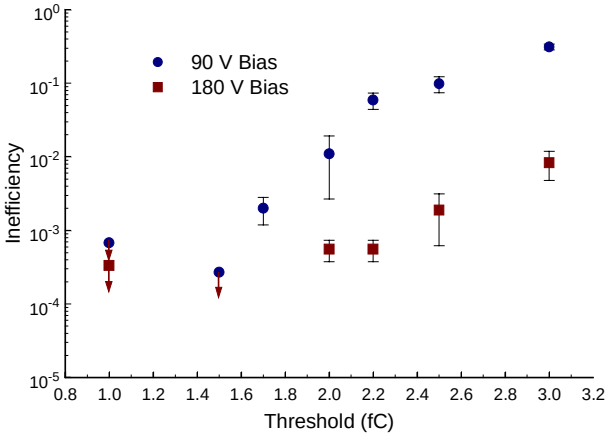

Figure 4. The tracking inefficiency as a function of the discriminator threshold, as measured in an electron test beam using the prototype module with 30 cm long strips. At 90 V we expect the detectors to be depleted to a depth of about 400 μm.

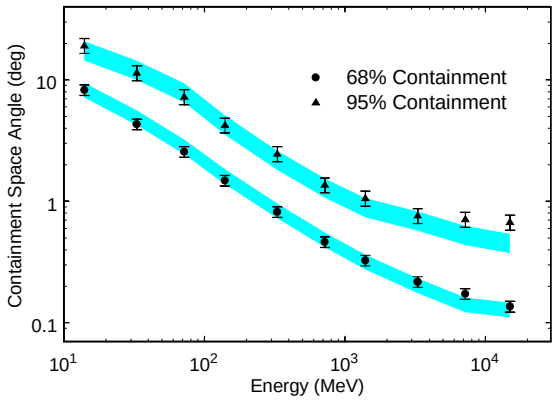

Figure 5. The angular resolution of the beam-test tracker, expressed in terms of the space angle for 68% containment of the data and 95% containment. The error bars are 2σ statistical errors. The shaded bands indicate 2σ Monte Carlo simulation confidence regions.

V. Conclusion

Progress has been made in the development of a mega-channel silicon-strip detector readout system that can operate reliably in space on a power budget of only about 250 W. Using conventional technology and standard CMOS design techniques, we have developed and tested an amplifier-discriminator chip that meets our power, noise, and threshold-stability requirements. Fifty-nine of those chips, with a total of 1888 channels, recently operated successfully in a test beam over a period of one month without developing any problems.

The present design consumes less than 150 μW per channel, leaving sufficient power in the budget for the remaining digital processing and data transmission that will be needed in the full-scale GLAST tracker. The noise level and threshold variation are small enough that we should be able to achieve essentially 100% detection efficiency for minimum ionizing particles passing through live detector regions, while still maintaining an acceptable noise occupancy level of 0.01% or less. We still must demonstrate, however, that operation of the full-scale digital readout in the chips now under development does not induce enough charge into the amplifiers to increase significantly the noise occupancy.

VI. Acknowledgements

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