ELSEVIER

Nuclear Instruments and Methods in Physics Research A 435 (1999) 224–232

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

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The silicon tracker/converter for the gamma-ray large area space telescope

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Abstract

The Silicon Tracker/Converter of the Gamma-ray Large Area Space Telescope (GLAST) will have an active area of 80 m^2, representing one of the largest planned applications of the silicon-strip detector technology. The large number of channels (1.3 million) to read out, together with the requirement that the tracker provide the trigger to the data acquisition, force the readout electronics to be of very low noise. Furthermore, to fit into the power constraints of the satellite environment, the electronics must have an ultra-low power consumption. To fulfill these requirements, plus others imposed by the space environment, such as redundancy, a mixed mode CMOS front-end readout chip and a digital readout controller chip have been designed and prototyped. In this article, we present the status of the readout electronics and the results from a test-beam study with a small GLAST tracker prototype.

1. Introduction

The high performance of silicon-strip detector technology coupled with large reductions in the price of silicon detectors has led to a boom in the construction of very-large-area precision tracking devices based on silicon. Examples are the LHC experiments, ATLAS [1] and CMS [2], the NAUSICAA [3,4] proposal for a neutrino oscillation experiment, and the Gamma-ray Large Area Space Telescope (GLAST) [5,6]. In the case of the GLAST, given the limitations of the space environment, silicon-strip technology provides some additional advantages: no consumables, relatively low voltage operation, reliability and robustness, high signal-to-noise, and high-density readout via standard CMOS technology.

The gamma-ray pair-conversion telescope currently in orbit, EGRET [7] on NASA's Compton Gamma-Ray observatory, has revolutionized the field of high-energy gamma-ray astronomy. Since it was launched in 1991, it has discovered dozens of new point sources such as active galactic nuclei and pulsars and has detected GeV photons in gamma-ray bursts and high-energy gamma rays in solar flares. Many questions remain to be addressed by more extensive and accurate observations. A good fraction of the sources detected by EGRET have

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0168-9002/99/$ - see front matter
PII: S0168-9002(99)00442-8

not been identified, especially in the galactic plane, and the production mechanisms and temporal variations of the sources are still generally poorly understood. GLAST, the next generation gamma-ray telescope, will address these questions with a sensitivity that is 10 to 100 times better than that of EGRET, guaranteeing the observation of hundreds to thousands of new sources of the types already known as well as offering a tantalizing possibility for discovery of entirely new phenomena. GLAST is scheduled to be launched in late 2004 and will be operational for at least a 5 year period. The GLAST collaboration comprises over 90 physicists from 20 high-energy physics and astrophysics institutions in the United States, Japan, and Europe.

The article presents the status of the development and construction of the GLAST tracker/converter. The second and third sections describe the design of the overall GLAST instrument and the tracker, respectively. The fourth section is dedicated to the status of the readout electronics, and in the fifth section the test-beam results are presented.

2. The gamma-ray large area space telescope

GLAST will study cosmic gamma-rays with energies between 20 and 300 GeV. Such photons are produced by cosmic-ray interactions with interstellar gas at the sites of the most energetic natural accelerators in the universe. This energy range extends significantly above EGRET's, in order to achieve some overlap with ground-based experiments [8,9] that detect the Cherenkov light produced in atmospheric showers produced by ultra high-energy gamma-rays. The main interaction process of gammas above 10 MeV is pair conversion $\gamma \rightarrow e^+ + e^-$. The GLAST tracker is, therefore, a pair-conversion telescope consisting of many layers of thin lead converter foil followed by silicon-strip tracking detectors. The electron and positron produced by the conversion in the lead foil are tracked by the silicon-strip detectors, and their energy is measured by a calorimeter that follows the tracker. Thus both direction and energy are measured for each incident photon. Monte Carlo simulations have also demonstrated a possibility of having some sensitivity to the photon polarization for photon energies around 100 MeV, although only on a statistical basis.

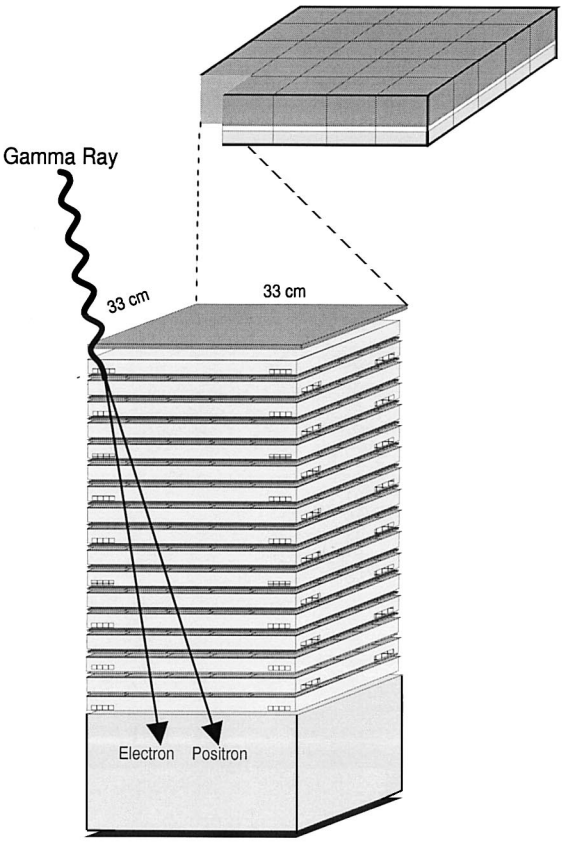

Fig. 1. View of the 5×5 towers and a zoom image of one of them. The drawing shows the 17 tracker trays and the calorimeter at the bottom.

The GLAST instrument is composed of three subdetectors, as illustrated in Fig. 1: a scintillator-based anti-coincidence detector (ACD) for rejection of charged cosmic-ray background, the silicon-strip tracker/converter, and a semented CsI crystal calorimeter. It is structured in a modular design, composed of a 5×5 array of identical towers, covered on the front and sides by the ACD. Each $32 \times 32\ cm^2$ tower has a tracker/converter of 16 tracking planes per view, a 10 X_0 calorimeter with crystals stacked in x, y planes to provide a hodoscopic view, and a data-acquisition/CPU board for readout, triggering, and online data reduction. The

total area in single-sides silicon-strip detectors is more than 80 m^2.

To maximize the scientific potential, GLAST should have a large area, good angular resolution, and a large field of view. These factors all enter into the point-source sensitivity, which is predicted to be 3.5×10^{-9} photons/cm^2s at 5σ in one year of data taking,[2] for gamma-rays with $E > 100$ MeV from sources well removed from the high diffuse back-ground of the galactic plane. The effective area of GLAST (area times efficiency) is about 8000 cm^2 at 1 GeV photon energy. The single-photon angular resolution (in astrophysics terminology the PSF, or "Point Spread Function") is 3° for 68% containment of the space-angle at 100 MeV and better than 0.1° for energies above 10 GeV (see Fig. 2). Those two parameters determine the sensitivity when GLAST is pointing at a given source, but the large field of view of 2.6 sr FWHM ensures that all sources can be continuously monitored while scanning the full sky during each orbit. Since many of the known sources exhibit large transient behavior, that is a crucial factor for the science.

The effective area and the PSF are conflicting parameters that both depend on the converter thickness. An increase in thickness of the converter foils increases the effective area but deteriorates the angular resolution, due to increased multiple scattering of the electron and positron. The GLAST design has been optimized using a full Monte Carlo simulation called GLASTSim [12], based on the object-oriented GISMO [13] program. To take a simplified approach, it is desirable that at about 1 GeV (roughly the geometric mean of the energy range) the multiple scattering in a foil should be no worse than the intrinsic two-plane measurement precision $\theta_n = \sqrt{2}\sigma/d$, where σ is the silicon-strip position resolution and d the distance between two measurement planes. Demanding that $\theta_n \approx 0.15°$ and, for practical reasons, choosing a silicon-strip pitch of 195 μm, leads to the GLAST baseline design of $d = 3.1$ cm and a Pb foil thickness of 3.5% X_0.

[2] Assuming continuous full-sky scanning throughout the year.

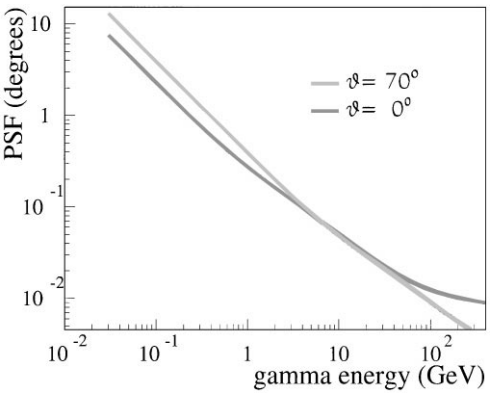

Fig. 2. The PSF (or spatial angular resolution) in degrees as a function of the gamma energy for normal and 70° incident angles. The PSF was calculated analytically using the Kalman Filter technique [11].

In addition to measuring the gamma-ray signal, the GLAST instrument must separate the gamma-rays from the cosmic-ray background of charged particles that are up to 10^4 times more numerous. That is achieved by a combination of the ACD veto system surrounding the front sides of the tracker, analysis of the hit patterns in the tracker, analysis of the shower shape in the finely segmented calorimeter, and analysis of the matching between the tracker and calorimeter. A full Monte Carlo analysis with GLASTSim has shown that sufficient rejection can be achieved to give a signal-to-noise of better than 20:1 for the high-latitude (i.e. out of the galactic plane) diffuse gamma-ray signal, one of the weakest signals that GLAST is designed to study.

The space environment imposes numerous constraints on the GLAST design in addition to the science requirements. That which is most restrictive to the tracker is the limited availability of power and cooling. The total power budget for the experiment is 650 W, with 260 W allocated to the tracker, or 200 μW for each of the 1.3 million readout channels. The tower electronics must be cooled passively and entirely by conduction to external radiators. In addition, the structures must withstand large accelerations and vibration during launch and potentially large thermal cycles. The bandwidth to the ground is very limited (order of 10^5 bps on average)

compared with HEP experiments, requiring significant real-time data reduction on the spacecraft. Finally, given the complete inaccessibility of the apparatus after launch, reliability is even more critical than in an HEP vertex detector.

It is important to design in redundancy to accommodate failures of components with out losing large amounts of detection capability. To that end, the 25 towers are networked on a grid structure, such that several entire towers could be lost without disabling the instrument. Within the towers, redundancy is also designed into the electronic readout, as discussed below.

3. The GLAST silicon tracker

The main component of the GLAST tracker [14] is the tray, a $32 \times 32\,\mathrm{cm}^2$ and 3.2 cm thick lightweight composite structure that supports silicon-strip detectors on both faces and readout electronics along the sides. The detectors on both faces have strips running in the same direction. Alternate trays are oriented at 90° with respect to each other and stacked and aligned on small corner posts such that there is a 2 mm gap between detector planes in each x, y pair. Sandwiched between the upper detector plane and its support structure lie the Pb converter foils, which are cut to match the active areas of the silicon wafers. In this way, the x, y pair is positioned as close as possible to the converter, in order to minimize the lever-arm for multiple scattering, and the silicon wafers are secured onto thick, rigid tray structures that can ensure survival during launch. Kapton flex circuits carry the detector signals around the tray corners to the electronics, with the detectors on opposing face of a tray reading out into electronics on opposite sides. Since alternate trays are rotated by 90°, the electronics and the heat they produce get distributed uniformly into all four sides of the tower. Kevlar cables pass through the corner posts to hold the stack in compression, and all four tower sides are covered by thin carbon-fiber sheets to conduct heat and to stiffen the structure.

Fig. 3 shows the elements of the tray. They are from top to bottom: (1) a plane of single-sided silicon-strip detectors, (2) the flex circuit for biasing the detectors and carrying the signals around the tray corner, (3) a carbon or aluminum face sheet, (4) a carbon or aluminum hex-cell core, (5) the other face sheet, (6) the Pb foils, (7) another flex circuit, and (8) the second detector plane. A closeout frame, probably to be constructed from

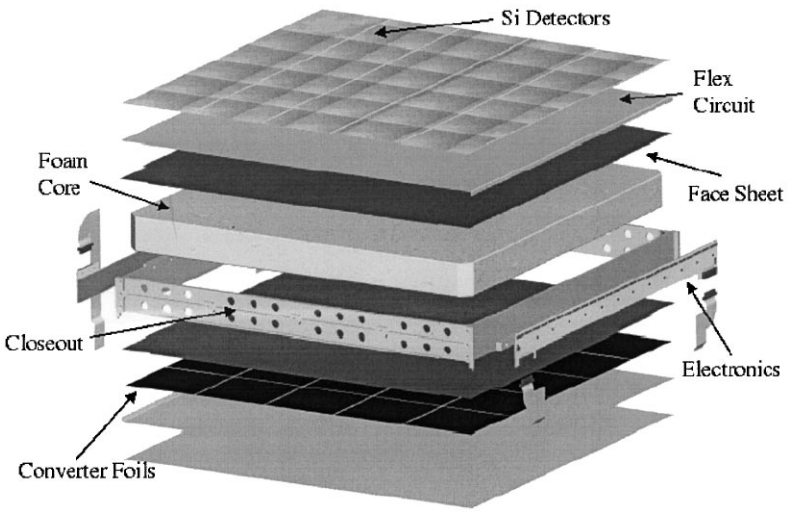

Fig. 3. View of the different elements of one tray. From top to bottom: A silicon plane, a C (or Al) cell core structure, the 3.5% X_0 converter plane, and the second silicon plane. The hybrids are mounted on the sides of the Al closeout.

carbon fibers, completes the composite structure. The total thickness in radiation lengths of a tray is less than 5%.

The silicon-strip detectors are edge-glued, wire bonded, and the wire bonds potted to form monolithic 5-detector "ladders," which are then glued to the flex circuit with a conductive epoxy. This procedure makes the detectors easy to handle during the wire bonding procedure and allows the ladders to be tested before bonding to the tray. Wire bonds connect the detector strips to 1600 short gold traces along one edge of the flex circuit, which carry the signals 90° around the tray corner to the hybrid circuit upon which are mounted the readout electronics. The hybrid circuit board is glued to the flex circuit and fastened with screws to the closeout. Each holds 25 64-channel front-end readout chips, which are wire bonded to the flex circuit, and two (for redundancy)readout controller chips. Two redundant multi-layer flex-circuit cables carry signals and power to and from the data acquisition board and connect into the hybrid circuits via miniature-connectors.

The silicon sensors are single sided, N-bulk, and AC-coupled, with the strip implants biased via polysilicon resistors. Three hundred detectors have been produced for prototype tower construction by Hamamatsu Photonics with dimensions of $6.4 \times 6.4\ \mathrm{cm}^2$ (from 4-in wafers) and a readout pitch of 195 μm. The thickness is 385 μm, rather than the 300 μm thickness commonly used in HEP, to increase the signal. They are of very good quality: the fraction of broken capacitors is $< 2 \times 10^{-4}$, and the leakage current is 0.5 nA/strip. In a sample of 54 detectors, the polysilicon resistors of four strips have been measured to be between 63–64 MΩ. The depletion voltage is typically 90 V.

The GLAST tracker will likely benefit from the 6-in silicon-strip technology currently in development by several manufacturers. This technology could produce sensors with significantly larger dimensions, which would reduce the dead space between detectors and the number of wire bonds, yielding both cost savings and improvements in performance. Hamamatsu Photonics has successfully produced a few prototypes with dimensions of $6.4 \times 10.7\ \mathrm{cm}^2$, and it is likely that the remainder of the detectors needed for the prototype tower will be manufactured to that size. The width was chosen to be compatible with the smaller detectors from 4-in wafers. In fact, larger detectors, such as $8 \times 10\ \mathrm{cm}^2$, could be fabricated, and the collaboration is considering changing the layout of the instrument to use such detectors in 5×4 arrays, with $40 \times 40\ \mathrm{cm}^2$ trays, and a 4×4 array of towers.

4. GLAST tracker electronics

The GLAST tracker readout is designed to be self triggering. The trigger is based upon a logical-OR (called a Fast-OR) of all 1600 channels of the 25 front-end readout chips on a single hybrid. A coincidence, in a 0.5 μs window, is formed between the Fast-OR of an x layer and that of the adjacent y layer. If three planes in a row in any single tower have such x, y coincidences, then a level-1 trigger is generated, which latches the tracker data in all 25 towers. For such a trigger to work, it is obvious that the single-channel noise occupancy in any random 0.5 μs window must be much less than 1/1600. That places stringent noise requirements on the electronics that must be met within the 200 μW per channel power budget.

The noise and power goals have been met using standard submicron CMOS technology[3] by keeping the design relatively simple. In particular, no attempt is made to digitize the pulse sizes from individual channels. A single threshold is applied to the amplifier output of each channel to give a binary signal.[4] Two separate programmable masks for each channel allow noisy channels to be excluded from the Fast-OR and/or data readout.

The design has been implemented in a 64-channel mixed-mode (analog/digit) front-end readout chip named GTFE64 [15,16]. Each channel includes a charge sensitive amplifier, an RC/CR shaping amplifier, and a comparator. The preamplifier

[3] The Hewlett-Packard CMOS26G 0.8 μ, 3-metal process. Future development will have to take place in another process, as this one is being discontinued.

[4] We may in the future add a second discriminator to each channel to allow one threshold to be applied to the Fast-OR inputs used for triggering and a second, lower threshold for the data to be read out after triggering.

is a charge-sensitive folded-cascode amplifier followed by a source-follower output stage. The folding minimizes the power dissipation by allowing the input transistor to be biased with only 2 V (about 25 μA of current for a 2500 μm wide transistor), while the remainder of the analog circuitry is operated on a 5 V supply. A current source supplies a continuous current to reset the feedback capacitor. The preamplifier is AC coupled to the shaping amplifier, which is also a charge-sensitive cascode amplifier with a source-follower output stage. The shaper has a peaking time of about 1.3 μs. A slow differential amplifier in the feedback loop provides a reset current and also stabilizes the baseline of the output, which is DC coupled to the comparator, a differential amplifier followed by an inverting amplifier. The gain up to the shaper output is about 120 mV/fC.

The electronics noise has been measured with electronic connected to actual detectors, with one to five 6.4 cm detectors connected in series. The results were obtained by measuring the occupancy versus threshold in random triggers, so that what was measured is directly relevant to the instrument requirements. The detectors were new, so the leakage-current contribution to the noise was negligible. With a strip capacitance of 1.2 pF/cm, the results may be expressed in terms of equivalent noise charge as ENC = 280 + 28. C electrons, with the capacitance C in pF. For the 32-cm strips corresponding to the GLAST design, the equivalent noise charge is 1350 electrons, or about 0.22 fC. A minimum ionizing particle will produce a signal at normal incidence on the 400 μm thick detectors of $\approx$ 5.3 fC. The rms threshold variation across a 64-channel chip has been measured to be 440 electrons. Taking that into account, to achieve essentially 100% efficiency and still meet our noise occupancy requirements, we estimate that the total noise should not be greater than about 2400 electrons, or 0.38 fC, giving us some safety margin.

The digital part of the GTFE64 is designed to satisfy a number of system requirements, including redundancy in control and readout. It is supported by a separate custom digital chip, the readout controller named GTRC [17,18], of which two are mounted on each hybrid, for redundancy. The main features of the GTFE64 digital circuitry are:

1. Two redundant serial-command decoders. Each interprets the command line provided by one of the two readout controller chips (right or left).
2. Separate masks for the Fast-OR and data, as described above.
3. A calibration mask that selects the channels to be pulsed. An internal programmable DAC sets the height of the calibration pulse, and the pulse is initiated via a command.
4. A second programmable DAC to set the threshold (common to all channels).
5. An 8-event deep FIFO for each channel, to buffer the readout.
6. Dual redundant readout registers. The data and Fast-OR are passed from chip-to-chip until they arrive at a GTRC chip. Each GTFE64 chip can be programmed by either GTRC chip to operate in either direction, so the readout can be split between any pair of chips. The readout registers are zero suppressing in the sense that if there is no hit in the chip, only a single bit is sent. If there is at least one hit, then 65 bits are sent.
7. External communication via low-voltage differential signaling (LVDS).

All of the internal digital circuitry that is clocked during normal running, as opposed to initialization activity, operates at 3 V, in order to minimize power and noise pickup. The clock does not run continuously but is turned on only when a command is sent or a readout is in progress.

The GTRC chip is purely digital and operates at 3 V. Its functions are as follows:

1. Mediate all communication between the data acquisition board and the GTFE64 chips during initialization, calibration, and data taking. It decodes commands from the data acquisition board and sends commands to the GTFE64 chips, as well as buffering the clock and trigger signals.
2. Control the readout of the GTFE64 chips and zero suppress the data, which get formatted into a list of addresses of hit channels.
3. Digitize the time-over-threshold of the Fast-OR signal to give a measurement of the collected charge. Since the GTFE64 shaper output tends

to reset linearly with time, rather than exponentially, for all but all the smallest signals, the time-over-threshold is roughly a linear function of the charge deposition. It is buffered in an 8-event deep FIFO that operates in parallel with GTFE64 FIFOs.

4. Send the data to the data acquisition board in a serial stream. GTRC chips in successive layers are daisy-chained in the readout, which is controlled by a token passed from bottom to top. Two 64-hit deep data buffers allow this to proceed in parallel with reading data from the GTFE64 chips into the GTRC chips.
5. External communication via low-voltage differential signaling (LVDS).

Prototypes of both custom chips have been tested and found to work according to design. The GTFE64 chip, however, has a problem with pickup between the digital clock and amplifiers. Individual clock swings are not seen, since the 20 MHz clock is well beyond the amplifier bandpass. There is pickup, however, when a readout is initiated and terminated, which prevents us from making use of the buffering to read out while the amplifiers are alive. To address this problem, a second prototype is presently being made in which the digital ground is completely removed from contact to the substrate. We are also investigating an SOI process as a possible replacement for CMOS26G process that we have been using.

The power consumption of the readout system has been measured in the laboratory [15]. For a pessimistic trigger rate of 12.5 kHz and assuming 400 bits read out per hybrid per event, the power consumed per channel is 213 μW, of which about 150 μW is consumed by the amplifiers and discriminators. This includes all of the power for transmitting clock and data around the hybrid circuit and the power for sending data to the data acquisition, as well as the power consumed in the GTFE64 and GTRC chips.

5. Test-beam results

In October 1997 a beam test took place at SLAC with a small GLAST tracker prototype. The beam was selected to be either electrons or gamma-rays with energies between 10 MeV and 40 GeV. The detector included an anti-coincidence system, a tracker/converter with 6 x, y planes, and a CsI calorimeter. The tracker/converter had the flexibility to change the radiator thickness from 0% to 6% X_0 and to arrange the silicon planes with spacings of 3 or 6 cm. The tracker planes were made of back-to-back single-sided silicon-strip detectors, one detector per view, with the exception of one plane that had five detectors chained together in one of the views to give a 30 cm ladder.

The test-beam experience allowed us to verify the analog electronics and detector performance in a realistic environment with actual particles.[5] It also served to validated our concept for a silicon-strip pair-conversion telescope by making detailed comparisons between the data and the Monte Carlo simulations. The most important result for the electronics was a measurement of the efficiency and occupancy of the five-detector module. The inefficiency was computed by extrapolating the tracks reconstructed with the other silicon planes to the five-detector module and counting the number of times that there silicon planes to the five-detector module and counting the number of times that there was no hit. The efficiency was at least 99.9% and showed little dependence on the bias voltage around the relevant thresholds (1–1.5 fC) (see Fig. 4). The noise occupancy, or probability that a single channel has a hit when a random trigger is sent, was measured to be lower than 5×10^{-5} for thresholds > 1 fC, satisfying the GLAST trigger requirements (as can be seen in Fig. 5).

The angular resolution of the telescope for gamma-rays was measured [19,20] by fitting the electron and the positron tracks and reconstructing the conversion. Fig. 6 shows the 68% and 95% containment angles for the reconstructed space-angle distribution for the configuration with 4% X_0 Pb foils and 3 cm separation between detector planes. The agreement between the data and Monte Carlo simulation is excellent. For a detailed explanation of the test-beam set-up and results see Ref. [10].

[5] The prototype readout chips used in the test beam did not have the digital functionality of the GTFE64 chip.

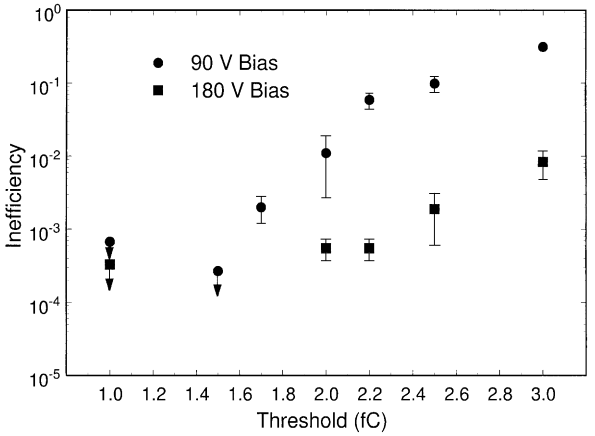

Fig. 4. Inefficiency of the five detector module versus the threshold level as a function of different bias voltages.

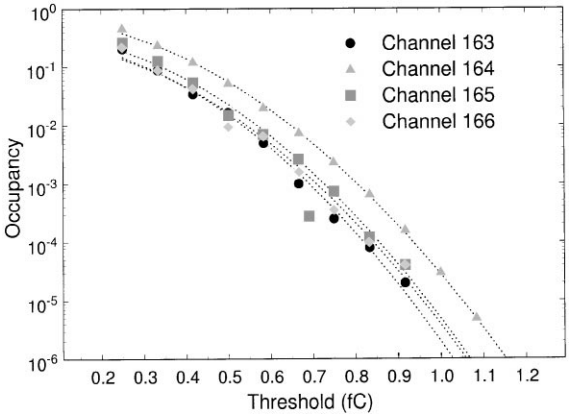

Fig. 5. Occupancy of some channels of the five detector module as a function of the threshold level. The dashed curves are Gaussian fits.

6. Conclusions

A complete conceptual design exists for a next-generation gamma-ray pair conversion telescope based upon silicon-strip detectors. The critical hardware components of the design have been prototyped and validated in the 1997 SLAC beam test, which demonstrated excellent agreement between the data and the simulations that have been used to develop and optimize the GLAST design.

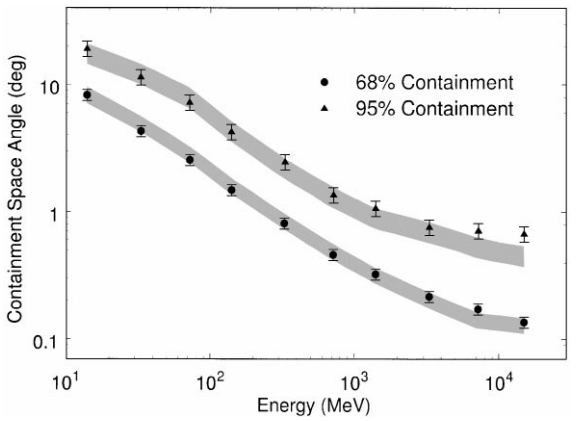

Fig. 6. 68% and 95% containment values of the angular resolution as a function of the gamma energy. The results correspond to the test-beam tracker configuration of 4% X_0 converters and 3 cm separation between silicon planes. The dots are the data and the bars the Monte Carlo simulation.

The NASA ATD program and SLAC are currently funding the construction of the first tower prototype, which is scheduled to be tested at the end of 1999. The full readout electronics chain for the silicon-strip tracker of the prototype tower, including two ASIC chips, has been successfully developed, and a complete hybrid assembly has been tested. The first tray is under construction and will be completed in December 1998, with construction of the remaining trays taking place during the spring of 1999 at SLAC and U.C. Santa Cruz. The GLAST mission itself has already been approved by NASA as part of their planning for the coming decade, with a launch tentatively scheduled for the end of 2004.

From the science point of view, GLAST will provide a flood of high quality data with which to study the high-energy gamma-ray sources in the universe. From the point of view of technology, GLAST will be one of the largest applications of the silicon-microstrip detector technique, in a different environment from the HEP accelerators for which it was initially developed.

References

[1] ATLAS collaboration, ATLAS technical Proposal, CERN/LHCC/94-43, December 1994. Web site: atlasinfo.cern.ch.

[2] CMS collaboration, CMS Technical Proposal. Web site: cmsinfo.cern.ch.
[3] J.J. Gomez-Cadenas, J.A. Hernando, A. Bueno, Nucl. Instr. and Meth. A 378 (1996) 196.
[4] J.J. Gomez-Cadenas, J.A. Hernando, Nucl. Inst. and Meth. A 381 (1996) 223.
[5] E. Bloom, G. Godfrey, S. Ritz, (Eds.), Proposal for the Gamma-Ray Large Area Space Telescope, SLAC-R-22, February 1998.
[6] W.B. Atwood et al., The gamma-ray large area telescope (GLAST), Nucl. Inst. and Meth. A 342, (1994) 302. Web site: www-glast.stanford.edu.
[7] G. Kanbach et al., Space Sci. Rev. 49 (1988) 69, Web. site: cossc. gsfc.nasa.gov/cossc/egret.
[8] M.G. Cawley, T.C. Weekes, Exp. Astron. 6 (1995) 7.
[9] G.B. Yodh et al., Space Sci. Rev. 75 (1996) 199.
[10] GLAST 1997 Test beam results, in preparation, Nucl. Instr. and Meth, to be submitted.
[11] J.A. Hernando, The Kalman filter technique applied to track fitting in GLAST, SCIPP 98/19, April 1998. For SCIPP notes see the web site: scipp.ucsc.edu/groups/glast.
[12] W.B. Atwood, design issues for GLAST silicon strip pair conversion telescope, SCIPP 97/31, May 1997.
[13] W.B. Atwood, T. Burnett, An object-oriented program for high-energy physics event simulation and reconstruction, Int. J. Modern Phys. C 2 (1992) 459.
[14] R.P. Johnson, The silicon-strip tracker for the GLAST prototype tower, SCIPP 98/28, August 1998.
[15] R.P. Johnson, P. Poplevin, H. Sadrozinski, E. Spencer, IEEE Trans. Nucl. Sci. 45 (3) (1998) 927.
[16] R.P. Johnson, Interface description for the GLAST front-end readout chip, GTFE64, SCIPP 98/26, August 1998.
[17] R.P. Johnson, Interface description for the GLAST tracker readout controller chip, GTRC SCIPP 98/26, August 1998.
[18] R.P. Johnson, GLAST tracker electrical and data acquisition interface, SCIPP 98/27, August 1998.
[19] B. Jones, Ph.D. Thesis, Stanford University, September 1998.
[20] R.P. Johnson, W. Kröger, Power consumption measurements of the GTFE64 and GTRC chips, SCIPP 98/30, September 1998.