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GLAST Tracker Electrical and Data Acquisition Interface

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Cable Connector Receptacle on the TEM Board

The receptacle on the TEM for each of the eight cables from the tracker tower is assumed to be a Nanonics horizontal surface mount, 37-pin single-row Dualobe plastic body connector. The pin-out is as follows:

1. RESET: hardware reset to the front-end chips and controller chips. Normally should be at digital ground potential. Set high for at least one clock period to produce a reset. Note that the RESET lines on the two cables on a given side of the tower are connected together by way of the hybrid circuits. Each hybrid has only a single RESET trace, which connects to both cables.
2. AVDD2: clean 2-volt analog supply for the front-end chips.
3. AGND: clean analog ground.
4. AVDD: clean 5-volt analog supply for the front-end chips.
5. DET_BIAS: bias potential for the detectors (approximately +100V). Should be referenced to the analog ground.
6. TEMP1/1: positive lead of the temperature monitor for one of the lowest four trays.
7. TEMP1/2: negative lead of the temperature monitor for one of the lowest four trays.
8. TEMP2/1: positive lead of the temperature monitor for one of the upper four trays.
9. TEMP2/2: negative lead of the temperature monitor for one of the upper four trays.
10. TOUTP8: output from differential FAST-OR signal of eighth (top) tray.
11. TOUTN8: complimentary output from differential FAST-OR signal of eighth (top) tray.
12. TOUTP7: output from differential FAST-OR signal of seventh tray.
13. TOUTN7: complimentary output from differential FAST-OR signal of seventh tray.
14. TOUTP6: output from differential FAST-OR signal of sixth tray.
15. TOUTN6: complimentary output from differential FAST-OR signal of sixth tray.
16. TOUTP5: output from differential FAST-OR signal of fifth tray.
17. TOUTN5: complimentary output from differential FAST-OR signal of fifth tray.
18. TOUTP4: output from differential FAST-OR signal of fourth tray.
19. TOUTN4: complimentary output from differential FAST-OR signal of fourth tray.
20. TOUTP3: output from differential FAST-OR signal of third tray.
21. TOUTN3: complimentary output from differential FAST-OR signal of third tray.
22. TOUTP2: output from differential FAST-OR signal of second tray.
23. TOUTN2: complimentary output from differential FAST-OR signal of second tray.
24. TOUTP1: output from differential FAST-OR signal of first (lowest) tray.

25. TOUTN1: complimentary output from differential FAST-OR signal of first (lowest) tray.
26. TACKN: complimentary trigger differential signal to all eight trays.
27. TACKP: trigger differential signal to all eight trays.
28. CLKN: complimentary clock differential signal to all eight trays.
29. CLKP: clock differential signal to all eight trays.
30. CMDN: complimentary command differential signal to all eight trays.
31. CMDP: command differential signal to all eight trays.
32. DATIN8: complimentary data differential signal from lowest tray.
33. DATIP8: data differential signal from lowest tray.
34. TOKON: complimentary token differential signal to lowest tray.
35. TOKOP: token differential signal to lowest tray.
36. GND: digital ground.
37. DVDD: 3V digital power.

Differential Signals

All differential signals are compatible with LVDS conventions, as long as approximately 3 V is used for the digital supply. The signals from the front-end controller chips (GTRC) are centered on one half the digital supply voltage, so if the digital supply were raised to 5 V, for example, then they would center on 2.5 V, which would violate the LVDS convention.

For the differential signals, a high logic state corresponds to the signal line being at a higher potential than the complimentary line.

Each differential signal going from the front-end controller chips to the TEM must be terminated by a 200-ohm resistor on the TEM placed between the two complimentary lines. 100-ohm termination resistors are present on the cables and hybrids for the differential signals sent from the TEM.

Power

The following table contains conservative estimates of the power requirements for a single side (eight readout sections) of one tower. Each tower side contains two cables, but the power leads and grounds in the cables are common. With the exception of the detector bias, the power passes through 250 mA fuses upon entry into the hybrid PC boards.

Name	Nominal Voltage	Minimum	Maximum	Quiescent Current at Nominal Voltage	Current at Nominal Voltage
Analog VDD	5 V	4.75 V	5.25 V	286 mA	286 mA
Analog 2	2 V	1.8 V	2.2 V	280 mA	280 mA
Digital VDD	3 V	2.9 V	3.3 V	162 mA	247 mA
Detector Bias	100 V	TBD	TBD	0.65 mA	0.65 mA