SCIPP 98/25
September, 1998

Interface Description for the GLAST Tracker Front-End Readout Chip, GTFE64

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Version 1.1

1. Prototype Chip Versions

- GTFE64A: first prototype.
- GTFE64B: second prototype. Command decoder bugs were fixed such that
  1. the decoder does not need a hard external reset after a load control register command is executed, and
  2. the internal line for transmitting the command data to the control register is disabled when the control register is not being clocked (to avoid introducing noise into the analog circuitry).
- GTFE64C: third prototype.
  1. The CAL pad was removed and the EINN, EINP, and EPON input pads were added.
  2. All connections between the digital ground and substrate were removed, and substrate ties were added to the digital circuitry and brought out to two new pads called SUBSTRATE.
  3. Logic was added to turn off the left FAST-OR input (TLIN and TLIP) when the chip address is 24 and turn off the right FAST-OR input (TRIN and TRIP) when the chip address is 0.

2. Bond pads.

Sizes:

- Channel Inputs: 100 μm × 100 μm
- Others: 100 μm × 150 μm

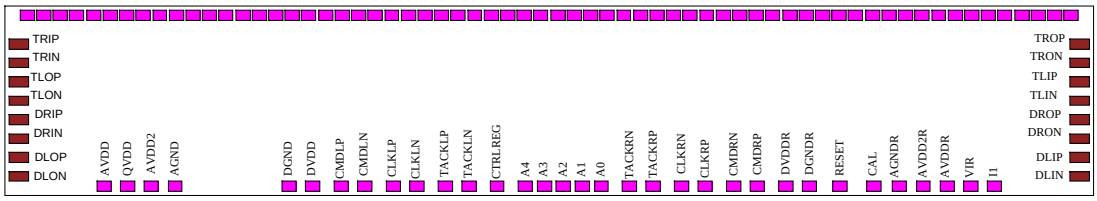


Figure 1. Bonding pad layout of the GTFE64B chip (not to scale). Channel 0 is on the left.

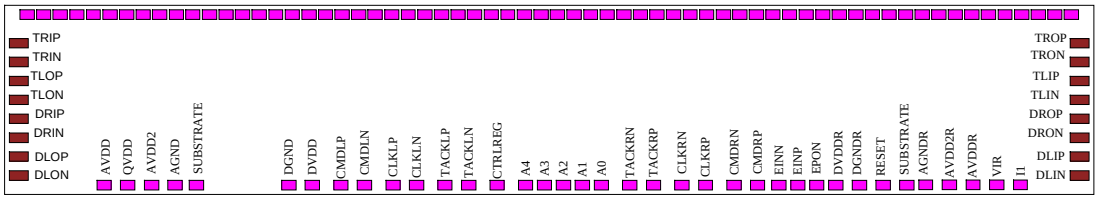


Figure 2. Bonding pad layout of the GTFE64C chip (not to scale). Channel 0 is on the left.

List of bonding pads:

- Front edge of chip (detector side, 64 pads):
  - ◊ 64 input pads.
- Right-hand edge of chip. (8 pads):
  - ◊ Fast-OR output. 2 pads. (TROP, TRON)
  - ◊ Fast-OR input. 2 pads. (TLIP, TLIN)
  - ◊ Data shift register output. 2 pads. (DROP, DRON)
  - ◊ Data shift register input. 2 pads. (DLIP, DLIN)
- Left-hand edge of chip. (8 pads):
  - ◊ Fast-OR output. 2 pads. (TLOP, TLON)
  - ◊ Fast-OR input. 2 pads. (TRIP, TRIN)
  - ◊ Data shift register output. 2 pads. (DLOP, DLON)
  - ◊ Data shift register input. 2 pads. (DRIP, DRIN)
- Back edge of chip (32 pads).
  - ◊ IREF pad. Reference current for amplifier bias.
  - ◊ AVDD2 pad (analog 2 volts). 2 pads, one on each end.
  - ◊ AVDD pad (analog 5 volts). 2 pads, one on each end.
  - ◊ QVDD pad (analog 5 volts for input transistor N-well).
  - ◊ DVDD pad (digital power). 2 pads, one on each end.
  - ◊ DGND pad (digital ground). 2 pads, one on each end.
  - ◊ AGND pad (analog ground). 2 pads, one on each end.
  - ◊ SUBSTRATE pad. *GTFE64C only*. (bond to analog ground) 2 pads, one on each end.
  - ◊ Hard-wired address. 5 pads. (A0…A4)
  - ◊ Command input left. 2 pads. (CMDLP, CMDLN)
  - ◊ Command input right. 2 pads. (CMDRP, CMDRN)
  - ◊ Clock for the command input, left. 2 pads. (CLKLP, CLKLN)
  - ◊ Clock for the command input, right. 2 pads. (CLKRP, CLKRN)
  - ◊ Trigger strobe, left. 2 pads. (TACKLP, TACKLN)
  - ◊ Trigger strobe, right. 2 pads. (TACKRP, TACKRN)
  - ◊ Control register output. 1 pad. (CTRLREG) This output is single-ended and tristate, since it will only be used for diagnostic purposes.
  - ◊ RESET. Force a reset of the command decoders. 1 pad.

- ◊ CAL. *GTFE64A and GTFE64B only*. Input an analog external calibration signal to override the internal calibration. For bench testing only.
- ◊ EINN, EINP pads. *GTFE64C only.* Differential digital calibration input. This provides a quieter way to introduce a calibration pulse (with the amplitude set by the internal DAC) than by way of the command decoders. For bench testing only.
- ◊ EPON pad. *GTFE64C only.* Turn on or off the EINN, EINP differential receiver.

3. Dimensions.

- Cut die size: 11.7 mm × 2.2 mm
- Active area: 11.4 mm × 2.0 mm

4. Commands.

Serial command format: 1cccaaaaa…data…

- Start bit: 1
- ccc: command: 3 bits, LSB first.
- aaaaa: address: 5 bits, LSB first. Wild-card address 1F addresses all chips simultaneously.
- Data: 207 bits for the load-control-register command only.

Notes:

- With the exception of the load-control-register, the chip ignores commands sent to the command input that has not been selected. Loading the control register is necessary for making or changing that selection.
- The load-control-register command should never be sent simultaneously to both command inputs (or else the control register will be loaded with rubbish).
- At least one zero must separate any two commands.
- The clock may be turned on well before sending the command, or the first clock rising edge may appear immediately after the first rising edge of the command.

Command Definitions

String	Name	Minimum Clocks	Data
000	No-Op	12	
001	Load-Control-Register	218	207 bits
010	Read-Event	10 + #output bits to shift (minimum 11 shifts)	
011	Calibration-Strobe	522	
100	Clear-Event	12	
101	Reset-Chip	12	
110	Reset-FIFO	12	
111	End-Read-Event	12	

5. Control register.

Contents (load starting with Bit 0)

Region	Bit Range	Explanation	Default	Default Value (hex)
Calibration Mask	0…63	0=ch 0 63=ch 63	Every other channel enabled	1111111111111111 ch 63 ← ch 0
Channel Mask	64…127	64=ch 63 127=ch 0	All enabled	FFFFFFFFFFFFFFFF
Trigger Mask	128…191	128=ch 0 191=ch 63	All enabled	FFFFFFFFFFFFFFFF
Calibration DAC V=5.4 mV + (DAC setting)×5.5 mV ***or*** V=18 mV + (DAC setting)×24.7 mV	192…198	192=range (set=high) 198=LSB	100 mV	0F
Threshold DAC (Same dependence as calibration DAC)	199…205	199=range (set=high) 205=LSB	150 mV	17
Left-Right Control Bit	206	set=right	Left	0

6. Calibration Pulse Height

The internal calibration capacitors are about 50 fF, so the calibration-DAC setting in mV should be multiplied by 0.05 to convert to fC of charge.

7. Amplifier Gain

The overall gain of the amplifier chain is approximately 126 mV/fC, so the threshold-DAC setting in mV may be converted to fC by dividing by this amount.

8. Power.

External Supplies Needed and
Power Consumption Estimates

	Digital (DVDD)	Analog 5V (AVDD)	Analog 2V (AVDD2)
Level	3.0–3.5 V	5.0±0.2 V	2.0±0.2 V
Current	Quiescent: 0.42 mA Peak: 0.60 mA	1.3 mA	1.6 mA
Power	Quiescent: 1.3 mW Peak: 1.8 mW	6.5 mW	3.2 mW

Note: the peak digital power assumes a 12.5 kHz trigger rate and 400 hits per readout section per trigger.

9. Signal levels.

Approximate Levels for the Digital Signals

Name	In-Out	Type	Low	High	Internal Bias	Internal Termination
Clock	in	pseudo-LVDS	1.3 V	1.7 V	None	None
Commands	in	pseudo-LVDS	1.3 V	1.7 V	None	None
Trigger	in	pseudo-LVDS	1.3 V	1.7 V	None	None
Fast-OR	in	pseudo-LVDS	1.3 V	1.7 V	None	~50 kΩ
Fast-OR	out	pseudo-LVDS	1.3 V	1.7 V		
Data	in	diff-CMOS	0	3 V	None	None
Data	out	diff-CMOS	0	3 V		
Address	in	CMOS-static	0	3 V	None	None
Control Reg	out	CMOS-tristate	0	3 V		
Reset	in	CMOS	0	3 V	Low	None
EPON	in	CMOS	0	3 V	Low	None
EINN, EINP	in	LVDS			None	None

- The RESET input is active high (set high for at least 50 ns to force a reset of the command decoder).
- The EPON input is set high to enable the EINN and EINP inputs.
- The Control Register output (CTRLREG) is enabled only if the chip is uniquely addressed by the load control register command. In that case, the previous contents of the register are output in a serial stream.

10. Clock.

- Two redundant differential inputs (CLKRN & CLKRP, or CLKLN & CLKLP).
- Both inputs are always enabled.
- May be turned off when commands are not being executed.
- The command input is latched when CLKRP (or CLKLP) goes high.

	Clock Frequency	Phase w.r.t. Commands	Duty Cycle
Nominal	20 MHz	–10 ns	50%
Minimum	1 Hz	TBD	TBD
Maximum	TBD	TBD	TBD

11. Trigger Strobe.

- Two redundant differential inputs (TACKLP & TACKLN, or TACKRP & TACKRN).
- Only one input is enabled at a given time, according to the left-right selection bit in the control register.

- Asynchronous signal. Only the leading edge is used (TACKLP or TACKRP going from low to high).
- For 100% efficiency in latching data at the comparator output, the trigger should be received about 1.3 μs after the occurrence of a Fast-OR.
- Data for up to 8 triggers can be buffered on the chip pending readout.

12. Fast OR.

- Two redundant differential outputs (TROP & TRON, or TLOP & TLON).
- Two redundant differential inputs (TRIP & TRIN, or TLIP & TLIN).
- The unused Fast-OR inputs and outputs are disabled, depending on the setting of the Left-Right control bit in the control register and the chip address. (The dependence on the chip address is implemented starting only in prototype C.)
  - ◊ TRIN, TRIP are powered on only if the Left-Right control bit is set AND the chip address is not 0.
  - ◊ TRON, TROP are powered on only if the Left-Right control bit is set.
  - ◊ TLIN, TLIP are powered on only if the Left-Right control bit is not set AND the chip address is not 24.
  - ◊ TLOP, TLON are powered on only if the Left-Right control bit is not set.
- The output is a logical OR of the 64 comparator outputs, after the trigger mask, and the Fast-OR input.
- Inputs self bias to logic zero if left unconnected.
- Termination required between output pairs: roughly 50 kΩ. This is provided by the corresponding inputs.
- Asynchronous signal.
- Pulse length: measure of the greatest time-over-threshold of the 64 channels and the Fast-OR input.

13. Data format.

Two Cases:

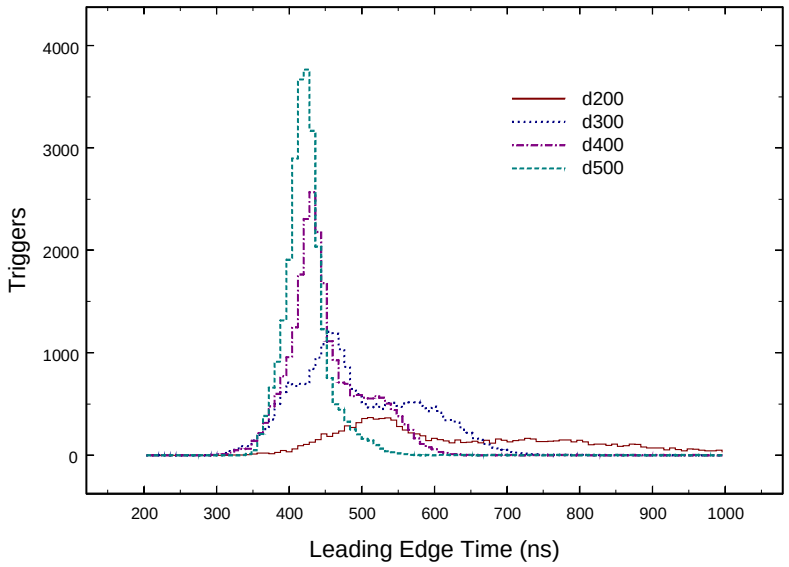
- No channels over threshold. Only a single zero bit is output.
- At least one channel over threshold. Output a one bit, followed by 64 bits, one for each channel. A one bit indicates a channel over threshold.
  - ❑ Shift left: first channel output is channel 0.
  - ❑ Shift right: first channel output is channel 63.

14. Input Protection

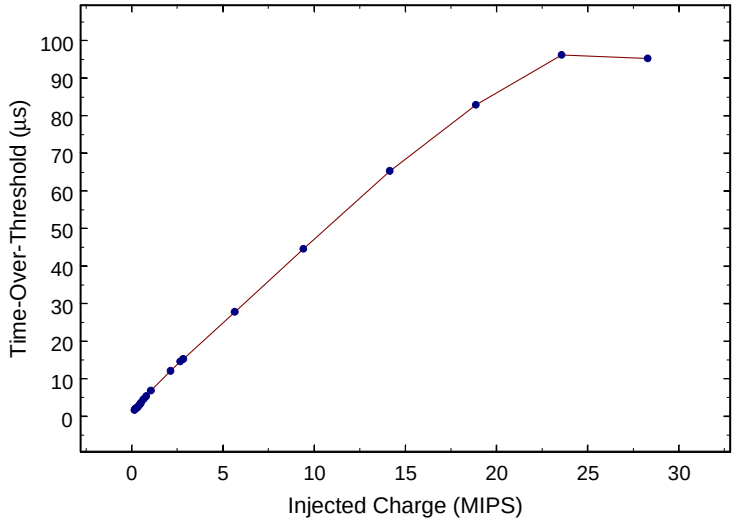
Diode protection structures are present on all analog and digital input pads.

15. Timing

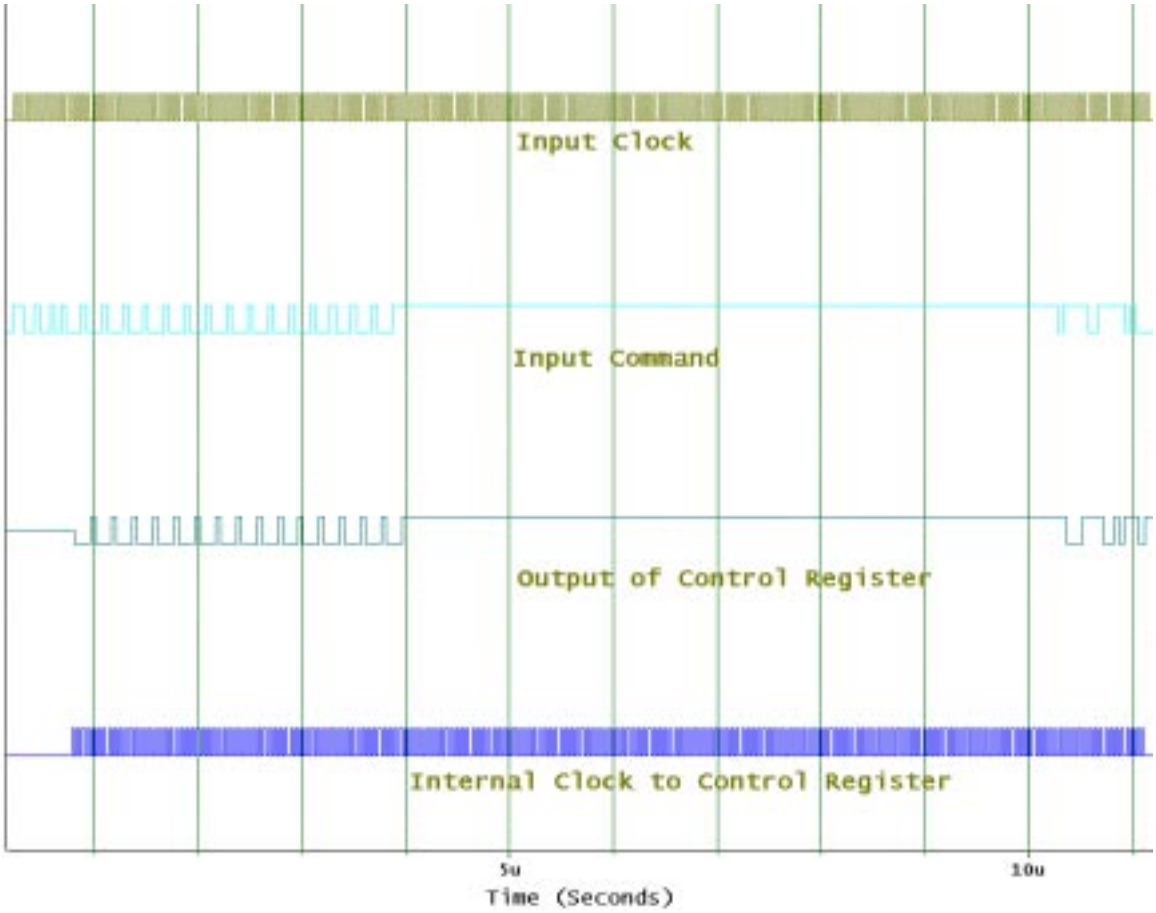
- Fast-OR peaking time. Shown below is the measured time of the leading edge of the Fast-OR signal from high-energy electrons in the October 1997 beam test at SLAC.



- Fast-OR time-over-threshold. Shown below is the measured time-over-threshold of the Fast-OR signal versus the injected charge. The maximum time-over-threshold is about 95 μs.



- Simulation of the load control register sequence. A specific address (09) is used, so the CTRLREG output driver is enabled. Note that the previous contents, the default values, of the control register are output as it is loaded.



- Simulation of the calibration and read event sequence. The calibration mask was previously initialized (by the load control register sequence shown above) such that every fourth channel is pulsed. The command stream shown here uses the 1F wildcard address in all cases. Note that the input trigger is asynchronous and in this example was set to occur roughly one microsecond after the calibration injection.