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Interface Description for the GLAST Tracker Readout Controller Chip, GTRC

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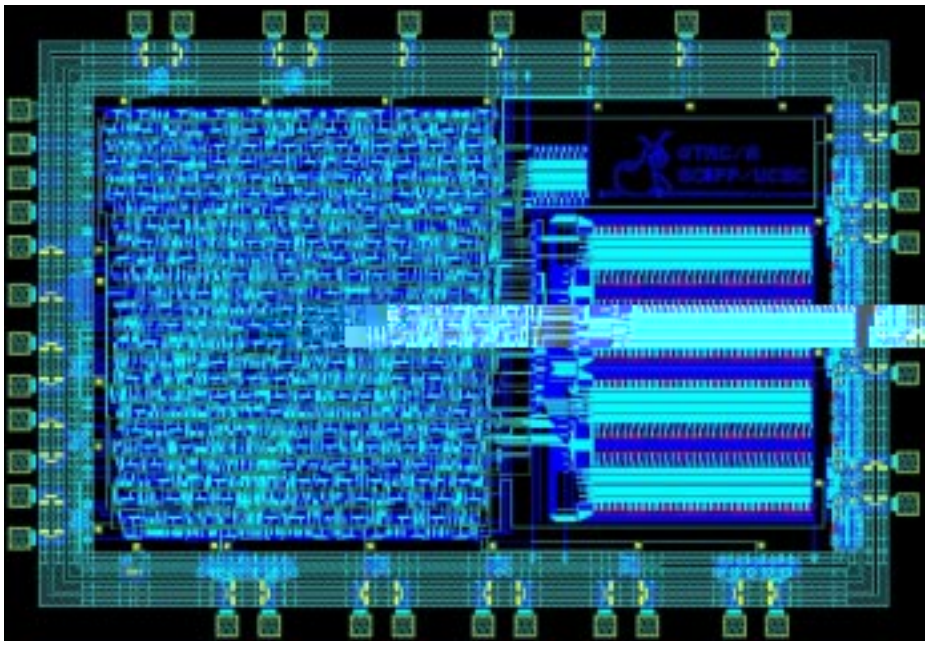

Figure 1. Drawing of the actual layout of the GTRC chip.

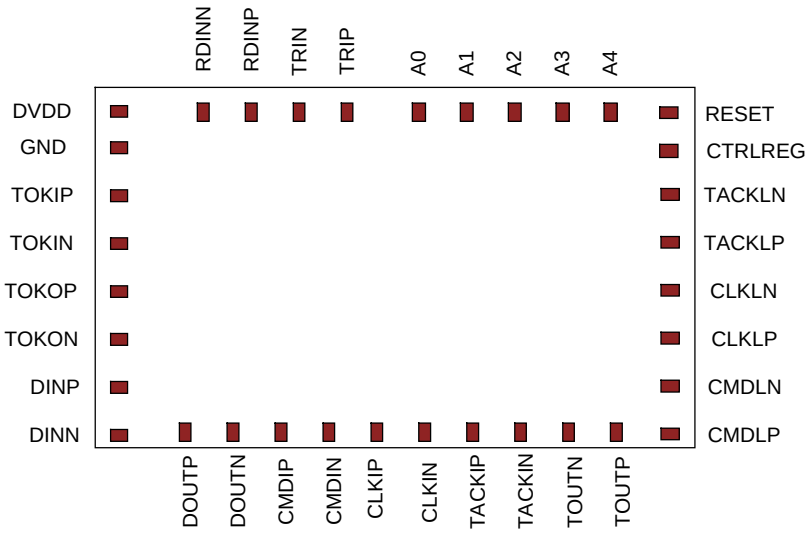

Figure 2. Bonding pad layout of the GTRC chip (not to scale). The two scan-chain debugging pads between GND and TOKIP are not shown. In addition, the double pads for DVDD and GND are shown as single pads.

1. Versions

- GTRC-A: First prototype. Has a short from VDD to substrate in the logo, and the external reset is active low.
- GTRC-B: Second prototype. External reset changed to active high.

2. Bond pads

- Size: 100 μm × 100 μm.
- Layout: see Figure 2.

List of bonding pads:

- DVDD: power; two pads, both of which must be bonded.
- DGND: ground; two pads, both of which must be bonded.
- A0–A4: chip address (programmed by connecting to power, for logic 1, or ground, for logic 0).
- RESET: external chip reset.
  - GTRC-A: Active low—lower to DGND to force a reset of the entire chip.
  - GTRC-B: Active high.
- CLKIN, CLKIP: clock input from the tower electronics module (TEM).
- CMDIN, CMDIP: command input from the TEM.
- TACKIN, TACKIP: level-1 trigger strobe from the TEM. *Note that in GTRC-A this signal is inverted internally, so the complement should be sent to GTRC (TACKIP should go low to signal a trigger).*
- TOKIN, TOKIP: token input from the layer below (or the TEM). *Note that this signal must be at least two clock periods long!*
- TOKON, TOKOP: token output to the layer above.
- DINN, DINP: data input from the layer above.
- DOUTN, DOUTP: data output to the layer below (or the TEM).
- CMDLN, CMDLP: commands output to the front-end readout chips.
- CLKLN, CLKLP: clock output to the front-end readout chips.
- TACKLN, TACKLP: level-1 trigger output to the front-end readout chips.
- RDINN, RDINP: data input from the front-end readout chips.
- TRIN, TRIP: Fast-OR input from the front-end readout chips.
- TOUTN, TOUTP: Fast-OR output to the TEM.
- CTRLREG: control register contents from any one of the front-end readout chips.
- Two additional pads located between ground and TOKIP are used to operate a scan chain for debugging of the chip. They should not normally be bonded out.

3. Signal Conventions

In general, for the differential signals logic 1 corresponds to the signal labeled P being higher in potential than the signal labeled N. The TACKIN/TACKIP pair is a special case in that it must be at least two clock periods long in order to be recognized.

4. Clock.

- Differential input (CLKIN & CLKIP).
- It is foreseen to be running continually.
- The same clock is fanned out to the 25 front-end readout chips (CLKLN, CLKLP), but only during execution of a command.

	Clock Frequency	Phase w.r.t. Commands	Duty Cycle
Nominal	20 MHz	−10 ns	50%
Minimum	1 Hz	TBD	TBD
Maximum	TBD	TBD	TBD

5. Power.

Required External Supplies and
Power Consumption Estimates

	Digital (DVDD)
Level	3.0–3.5 V
Current	Quiescent: 5.3 mA Total: 7.9 mA
Power	Quiescent: 16 mW Total: 26 mW

The values given here correspond to the first chip in the tower (address 0). The other chips use about 0.7 mA less quiescent current, because of less power being used for the data output drivers. The clock-related power is based upon measurements made at a 12.5 kHz readout rate, but it is only very mildly dependent upon the data volume and trigger rate.

6. Dimensions.

- Cut die size: 4.6 mm × 3.2 mm
- Active area: 4.316 mm × 2.968 mm

7. Data Format.

Each packet consists of a start bit followed by a variable number of 11-bits words:

- Start bit—a single 1.
- Layer address (5 bits), followed by the number of hits (6 bits) counted starting with 1.
- Error flag (1 bit), followed by time-over-threshold (10 bits).
  - ◊ Error flag bit: did an error occur during the readout? 1=error.
- Sequence of hits, each hit consisting of an 11-bit channel address (5 bits for the readout-chip number followed by 6 bits for the channel within the chip).
- 11-bit Frame-Check Sequence for the Cyclic Redundancy Check. This can be turned off via the control register when not needed, to improve the readout speed.

8. Cyclic Redundancy Check (CRC)

If enabled in the control register, an 11-bit Frame-Check Sequence (FCS) is appended to the data packet. To check whether any bit errors occurred in the data transmission, the data packet (frame) together with the FCS should be divided by the "polynomial" $x^{11} + x^9 + 1$ (*i.e.* by the bit pattern 101000000001). If the remainder is not zero, then there is an error in the frame.

9. Time-Over-Threshold Encoding

The time-over-threshold counter runs at a speed that is 4 times less than the clock speed. Therefore, at the nominal 20 MHz clock speed, each count is 200 ns and the maximum range of 10 bits corresponds to 204.8 μs.

10.Address.

Any 5-bit address, except 11111, may be programmed by bonding the pads A0 through A4 to power (logic 1) or ground (logic 0). The address 11111 is reserved as a wild-card address for commands to be sent simultaneously to all chips. In addition, address 00000 is special. If the chip is programmed to that address, then the data output driver will operate at 10 times the normal current. That is intended only for the controller chips in the lowest plane of the tower, which must send the data all the way past the calorimeter to the tower electronics module.

11.Commands.

Serial command format: 1aaaaaccc…data…

- Start bit: 1
- Address: 5 bits, LSB last. Wild-card address 11111 addresses all chips simultaneously.
- Command: 3 bits, LSB last.
- Data: length differs from one command to another.

Note: at least one zero must separate any two commands.

Command Definitions

String	Name	Data
000	Load GTRC control register.	8 bits.
001	Clear event.	
010	Read event.	
011	Load the control register of a front-end chip.	Complete command string for the front-end chips, *including the start bit, command, address, and contents.*
100	Turn on the clock to the front-end chips.	
101	Send calibration strobe to the front-end chips.	Complete calibration strobe command string for the front-end chips, *including the start bit, command, and address.*
110	Send RESET or RESET-FIFO command to the front-end chips.	Complete command string for the front-end chips, *including the start bit, command, and address.*
111	Reset the GTRC chip.	

12. Control register.

Contents (load starting with Bit 0)

Bit Range	Explanation	Default	Default Value
0	Not used.		1
1	Read layer even if Fast-OR was not generated?	Yes	1
2	Calculate 11-bit CRC?	Yes	1
3…7	Number of FE chips to read. Bit 3 is the MSB.	5 chips	00101

When the control register is loaded, the previous contents appear on the data output line, first-in-first-out.

13. Signal levels.

Approximate Levels for the Digital Signals, assuming DVDD=3.0 V.

Name	In-Out	Type	Low volts	High volts	Quiescent Current	Termination
Clock, Commands, Trigger	in	Commercial LVDS chips	≈1.0	≈1.4	≈4 mA	End of cable, ≈100Ω
Clock, Commands, Trigger to front-end	out	Pseudo-LVDS	1.2	1.8	0.6 mA	On hybrid. ≈1 kΩ
Token daisy chain	in/ out	LVDS	1.4	1.6	0.2 mA	On hybrid ≈1 kΩ
Fast-OR	in	pseudo-LVDS	1.3 V	1.7 V	0.03 mA	~12 kΩ internal
Fast-OR	out	LVDS	1.4	1.6	1 mA	TEM, ≈200 Ω
Data from FE chips	in	diff-CMOS	0	3 V	0	None
Data daisy chain	in/ out	LVDS	1.4	1.6	1 mA or 0.2 mA	200 Ω on TEM or 1kΩ on hybrid
Address	in	CMOS-static	0	3 V	0	None
Reset	in	CMOS	0	3V	0	None
CTRLREG	in	CMOS	0	3V	0	None

Some more testing is still required to determine whether the termination values given here will work well in practice.

14. Known Bugs

GTRC-A

- There is a short between VDD and substrate (about 50 ohms) by way of the slug logo. It has been removed on all 25 chips with an IR laser.
- The external reset is active low, while that of the front-end chips is active high.
- When the control register of a front-end chip is loaded, the last bit that is returned from the front-end chip does not appear on the GTRC data output.

GTRC-B

- When the control register of a front-end chip is loaded, the last bit that is returned from the front-end chip does not appear on the GTRC data output.

15. Operation

- ***Trigger***

At initialization time, each front-end chip on each hybrid is told (by loading its control register) whether it should pass data and Fast-ORs to the left-hand controller or the right-hand controller. Depending on the setting, when a hit occurs in any one or more of its unmasked channels, it sends to the chip on the right or the left a logical OR of its own Fast-OR with the one it received from the previous chip. Thus each controller receives on its Fast-OR input a logical OR of the outputs of all unmasked comparators on the front-end chips for which it is responsible. That Fast-OR is immediately (asynchronously) sent down the tower to the TEM.

The Fast-OR input is also used to clear and start a time-over-threshold counter in the controller chip. At the same time a five-bit trigger latency counter is started. The time-over-threshold counter stops when the Fast-OR input goes low again or when it reaches its maximum count. The latency counter stops after 32 counts or when a trigger signal is received from the TEM.

The TEM takes all of the Fast-OR signals from the tower and generates the final trigger. When such a trigger occurs, a trigger signal is sent to all controller chips in the entire GLAST tracker. The controllers on the hybrid process the trigger as follows:

- When the signal is received, it is immediately fanned out to the front-end chips on the hybrid to latch their comparator outputs.
- The contents of the time-over-threshold counter are loaded into a FIFO buffer that has the same depth (8) as the FIFO buffers on the front-end chips. If the counter is still running when the trigger is received, as would usually be the case, then the chip waits until the counter stops before storing the results.

An exception to this processing can occur if bit number one in the control register is not set, in order to operate in the mode where data are read from a readout section only if that section produces a fast-OR signal. Then, if the trigger is received while the latency counter is not counting, the latch signal is not sent to the front-end chips, the time-over-threshold is not latched, and the controller chip does not report any data for that event.

The front-end chips respond to a trigger signal by latching the outputs of their discriminators into their event FIFO buffers. The TEM must keep track of how many trigger signals versus read-event commands have been sent, in order to be able to disable the trigger whenever the event and time-over-threshold buffers are full. Also, the trigger logic must respond quickly enough such that the trigger signal reaches the front-end chips while the comparator outputs are still high (about 1.3 μs minimum time-over-threshold).

The following figures illustrate some details of the trigger and time-over-threshold operation:

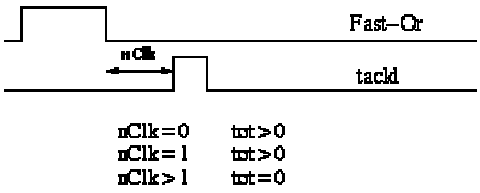

Figure 3. If the trigger signal arrives more than two clock cycles later than the falling edge of the Fast-OR signal, then the time-over-threshold is set to zero. Except for pulses that barely rise above threshold, the trigger signal will arrive well before the falling edge of the Fast-OR.

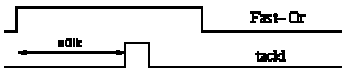

Figure 4. The trigger latency counter is only used if bit-one of the control register is not set. In that case, if the trigger signal arrives more than 32 clock cycles after the rising edge of the Fast-OR signal, then the time-over-threshold is set to zero. If bit-one is set, then the time-over-threshold value always corresponds to the Fast-OR width, independent of whether the latency counter has expired.

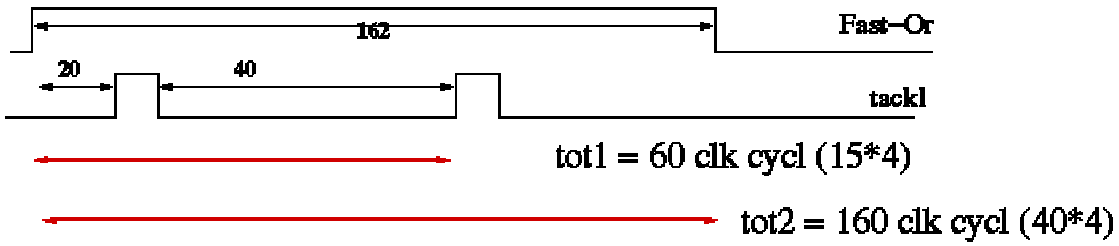

Figure 5. If a second trigger signal arrives before the Fast-OR from the first event has fallen, then the time-over-threshold for the first event is the time from the rising edge of the Fast-OR to the rising edge of the second trigger signal. The time-over-threshold for the second event is the full pulse length of the Fast-OR.

- ***Readout Sequence***

At an arbitrary time following the trigger, the readout sequence is initiated by sending a read command to the controller chips. Each of them responds by pulling the time-over-threshold from the FIFO buffer and sending a read-event command to the front-end chips (unless bit-one of the control register is not set *and* the trigger did not arrive while the latency counter was active). The front-end-chip read-event command causes an event to move from the front-end-chip FIFO into the data output shift register, after which the clock is directed to the shift register to move the data toward the controller chip. Another command, end-read-event, is sent by the controller chip at the appropriate time to turn off the clock to the shift register. During all of the intervening time, the controller chip continues to supply a clock to the front-end chips. How many clocks are needed to shift the data depends on how many front-end chips the controller is programmed to read and on the data itself.

As the data are clocked in, the controller keeps a chip counter and a hit counter going and latches the counts each time a hit is detected, for up to a maximum of 63 hits. Those hits are stored in one of two 63-deep buffers, alternating from one buffer to the next with each new event.

The format of the data that are shifted out of the front-end chips is

- Header bit: 1 if the chip has any hits, 0 if no hits.
- Data bits: none if the chip has no hits, 64 if the chip has at least one hit.

The controller chip first looks at the header bit. If it is zero, then it increments the chip counter and looks at the header bit from the following chip. On the other hand, if it is a one, then it starts up the hit counter and counts while clocking in the next 64 data bits, latching the hit counter each time a one is detected. Then it increments the chip counter and goes on to the next header bit, and so forth. The readout ends when the data from the last chip have been read or when the event buffer is filled (63 hits).

Movement of the data from the controller chips into the TEM is initiated by the TEM by sending a token to the first controller chip, which responds by sending its data to the TEM as soon as it has finished reading from the front-end chips. When it has finished sending its data out, it passes the token to the controller chip on the layer above, giving it permission to send its data out on the serial line. Each controller has two event buffers, so that while it is sending data it can receive another read-event command and begin clocking the next event out of the front-end chips. Therefore, a second read-event command may be sent before the previous event has been read out of the controller chip. The controller chips hold the pending read-event command until the data from the previous event have all been clocked out of the front-end readout chips. They then begin clocking out the next event. The TEM is responsible for keeping track of whether or not a buffer is free in the controller chips. What that means in practice is that it should never send a *third* read-event command until all of the data from the first one have been received.

Also, there may be a delay between the time that the token is sent to a controller chip and the data start coming out, in the case that the chip has not finished clocking the bits from the front-end chips. The controller chip holds the token until it is ready.

When a controller has finished sending its data packet, it passes the token on up to the next layer. When it is not in possession of the token, whatever it sees on its data input port (from the next layer) it passes to its data output port on the following clock cycle. If a chip has no data for the given event, it still sends the first 11-bit word, consisting of the layer number and the number of hits, which is zero in such a case. This allows the TEM to know when the readout is complete—it just has to wait for the last layer to report its data. It is the responsibility of the TEM to ensure that an event has been completely read out before a token is sent to initiate the readout of the following event.

The following points should be kept in mind when operating the GTRC chip:

- A token may be sent immediately after issuing a read-event command. The GTRC chip holds the token until it is ready to send the data.
- Two read-event commands may be send one immediately following the other, or with a token sent in between or simultaneous with the second read-event command. The TEM must wait until the first event is completely read out before sending either the third read-event command or the second token. The third read-event command and the second token may be sent simultaneously.

- A token should never be sent while the GTRC chips are outputting data.
- The token for a given event cannot be sent simultaneous or prior to the read-event command for the same event.
- The chip counter starts at 1, rather than at 0, so the addresses of hits in the first front-end chip to be read out have a 1 for the chip number.

- ***Initialization***

Reset the chip and, if necessary, load the control register. When the control register is loaded the previous contents appear on the data output lines. Therefore, repeat the load control register operation if it is desired to verify that the correct data are loaded.

Load the control registers of the front-end chips that will send data to this controller chip (see Figure 6 for the timing diagram). If the front-end chips are addressed individually, as would normally be the case, then the previous contents appear on the controller chip data output lines. The left-or-right bit of the front-end chip control register must be set to direct the output data toward the controller chip being initialized.

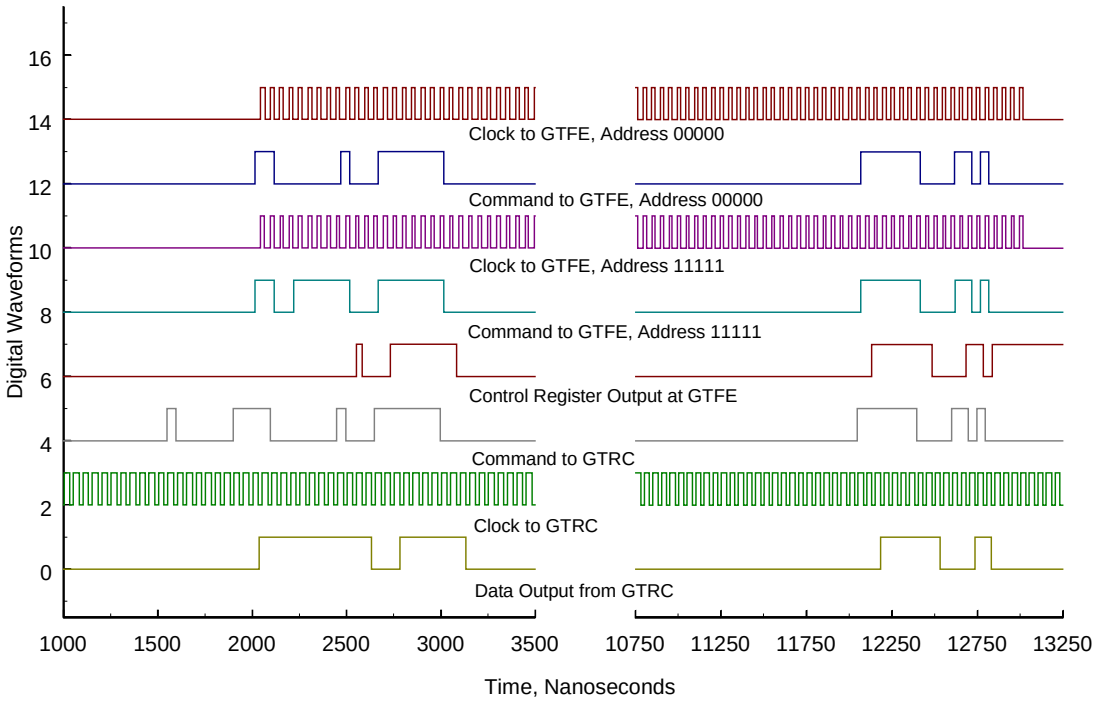

Figure 6. Timing diagram for the initialization of the front-end readout chip control register, as measured with a logic analyzer. Lines 8 and 10 correspond to the case in which the 11111 wild-card address is used for the front-end chips and there is no output from the control register. All other lines correspond to address zero. Note that the GTRC output is missing the last bit from the control register.

- ***Calibration Run***

During the initialization procedure, set up the front-end chip calibration masks to determine which channels should be pulsed (not more than 64 per controller chip). Also, set the DAC bits in the front-end chip for the calibration pulse height. All of these bits are in the control register of the front-end readout chip.

Send a calibration-strobe command to the controller chip. About 1 μs later send a trigger pulse to the controller chip. After some arbitrary length of time, send a read-even command to the controller chip, followed by a pulse on the token line. An example of such a read sequence is shown in Figure 7. The controller chip address is 00000, while the address 11111 is used to broadcast the read command to the GTFE64 chips. The GTRC chip automatically generates the clock and command signals for the GTFE64 chips. The data stream that comes back is a start bit followed by

Word	Bits	Interpretation
1	00000000101	Address 00000, 5 hits
2	00010000110	No error, TOT=134
3	00001000000	Chip 1, Hit address 0
4	00001001011	Chip 1, Hit address 11
5	00001010110	Chip1, Hit address 22
6	00001010111	Chip 1, Hit address 23
7	00001011000	Chip 1, Hit address 24

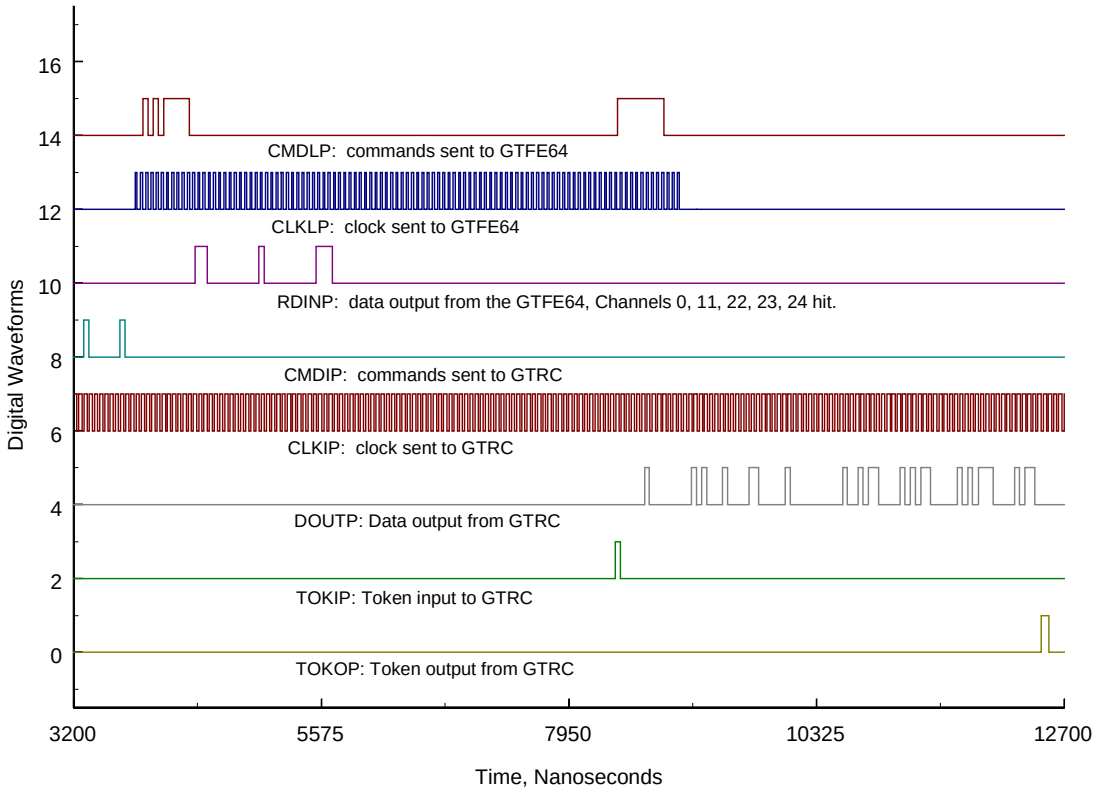

Figure 7. Timing diagram for an example readout sequence, as measured with a logic analyzer. The initialization sequence for setting the calibration mask (to pulse only channels 0, 11, 22, 23, and 24) and the calibration DAC is not shown. Also not shown are the calibration strobe command used to inject charge and the trigger strobe used to latch the data.