# Power Requirements for the GLAST Tracker Electronics 

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Since we have in hand prototypes of the complete GLAST tracker front-end readout chip (GTFE-64) and the readout controller chip (GTRC), it is interesting to update our tracker power estimates on the basis of actual data. The amplifierdiscriminator power has been well known already for some time. The only news there is that the discriminator current increased by about $10 \mu \mathrm{~A}$ per channel with respect to the beam-test-chip, because of a modification needed to increase the threshold range. There is a good possibility, however, that that can be recovered in a future version. There may also be some room for reduction of the analog power, which has not been fully optimized up to this point.

The prototypes have given us the first opportunity to measure the digital power consumption of the front-end chip and the controller chip. Those measurements are detailed in a recent note. ${ }^{1}$ The results depend on the data rate. For this note, we assume a conservative $12.5-\mathrm{kHz}$ level- 1 trigger rate and 150 bits per readout section per event. That would correspond to reading data from roughly 2 chips out of the 25 in the readout section, which is reasonable, considering the anticipated stochastic noise rate. ${ }^{2}$ The controller chip power depends weakly on the data rate, being dominated by quiescent power used in the drivers and receivers and by clock-related power used within the chip. There has been up to now some uncertainty in the termination requirements for the transmission lines. We would like not to have to terminate the $32-\mathrm{cm}$ long PC-board traces going from the controller chips to the front-end chips at their characteristic impedance. For the present note we are assuming 1000 -ohm termination. That appears to work well in preliminary tests done so far with a single GTFE-64 chip plus a controller chip mounted on a full-length hybrid.

The results are presented in the following spreadsheet. The bottom line, averaged over a full tower, works out to be $215 \mu \mathrm{~W}$ per channel. ${ }^{3}$ That exceeds by $8 \%$ our stated goal of $200 \mu \mathrm{~W}$ per channel. If we decide in the future to add a second discriminator per channel, to improve control over the triggering, that would add about $15 \mu \mathrm{~W}$ per channel to the power consumption. Other than that, the needed contingency should be small, since these power requirements are derived from measurements on actual prototypes. In

[^0]addition, there is considerable room for improvement through further development on both the analog and digital sides.

Table 1. Spreadsheet for compilation of the power consumption in the tracker tower.

|  | Analog 2V Current (mA) | Analog 5V Current (mA) | 3 V Current (mA) | 120 V <br> Detector <br> Bias (mA) | $\begin{array}{\|l} \text { Power } \\ (\mathrm{mW}) \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Front-End Chip |  |  |  |  |  |
| Input transistor bias | 1.40 |  |  |  | 2.80 |
| Amplifiers and bias circuit |  | 1.43 |  |  | 7.15 |
| Quiescent digital power |  |  | 0.44 |  | 1.32 |
| Clock-related digital at 12.5 kHz and 150 hits per readout |  |  | 0.06 |  | 0.18 |
| Subtotal: | 1.40 | 1.43 | 0.50 |  | 11.45 |
|  |  |  |  |  |  |
| Controller Chip, address 0 |  |  |  |  |  |
| Quiescent |  |  | 5.30 |  | 15.90 |
| Clocked |  |  | 3.38 |  | 10.14 |
| Subtotal: |  |  | 8.68 |  | 26.04 |
|  |  |  |  |  |  |
| Controller Chip, other addresses |  |  |  |  |  |
| Quiescent |  |  | 4.60 |  | 13.80 |
| Clocked |  |  | 3.30 |  | 9.90 |
| Subtotal: |  |  | 7.90 |  | 23.70 |
|  |  |  |  |  |  |
| Bottom Readout Section |  |  |  |  |  |
| Front-End Chips | 35.00 | 35.75 | 12.50 |  | 286.25 |
| Controller Chips |  |  | 17.36 |  | 52.08 |
| Detector Bias: |  |  |  | 0.080 | 9.60 |
| Subtotal: | 35.00 | 35.75 | 29.86 | 0.080 | 347.93 |
|  |  |  |  |  |  |
| Readout Section |  |  |  |  |  |
| Front-End Chips | 35.00 | 35.75 | 12.50 |  | 286.25 |
| Controller Chips |  |  | 15.80 |  | 47.40 |
| Detector Bias (end of life): |  |  |  | 0.080 | 9.60 |
| Subtotal: | 35.00 | 35.75 | 28.30 | 0.080 | 343.25 |
|  |  |  |  |  |  |
| Half Tower (16x or 16 y) | 560.00 | 572.00 | 454.36 | 1.280 | 5496.68 |
| Half tower quiescent | 560.00 | 572.00 | 324.60 | 1.280 | 5107.40 |


[^0]:    ${ }^{1}$ Wilko Kröger, "Power Consumption," SCIPP 98-34.
    ${ }^{2}$ The occupancy required by the trigger would indicate less than one chip per readout section with noise hits, but we may wish to allow more noise in the data readout than is allowable for the trigger. The actual data volume will therefore depend on to what degree we choose to mask noisy channels from the data, among other things.
    ${ }^{3}$ It should be kept in mind that the power requirements considered here are for fully conditioned power.

