# Linear Collider Chip: LCFE
# Notes on Prototyping

## Two Thresholds

Minimum charge threshold estimate 0.29 * 4fC = 1.16fC for VthH

4 fC taken to be minimum ionizing track charge

142 mV at charge of 1.16 fC, most likely High threshold

Range of 0.4 – 0.7 is likely, but calibrate 0.4 – 1 fC

VthL will not be below 50 mV (1/3 of 142mV), so channel gain is in good range

## Noise

Capacitive load in sim: 200 pF
cot(arccos.8 ) * 125 cm
167 cm * 1.2 pF/cm = 200 pF, optimize to this
Target shaping time signal/noise purposes: 1-10 usec
Shaping time for power consideration: 3-3.5 usec
*4 noise params:*

1) Input Transistor dimensions and layout, 4pF input gate capacitance, 200 ohm channel resistance at bias
2) Bias current : 240 uA

3) Shape optimum?
4) Always noise limited

## Channel Crosstalk

Pitch: 50 um
Prototype is 237 um, 10 cm sections
2% dominated by channel capacitance?
BaBar has ~~5% crosstalk
*Need network parameters of detector:*
Metal linear resistance
1st Neighbor unit capacitance
2nd Neighbor unit capacitance
Backplane unit capacitance
Strip AC coupling unit capacitance (unimportant?)
Doped strip unit resistance
Amplifier input impedance
Detector strip length

Electronic crosstalk: Can the amplifier input impedance be more aggressive?
(Do not spend too much time on this.)

## Power

Rate for Warm Proposal: 120 Hz, 300 ns time window, 200 buckets
Rate for Cold Proposal: 5 Hz, long signal 2 msec
Front biased at 360 uA @ 1.3 V
.38 mA *1.3 V * 0.015 = 7.4 μW/channel analog
$10^6$ channel => 14 W detector for analog
(We ought to be able to cool this!)
Surface area, gas flow needed to specify target power.

## G&S

Pickup from power cycling: we have a triggered system

Chip Readout
Use standard LVDS drivers and receivers
Interface with Xilinx
No channel compression
Put LVDS in separate power section. Define inputs when front power is off.
LVDS are not part of power budget.

## Timing Signals for Turn-on Time Minimum

There are four timing signals for turn-on. These signals will need to adjustable for turn-on time optimization. Best turn-on time is ~70 us, so this time dominates the power:

70us(120Hz) = 0.8% duty cycle (1% - 2 % of DC power is goal for system)
130us(120Hz) = 1.6% duty cycle

4 control signals @ 120 Hz using LVDS logic, 8 IC pads needed

| SIGNAL | Begin time | End Time | PURPOSE |
|---|---|---|---|
| I2 | -70 μs<br>(70 μs Before Crossing) | + 60 μs<br>(60 μs after crossing) | ~130 μs Power cycle for Amplifier-Comparator stage |
| PwrOff | 61 μs<br>(1 μs after I2 off) | -71 μs<br>(1 μs after I2 on) | Drives switches for off state bias |
| ShapSam | 53 μs | 59 μs | 6 μs sample of input bias voltage at end of I2 cycle |
| PullStr | -121 μs | -71 μs | Pulls up both preamp and shaper stage outputs before I2 at end of PwrOff cycle |

For prototyping, relative to I2, the three other Turn-on Signals will need to be iteratively adjusted for best turn-on time. Picoprobing should be part of prototype time optimization.

## PADS

| | |
|---|---|
| Input: | 16 PADS |
| 2 comparators LVDS, 4pads/channel: | |
| Channel data: | 64 PADS |
| 4 control signals LVDS: | 8 PADS |
| BIAS: I2, Ishaper: | 2 PADS |
| Power: AGND, AVDD, AVDD2, QVDD: | 4 PADS |
| Threshold: VREF, VTHH, VTHL: | 3 PADS |
| Output Power: VOUT, GNDOUT: | 2 PADS |
| Calibration: | 4 PADS |

Front edge: 16 inputs
Sides: 11 +12 service pads on two side edges
Rear: 64 Data pads on rear edge

Gav's additional note
Some of the pin names above have changed, and one signal has been added: rampgate.