A 128-Channel Digital Pipeline Chip for Silicon Strip Detector Read-Out

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Abstract

A digital VLSI device for silicon-strip detector read-out has been developed which supports 128 channels as well as providing amplifier calibration signals. This device provides buffering for 256 machine cycles of the hit-pattern of the strips as sensed by multi-channel amplifier/discriminator chips. A second-level buffer is provided. Testability, and alignment features are also provided. The device has been manufactured in a radiation hardened CMOS process. The power demand is 0.21 mW per channel at normal operating conditions. Maximum operating frequency is above 60 MHz. Layout takes into consideration detector geometry, so that mosaic placement of chips can be used to provide electronics pitch no larger than detector strip pitch, down to 45 microns. Serial control and read-out is implemented, to allow optical fiber communication with the controller. Use of dual-ported RAM for the pipeline implementation provides zero-dead-time acquisition. Signal levels to and from the chip are minimized for low noise operation.

I. General

A digital read-out chip has been manufactured for use in silicon-strip detector experiments. The architecture implements a clock-driven pipeline (CDP128) in a CMOS VLSI chip, similar to the earlier CDP64 being used in NA50[2], and DTSC being used in ZEUS LPS[1]. It is meant to be used with an amplifier/discriminator analog VLSI chip which provides a hit/no-hit signal for each strip every machine cycle. The hit-pattern is provided in parallel to the CDP chip via chip-to-chip bonds at the strip pitch. The silicon detector, and many amplifier/CDP128 pairs reside on a hybrid near interaction-region, with the DAQ bus leading to a controller away from the beam-line(figure 2). The CDP128 provides the following primary functions:

- Storage of Hit Pattern for Trigger Latency Period
- Second-level buffering of Level-1 tagged events
- Serial DAQ Bus Interface
- Channel Activity Histogram for Alignment
- Device and System Testability
- Calibration Pulse Generation for Amplifier
- 1-Supression for Edge Detection

The read-out chip functions logically as a storage pipeline(figure 1). The hit pattern from the amp chip is sampled every clock cycle, and passes through the pipeline at the clock rate. After the trigger latency period, a record of the hit-pattern emerges from the far end of the pipeline, and is loaded into the level-2 buffer if a trigger occurs. When detector read-out is initiated, the contents of the level-2 buffer are loaded into a result register which is then shifted onto the DAQ bus in a coordinated manner.

Several additional functions have been added to the basic pipeline architecture. The accumulator register marks any channel that has become active since the last cycle that the device was reset. This is useful for detector alignment using columnated X-rays. A data-path bypass is implemented which allows the pipeline to be filled through the DAQ bus rather than from the amplifier chip, for testing the bus and the chip. A circuit on the input of the pipeline can be programmed to filter all but the first one or two clocks of an active channel. This is used for 1-supression and time-walk correction. Additionally, the chip provides a 'timestamp' of the pipeline stage being read-out, which is useful as a debugging utility for system timing.

The pipeline depth is 256, and the width is 128 bits. At 60 MHz, this provides a storage time of 4 μsec. The level-2 buffer can store up to 9 events. The physical architecture makes use of a RAM block and an address register. The address register points to the 128-bit word in the RAM block that can be written and read during a given clock cycle. During data taking, the chip is instructed to write into the RAM and increment the address pointer every clock. When the address register reaches a count of 256, it automaticly resets itself on the following clock cycle. When the trigger arrives, the hit-pattern from the appropriate time-bin is moved into the level-2 buffer and eventually read out through the bus interface.

Local generation of calibration pulses for the amplifier chip can be produced in response to a control command, along with a two-bit calibration code for the amplifier. The calibration code selects one of four possible calibration patterns for the amplifier chip. When the CDP128 receives a calibration command, it raises the differential calibration signal and lowers it after 128 clock cycles. This is useful because the edge-shape of the calibration pulse affects the behavior of the amplifier, and calibration signals would be badly distorted by the 20-meter DAQ bus from the counting house.

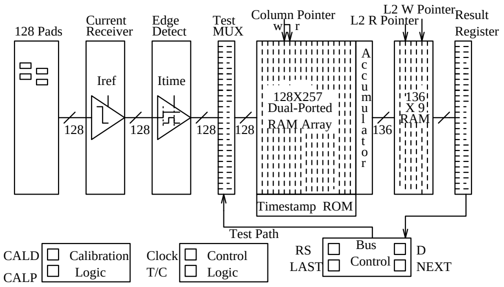

Fig 1. Block Diagram of CDP128

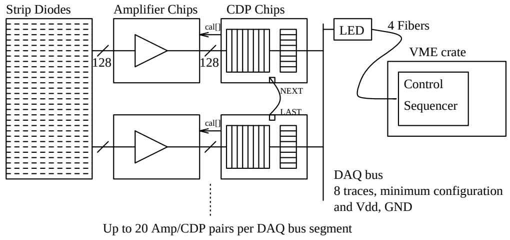

Fig 2. Block Diagram of Detector System

Control and read-out of the chip occurs serially, so that the DAQ bus can be implemented with optical fiber. The system requires four fibers to operate a large number of CDP128 chips, and future revisions will reduce this to three. The CDP chip has 150 signal pads, grouped into various busses. These are itemized as follows:

- i[127:0] The 128 bit input data word
- $\phi[\pm]$ The differential clock signal
- T/C[±] Combined level 1 trigger and control signal(differential)
- RS[±] Read-out Strobe control signal(differential)
- D[±] Data output signal(differential)
- Iref,Itime Reference currents for receiver threshold and acceptance window
- LAST, NEXT Read-out Flag passing signals daisy-chained from chip to chip
- CALD1, CALD0 Calibration pattern code to the amplifier chip
- CALP[±] Differential calibration pulse to the amplifier chip
- TEN Test-mode Enable (single-CMOS levels)
- TP[3:0] Test-path Data nibble (single-ended CMOS levels)
- EEN Edge-mode Enable (single-ended CMOS levels)

The CDP128 receives a combined Level1-trigger and Control signal. If the level1 trigger remains true for more than three clock cycles, the next series of signals on this line are interpreted as a command word. The command word triggers special actions within the chip, such as reset and the calibration pusle. Values on the 128 input pads are sampled every clock cycle, and the command word determines how this data will be dealt with.

The test-mode signal causes the chip to substitute the input data word with the value in the input test register. The contents of this register are set by the controller through the DAQ bus. This allows the chip to be operated without a companion amplifier chip, for either system testing or production testing. When TEN=1, the chip behaves as if i[3:0]=TP[3:0], i[7:4]=not(TP[3:0]), ..., i[123:120]=TP[3:0], i[127:124]=not(TP[3:0]).

Data-taking mode causes the pipeline to be filled with an unfiltered version of the hit-pattern from the amplifier. The edge-mode signal EEN causes the chip to filter the input word through 128 parallel timer circuits. The period of the timer circuits is determined by the Itime reference current. If a channel is inactive, a zero is recorded in the RAM pipeline. If a channel is active and has been active for less than the timer period (acceptance window), a hit is recoded in the pipeline. If the channel remains active longer than this period, no more hits are recorded until that channel has deactivated and reactivated. The Itime pad self-biases to a current corresponding to the nominal 20 ns acceptance window. If a different period is needed, an off-chip Itime current can be supplied through the bond-pad. (bugnote: Polarity of EEN is reversed. EEN=0 causes edge-mode)

The bus interface is a token-passing data-push style with a differential output bit-pair **D** [±]. It is synchronous, and runs at the same clock rate as the pipeline. The signals involved are the LAST and NEXT token passing signals, differential Read-Strobe **RS** [±] signal, and the Data signal (**D**). When the chips receive a read-strobe pulse, they load their result registers from the level-2 buffer. A chip can then unload its result register through its data port when it gets a read-out flag. Chips on a single hybrid have a daisy-chained read-out flag, which enters a chip through a LAST pad on the lower side of the chip and exits through a NEXT pad on the upper edge, which is bonded to the LAST pad of the previous chip. When the controller sends a reset command, all chips assert false on their NEXT pads. The LAST pad on the first chip in the chain can be wired high or provided from the controller. If LAST=true and a chip has not yet read out, it shifts its result register out its **D** pad to the fiber LED driver. Once a chip is finished shifting out its data, it tristates the **D** signal and raises its NEXT signal. The next chip in the chain will then hear LAST=true, and assert its data onto the **D** signal.

The output drivers of the chip have an output impedance of about 500 Ω. This is intended to accommodate 50 Ω terminated cable with 0.4 volt signal levels, for low-noise and high bandwidth at moderate power. When not addressed, the output drivers are in high-impedance state.

All run-time control and bus signals are differential. Reduced voltage logic levels with as little as 0.125 volt swing can be used to minimize system noise. Testing and configuration signals (TEN, EEN, TP[3:0]) are single-ended CMOS signals in this implementation. LAST and NEXT are also single-ended CMOS, because they are chip-to-chip wires and have slew-rate limiting drivers.

The CDP128 receives the 128-bit data word from the amplifier chip by means of current-mode signals(figure 3). The arrangement can provide up to 100 Mbit/second bandwidth through each chip-to-chip bonding wire. A current signal is received from the amp chip into a moderately low input impedance receiver (approximately 500Ω). Current flows from the CDP supply voltage through a transistor in the amplifier chip, and back to the CDP through a ground-return. The levels are Iil $\leq$10 μA, and Iih $\geq$ 50 μA. Iref sets the threshold between the input logic levels, and self-biases to the nominal 20 μA. If a different threshold is desired, an external Iref current can be supplied through the bond-pad. The voltage on the input signal pads sits at about one Pfet threshold below Vdd, or about 2.9-3.3 volts for nominal Vdd = 4 volts. The voltage swing is about 0.2 volts.

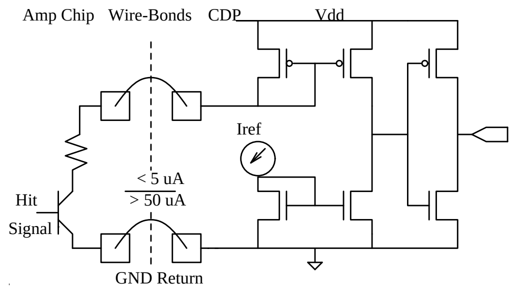

Fig 3. Amp/CDP Communication Scheme

Due to the use of dual-ported RAM to implement the pipeline, the chip has no dead time. In this architecture, there is no occupancy-dependent loss of efficiency as might be the case for a CAM-based pipeline. Low-noise bus architecture allows data acquisition to occur during data-taking. Digital noise coupling into the front-end amplifiers seems to be less than 5% of the typical amplifier input signal.

The architecture requires about 400K transistors. The drawn die size is (6.0 X 5.25) mm^2, and the physical size is (6.2 X 5.45) mm^2 X 400 microns. The device has been manufactured in Honeywell's RICMOS-IV radiation-hardened 0.8 micron 3-metal single-poly n-well CMOS process. Radiation tolerance of the CDP128 to gamma, proton, and neutron exposure has been measured and found satisfactory. The design can also be manufactured through MOSIS, using HP's 0.8 micron 3-metal process.

II. Operation and Programming

When an output cycle is initiated (LAST=true, RS pulse has been received), the chip drives out its result register by putting a new bit on the bus every clock cycle. The result register is 136 bits wide (128 bit hit-pattern and 8 column-code bits), so a read-out cycle takes 136 clocks plus an initial token-passing clock cycle. The first 8 read-out cycles contain the column-code CC[7:0]. The read-out cycle is sequenced as follows, with entry per clock:

-1: Read-out Condition Occurs: (has been an RS and LAST rises) or (LAST=true and RS pulses) **D** goes from high-Z to output enabled
0: CC4
1: CC5
2: CC6
3: CC7
4: CC0
5: CC1
6: CC2
7: CC3
8: i0
9: i1
...
134: i126
135: i127
136: **D** goes high output impedance

The CDP128 responds to a small number of control commands. These are encoded as unique sequences of pulses on the T/C signal. If the T/C signal is sampled true for between one and three clocks, it is interpreted as a level-1 trigger. If T/C is sampled true for four consecutive clock cycles, the value of T/C over the next four clock cycles is decoded as a command and trigger activity is suppressed in the chip. Sending a command to the chip therefore requires 8 clock cycles. The command sequences are as follows:

T/C= 1 1 1 1 0 0 0 0 - Reset: initialize address pointers, clear accumulator register, set NEXT to false
T/C= 1 1 1 1 0 1 b0 b1 - Load Calibration Register: set CALD0 to the state of b0 and CALD1 to the state of b1
T/C= 1 1 1 1 1 0 0 0 - Trigger Calibration Pulse: CALSP=true and CALSN=FALSE for 128 cycles
T/C= 1 1 1 1 1 1 1 0 - Read Accumulator: Value of accumulator register is written into level-2 buffer

An example short program to read column zero of the pipeline is written below. The configuration is TEN=true, EEN=true(disable edge mode) LAST=true, TD[3:0]=5.

——— reset — fill pipeline —
T/C: 1 1 1 1 (0 for 257 clocks) 1 0 0 0 0 ...
RS: 0 0 0 0 (0 for 257 clocks) 0 0 0 0 1 0 ...
D$\pm$: z z z z (z for 257 clocks) z z z z z 0 0 0 0 0 0 0 0 1 0 1 0 0 1 0 1 ...

The same program modified to read column one of the pipeline is written below. The configuration is TEN=true, EEN=true(disable edge mode) LAST=true, TD[3:0]=A.

——— reset — fill pipeline —
T/C: 1 1 1 1 (0 for 258 clocks) 1 0 0 0 0 ...
RS: 0 0 0 0 (0 for 258 clocks) 0 0 0 0 1 0 ...
D±: z z z z (z for 258 clocks) z z z z z 0 0 0 0 0 0 0
0 0 1 0 1 1 0 1 0 ...

Note that because the T/C signal must be filtered by 4 clocks to detect a command, its effect as a trigger appears to be delayed by 4 clocks with respect to the data and other control signals. This is why the L1 trigger and RS pulse are separated by four clocks in the following program. Command sequences must be separated by at least one cycle with T/C=false. This means that two consecutive commands require a total of 17 clock cycles to be transmitted.

A short program to write 00 into the calibration-code register and then 11 into this register is given below. Three commands are sent: a reset followed by two register writes.

T/C: 1 1 1 1 0 0 0 0 0 1 1 1 1 0 1 0 0 0 0 0 0 0 1 1 1 1
0 1 1 1 0 0 0 0

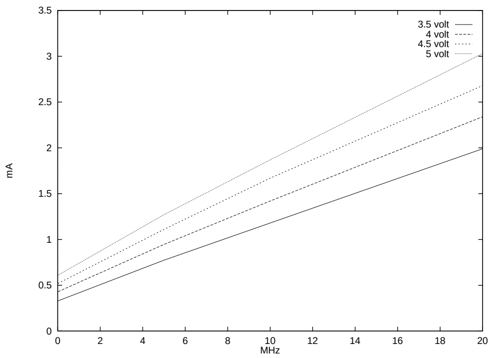

Fig 4. Current vs. Frequency

Note that since the pipeline RAM is actually 257 columns long, the column-code for the last column in the RAM is 01010101. The column-code for the accumulator register is 10101010. These two column-codes are not unique, corresponding to two locations in the pipeline.

In this architecture, the operating current is influenced primarily by the length of the pipeline, the supply voltage, and the operating frequency. Figure 4 shows the chip's current draw vs. frequency at various supply voltages. At the nominal conditions of 4V supply and 40 MHz, the chip will require 160 μW per channel for zero occupancy and trigger rate. Each active channel will require an additional 50 μA. The output bus requires 8 mA when active. In a typical operating situation, with 0.1% occupancy and and a chip reading out at an 10% duty-cycle, the the per-channel power will be 210 μW. If the chip were built with a 128-stage pipeline for an experiment with shorter trigger latency, the power could be expected to decrease to 150 μW per channel.

Although the CDP128 is capable of operating in a stand-alone configuration, a hybrid-side supervisor chip has been manufactured to extend its performance. The HAC (Header-Adder Chip) provides electrical buffering between the CDP's and cable, detects and recovers from error conditions, and provides additional flexibility of trigger generation and cable configurations. HAC/CDP hybrids have been reliably operated at 40 MHz at the end of a 20 meter cable with no cable-drivers on the hybrid.

A combined amplifier/CDP chip has been produced through MOSIS using the SVX CMOS amplifier developed at LBL. This chip has been found to be functional, and measurements indicate that digital noise does not have a large impact on the overall noise-floor of the system. A mixed-mode device such as this allows further reduction in power, materials, and physical complexity of embedded electronics for silicon vertex detectors.

References

[1] **The Time Slice System**, Joel DeWitt, Nuclear Instruments and Methods in Physics Research A288 (1990) 209-211

[2] **A Pipeline and Bus Interface Chip for Silicon Strip Detector Read-Out**, Joel DeWitt Proc. of IEEE 1993 Nuclear Science Symposium, San Francisco, CA, Nov. 1993.