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A Fast Shaping Low Power Amplifier-Comparator Integrated Circuit For Silicon Strip Detectors*

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Abstract

We have designed and tested a 64 channel amplifier-comparator integrated circuit on the Maxim SHPi bipolar process. The low power design, 840 µW/channel, is intended for use as a frontend with high clock rate silicon strip detector systems. Peaking time at the comparator input is 20 ns, for good double pulse resolution, and noise is near optimum for the technology used. We have used the chip successfully in a proton beam test at KEK in Japan with a 40 MHz data clock.

I. INTRODUCTION

Silicon strip detectors used as vertex detectors in high rate colliders are well suited for integration with multichannel integrated circuit amplifiers[1]. Inclusion on the IC channel of a single precision comparator with a digital output provides a low power and low cost front-end analog system, yet provides capability to measure system characteristics such as noise, crosstalk and efficiency. We developed the LBIC IC as a prototype amplifier-comparator for the SSC silicon tracker, so it has direct applicability for binary readout of the trackers proposed at LHC. In this paper, we will review the general specifications of the frontend system, then describe the circuit details, and discuss chip test results, which will include effects of proton irradiation on the LBIC.

II. SPECIFICATION

Amplifier peaking time: The channel digital output needs to be assigned to the correct collider bunch crossing, which occurred every 16 ns in the SSC. Silicon strip signals in 300 µm thick detectors can take up to 25 ns to collect. For good signal/noise, shaping time should be longer than collection time. A comparator with fixed threshold will fire earlier on a larger amplitude signal for a given signal shape. Comparator firing time variance on the range of signal amplitudes, called time walk, should ideally be at least 5 ns less than the bunch crossing rate in order to allow easy assignment to a unique time bucket. Time walk for a signal shape is mostly dependent on the signal peaking time. In our design, the comparator itself contributes less than 1 ns of time walk on all amplitudes of signals. We want to keep double pulse resolution to 60 ns or less, which in practice implies a peaking time of at most 20 ns. Balancing these considerations, we selected a 20 ns peaking time. For the SSC this might have necessitated time walk correction circuitry, which the LBIC design does not include. For the LHC, which has beam crossings of 25 ns, a time walk requirement of 20 ns is a good match for the LBIC shaping.

Chip power use: At a hadron collider the silicon tracker is deep inside a massive 4π detector. Heat from circuit power use must be removed, and material used in transporting the heat out of the detector increases the interaction probability for particles. Power use for this chip was specified to be below 1mW/channel, with any further reduction being useful.

Noise: Silicon strip signals in 300 µm detectors are small: the most probable amplitude is about 4 fC. Setting the discriminator threshold at 1 fC has been shown in beam tests to give good efficiency. To keep the noise false hits at a low rate, we need to set the threshold at the 4 sigma level of the strip channel noise. In addition to simple bipolar amplifier noise, there is series noise from the detector strip resistance, shot noise from irradiated detector leakage current, and noise from adjacent strips. Neighboring strips are important since strip capacitive load is mostly with its neighbors. Since the shaping time is similar to the signal itself, there is also some ballistic deficit, typically about 10 %. A 12 cm long n-type detector strip presents an 18 pF capacitive load, and typically has a noise of σ = 1600 e- at 20 ns shaping, when we consider all noise sources. Ballistic deficit raises this to an equivalent 1800 e-. Four times this noise implies a threshold of 1.15 fC of n-type signal. We must optimize amplifier noise contributions, as well as the other noise sources, to keep the particle detection efficiency high.

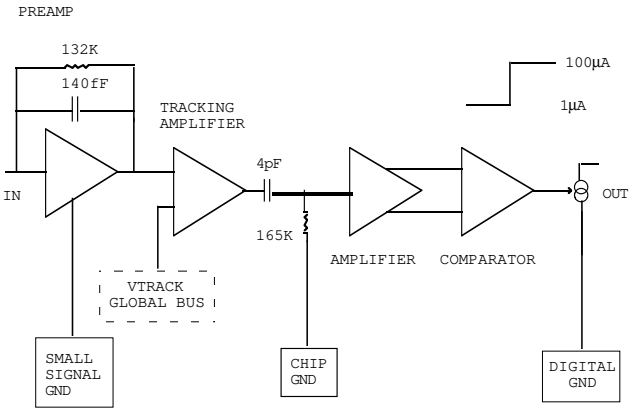

Figure 1. LBIC functional block diagram.

Precision: All the channels on a chip get a common threshold at their comparator inputs, so the false hit rate will be dominated by the amplifier with the highest gain. An acceptable increase in false hit rate is found with an equivalent channel variation of one-third the noise, or equivalent threshold sigma of 0.08 fC of input signal.

System pickup: Sporadic digital pickup increases the apparent frontend noise, so it must be avoided. Synchronous digital clock pickup can cause offsets between channels, which reduces matching precision and introduces clock phase dependence of the effective threshold. The frontend system needs all the isolation from the digital readout that we can provide.

Radiation Resistance: SSC and LHC specified good performance for a fluence of at least 2 x 10^{14} protons/cm^2. Channels in a given module using a common threshold are assumed to receive the same fluence. The main radiation effect is a decline in npn DC beta, initially about 100, to about 40, so the design must compensate for this change.

Cost and mass: Chip area needs to be minimized. The silicon chip mass is a substantial contributor to the material in the detector volume. Precision needs to be attained without adding the expense of laser trimming or special selection procedures. Minimizing chip area will minimize cost if yields can be kept high.

III. DESIGN

We chose Maxim's SHPi process, which has 8 GHz f_t npn's with a minimum emitter size of 1.3 x 3.6 µm[2]. The very low npn collector capacitance enabled us to set quiescent biases as low as 2.7 µA with correct design bandwidth, and the very small emitter volume demonstrates sufficient radiation resistance. Typical npn beta is 100, with 3 σ V_{be} matching of 1 mV for adjacent npn's. Adjacent 3 σ resistor matching is 1 % and process resistor variation is +/- 22 %. SHPi allows very low currents, has sufficient precision, and possesses workable radiation resistance.

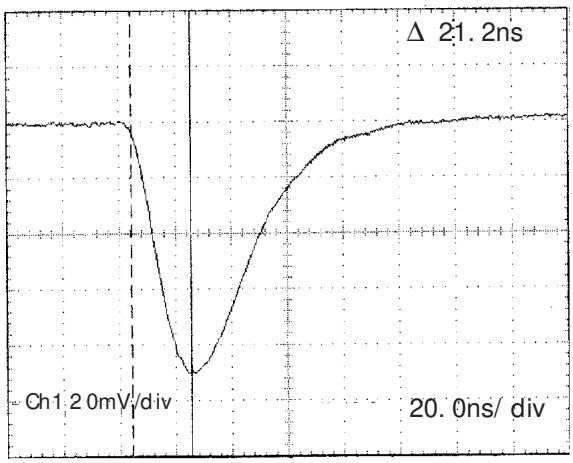

Figure 2. One of two signals at the differential comparator input.

Figure 1 shows the five LBIC circuit stages of preamp, tracking amplifier, AC coupling, amplifier, and comparator with open collector output. The tracking amplifier boosts the dynamic signal before the AC coupling ,so that we minimize the threshold errors contributed by later stage DC variations. Gain is 180 mV/fC at the comparator input, determined by precision design concern. Analog signal shape, Figure 2, is semigaussian for fast return to the baseline, best for double pulse resolution. Three analog probe points are provided on even numbered channels, PR1 - PR3.

Figure 3 is the channel subcircuit, 64 on each chip. Figure 3 also indicates the global buses. The primary supplies are 3.5 V and ground. Ground is supplied to 3 independent buses for stage isolation. The other chip supplies are the differential threshold, VT1 and VT2, and V7. VFRONT global bus provides current sink bias at 3.3 µA per minimum transistor unit.

In the preamp, J1 is an active current source, whose gate is controlled by a global voltage bus, VJ1. This bus is driven by a simple op-amp circuit that needs a supplementary 7 V supply, V7. J1 current is programmable by an external voltage. 0 V sets J1 at 130 µA, the noise minimum for 14 pF front load with an irradiated chip. Q1 input transistor is 8 times the minimum transistor size as a noise trade-off between declining irradiation beta and base resistance of 54 Ω. Cascode Q2 increases preamp open loop gain which lowers the front input impedance, and decreases strip crosstalk. Capacitor feedback, C4 and C1, is split, which increases the gain of diff amp Q8-Q11 by lowering the dynamic emitter impedance of Q8. This saves power. Additionally, split feedback narrows the preamp bandpass, giving a semigaussian rather than RC-CR signal shape.

Under irradiation, the emitter of Q3 shifts 300 mV as Q1 base current goes from 1 to 3 µA, since this current is supplied through feedback R1. The tracking amp stage, Q8 - Q11 has a global voltage bus, VTRACK, that tracks the preamp output and biases Q9 as a voltage source. A heavily decompensated preamp circuit, Figure 4, drives the VTRACK bus. Note that the circuit depends on cross chip component matching since more than 5 mV mismatch in VTRACK brings a noticeable gain change in the diff amp. The collector of Q9 is a signal integration point.

We make the AC coupling time constant as large as chip space allows. After this coupling, circuitry is full differential for DC precision. VDIFF global voltage, 2.2 V, provides DC input bias. The next diff amp has the differential thresholds, VT1 and VT2, applied to its collector voltages, where the full differential signal is integrated for the third time. The full differential threshold allows the threshold to be applied across many channels and chips with good common mode rejection. The differential dynamic signal is applied to the comparator stage, Q31 - Q42.

The core of the comparator is a differential pair amplifier with positive feedback through capacitor C3. Q35 is biased at 24 µA. All this current flows through collector resistor R30 in the quiescent condition. In the triggered state, the tail current switches into diode Q38, then is mirrored into a 100 µA current into the collector of Q41. The comparator current output is shown in Figure 5.

The emitter of Q41 is referenced to digital ground of the receiving CMOS chip, so the output signal is referenced to digital ground. Some isolation between analog and digital ground is provided by passing the comparaator signal through the high impedance of the collector of Q39.

The comparator transfer function with one input driven directly is shown in Figure 6. For a perfect comparator, we expect a 1:1 ratio between the input signal and the trigger threshold of the comparator. Figure 6 indicates this perfect transfer function. In this comparator, most of the voltage gain comes from the positive AC feedback, which is input amplitude and frequency dependent. As a consequence, the actual transfer function in Figure 6 has a slope of 0.92 instead of 1. This deviation from ratio 1 is interpreted as an offset in Figure 6. Simply described, the comparator transfer function is moderately nonlinear, has a gain of about 0.9, with a DC offset of about 30 mV. The minimum threshold for full switching output is 50 mV.

Comparator input signals 5 mV above the threshold give sufficient digital pulse width, wider than 25 ns. Global bus VPRE and Q42 keep the output at 1 µA for the off state.

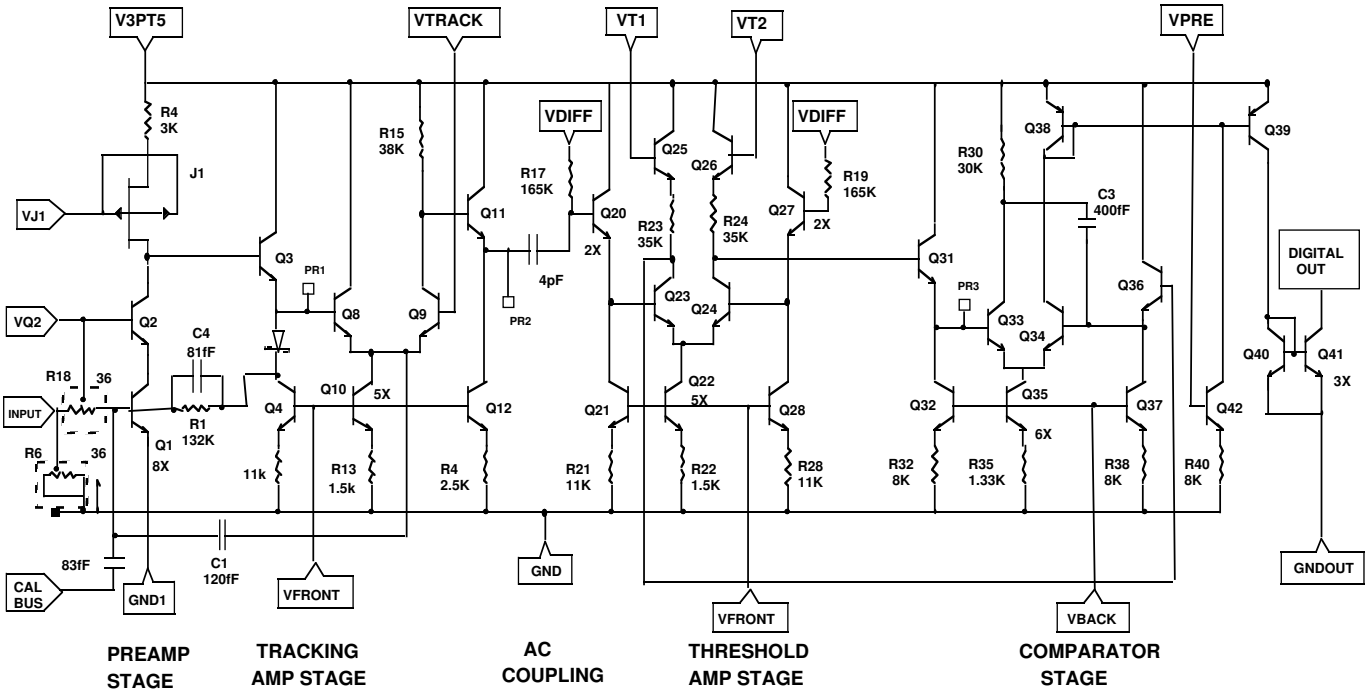

Figure 3. LBIC channel schematic, 1 of 64.

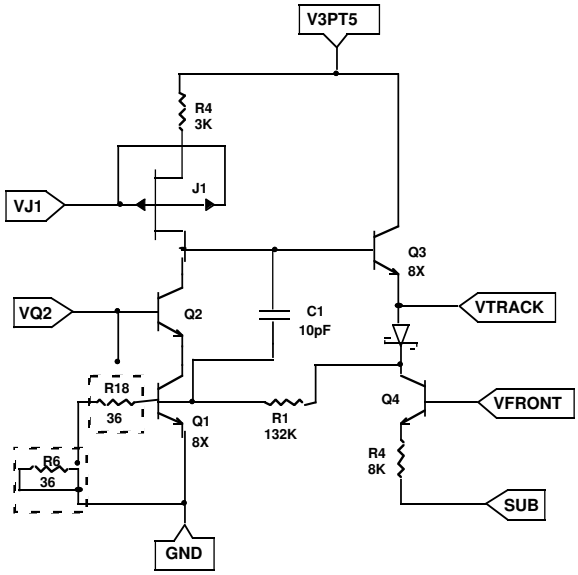

Figure 4. VTRACK global bus generator.

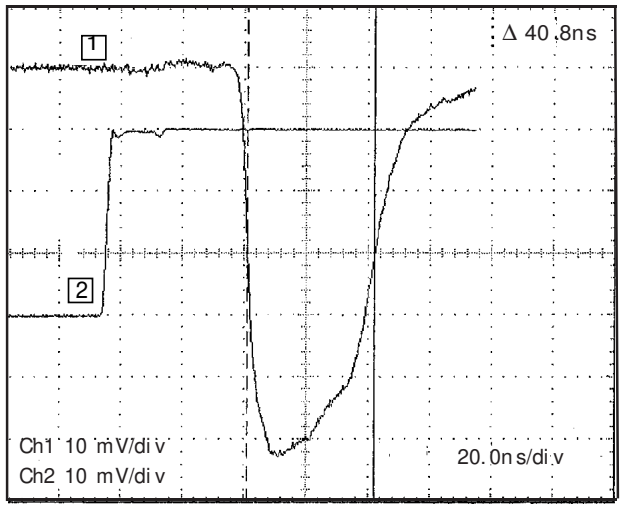

Figure 5. Digital output current signal into 600 Ω.

Layout of the LBIC channels is on a 40 µm pitch, so that the chip matches a 50 µm pitch strip detector. V3.5 has a 72 pF bypass cap. All the global voltage buses and supplies have a bypass capacitor of typically 7 pF to chip ground, except VTRACK. On the input of each channel is an 84 fF MIM calibration capacitor, the other end of which is tied to one of four calibration buses in alternating fashion.

IV. MEASUREMENTS

We measure the LBIC performance using a 64 channel input CMOS digital chip, the CDP, that we have fabricated in several versions: 1.2 µm MOSIS, .8 µm MOSIS, and .8 µm Honeywell rad-hard[3]. The CMOS chip provides the digital reference ground, GNDOUT in Figure 3. The digital/analog isolation zone takes place on the LBIC itself between the high impedance collector of Q39, which is referenced to V3.5, and diode connected Q40, referenced to digital ground. The CDP receives the open collector LBIC signal with a diode connected PMOS transistor with an input impedance of 4 kΩ. This current is then compared with a programmable threshold, typically 40 % of full signal. We prototyped this LBIC only for p-strip signals, although it works with n-strips with a reversal of output levels. The n-strip output time widths are also narrower.

We constructed four assemblies each consisting of a Hamamatsu double-sided detector mounted on a pc board. 128 channels on each detector face were bonded to a total of 16 LBIC chips. We then developed a complete calibration and readout system at 40 MHz clock rate and tested this system in a beam test in June, 1994 at KEK. All measurements are done using this system. For channels bonded to a detector, digital clock pickup at 40 MHz is small. For channels that are unloaded, clock pickup can skew gain measurements, and we have to take some care.

We define the amplifier-comparator response to an input charge as the threshold setting in mV which shows a 50% count rate. This response measurement includes the amplifier nonlinearity, comparator nonlinearity, and the apparent comparator DC offset. Figure 7 illustrates our method of determining this response for a 1 fC preamp input signal. The comparator count fraction is plotted versus threshold for a fixed input charge. The input noise spectrum is white in character, so the fit of a gaussian error function to the Figure 7 points is good. The fit parameters provide a noise sigma and a 50% point.

FIgure 8 shows the 50% count point of the amplifier-comparator versus input charge. This response curve shows some nonlinearity and an apparent DC offset. A four term polynomial or cubic fits this curve well. The constant term is taken as the DC offset, and the remaining three

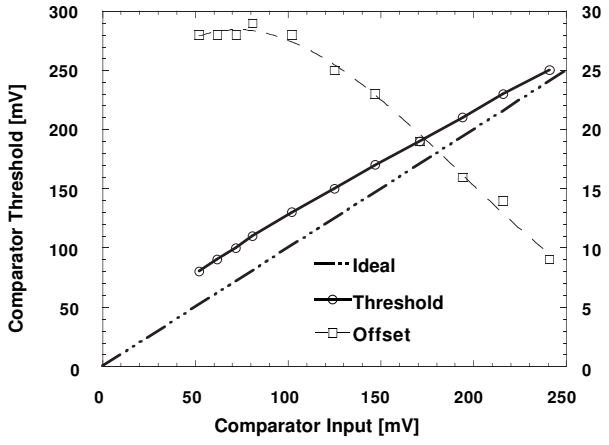

Figure 6. Comparator transfer function and offset versus single-ended signal injected into comparator by probe.

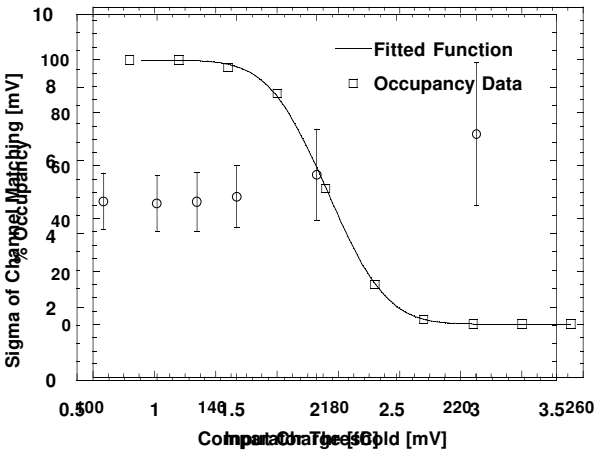

Figure 7. Channel to channel matching in mV for 3 thresholds as a function of input charge

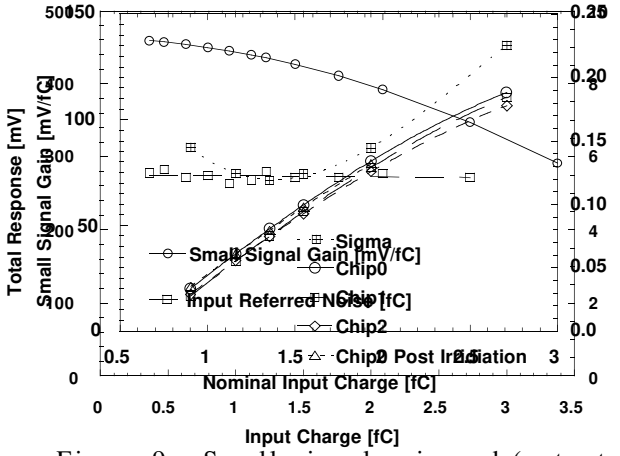

Figure 9. Small signal gain and (output noise)/(small signal gain) versus input charge.

describe the amplifier-comparator gain. The output noise sigma plotted in Figure 8 uses the method of Figure 7.

By taking the derivative of the response curve, we find the small signal gain of the amplifier-comparator. A small signal, such as a typical noise impulse, rides on top of a much larger calibration input signal. For a simple linear system, the small signal gain and large signal gain are the same. Figure 9 plots the small signal gain versus preamp input charge for this nonlinear amplifier-comparator. In Figure 8, output noise decreases with increasing signal. Figure 9 shows that this noise referred to the input by dividing by small signal gain is actually a constant 0.12 fC. The actual noise figure is 16 % lower (632 e-) because of the VTRACK correction discussed below.

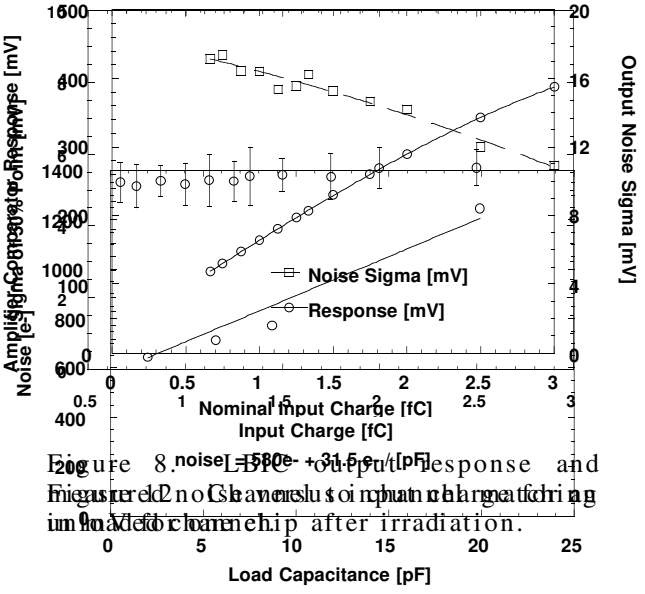

Figure 8. LBIC output response and measured noise versus input charge for one channel.

Figure 10. Noise versus capacitive load.

Figure 10 shows noise versus capacitive load, which is a chip capacitor bonded to the input and the printed circuit board ground. Noise, at a 120 μA front transistor bias, is 580 e- + (32 e-)/(pF), which is very close to simulations. The 9 pF data point shows lower noise than expected because the load capacitor, its inductive bonds, and the channel input form a resonant LCR circuit. The signal peaks more, which improves signal/noise. Detector strip loads do not show this resonant effect.

We compare channel to channel matching of input response within a chip for 3 chips. Figure 11 shows a sigma of 5 mV at 1 fC input, or 3 % variance of 1 fC gain. This includes calibration capacitor variation, channel gain variation, comparator offset differences, and any difference in digital pickup across the chip. From this measurement, we conclude that the global voltage sourcing technique works well.

Four LBIC and CDP chip sets were irradiated with 5 x 10^{13} protons/$(cm)^2$. Figure 12 indicates that the channel matching for 59 channels on one chip remained very good, σ = 5.2 mV. The lateral pnp beta declined to 4.5, which lowered the digital output to 64 μA. Five channels had their comparator function shift in an unexpected way due to erratic pnp deterioration.

Figure 13 indicates average input response for 4 chips: the 3 unirradiated from Figure 10, and the one irradiated from Figure 11. No significant change in response is seen for the irradiated chip. Matching chip to chip for this wafer is good enough to allow common thresholds without having to move thresholds higher in order to reduce noise hits.

The VTRACK bus had insufficient on-chip bypassing, and we found 1% channel to channel negative crosstalk on all chip channels. This is not a problem in actual use where simultaneous hits are rare, but 16 channels fire when calibrating, introducing 16 % low gain at 1 fC. Figure 14 shows the gain correction curve between single channel operation and 16 channel calibration. We placed a bypass capacitor to ground on the VTRACK bus by using steel probes. The two response curves shown are with the bypass on and off the bus.

V. CONCLUSION

The LBIC design meets the typical specifications needed for the LHC. The design meets specifications for the late SSC, except possibly for time walk. With very low power of .84 mW/channel, we have demonstrated precision amplifier/comparator functioning and matching. Noise is near optimum. Radiation resistance of the design is evident to $5 \times 10^{13}/cm^2$ proton fluence. Lateral pnp's are not reliable at the fluences needed, but acceptable vertical pnp's are now available from Maxim. Digital pickup at 40 MHz has been shown to be negligible for channels with a detector load.

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VI. REFERENCES

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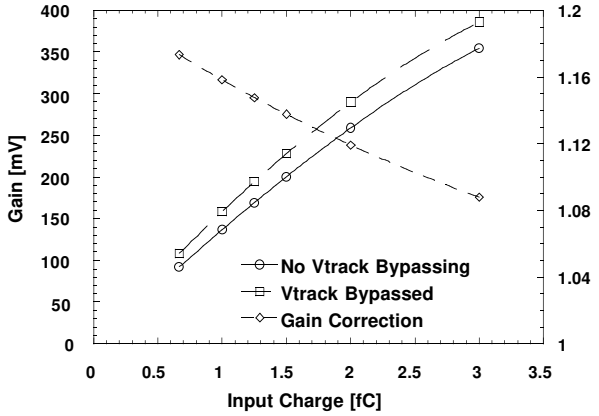

Figure 14. Response for VTRACK bypassed and not bypassed, and gain correction ratio.