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Design, Testing and Performance of the Frontend Electronics for the LPS Silicon Microstrip Detectors

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Abstract

We present our experience in design, construction, testing and operation of the frontend electronics (FEE) for the LPS silicon strip detectors for HERA. A total of about 22,000 channels has been operated as close as the 10σ envelope of the 820 GeV proton beam. This FEE system is binary, controlled by one threshold set at about 0.8fC, and has been optimized by combining a fast low-noise bipolar amplifier/comparator VLSI with a low-power digital pipeline manufactured in radiation-hard CMOS.

1. INTRODUCTION

Silicon microstrip detectors are used extensively in HEP experimentation. The small feature sizes and the large number of channels are ideally suited to integration with VLSI electronics and on-detector data reduction. The frontend electronics has to adapt to the specific requirements of the experimental situation, which are different for fixed target, collider and space applications, respectively. We report here on the frontend electronics for the Leading Proton Spectrometer (LPS), operating in conjunction with the ZEUS detector at HERA. This device, described in detail in Refs. [1-3], detects and momentum analyses diffractively scattered protons in e-p collision with planes of silicon microstrip detectors positioned in close proximity to the circulating proton beam. The detectors are moved within the 10σ envelope of the proton beam with the help of “Roman Pots”, (the closest distance to the beam center is 2mm) and retracted during injection and unstable beam conditions. In comparison with previous applications, the 10MHz collision frequency of HERA and the high radiation levels were new challenges. In addition, we chose to build a conceptionally simple system which recorded only the addresses of strips whose pulse height exceeded a set threshold, but not the pulse height itself, which put stringent requirements on the noise immunity and uniformity of the frontend electronics.

In the following, we first describe the design of the FEE VLSI chips. We then report the results of extensive testing of the FEE chips, including channel-to-channel matching of gain and noise. Next is a brief account of the assembly of FEE-detector modules and their testing using a laser test station. We then report on the performance of the frontend electronics during data taking at HERA. Finally, we present results on radiation hardness, both in tests of the FEE and in our experience in the HERA beams.

2. DESIGN OF THE FRONTEND ELECTRONICS VLSI

The design and the choice of technology for the LPS electronics at HERA was based on a set of specifications, which were derived from the properties of silicon microstrip detectors, the environment at HERA and the read-out and trigger architecture of the ZEUS experiment:

Radiation hardness up to a high energy proton fluence of 10^{14} p/cm^2, corresponding to a similar neutron fluence combined with a total ionizing dose of 3.3Mrad.

30 ns shaping time commensurate with the collection time of the holes of a fully depleted detector. An amplifier shaping time of the same order ensures that the signal peaking time is less than the 96ns between HERA beam crossings, which allows the assignment of the correct bunch crossing to every detector signal. It also reduces deadtime.

Narrow channel width to match the smallest detector pitch of 85µm, while leaving room for bonding between chips.

Low noise to ensure good signal-to-noise ratio. With a signal charge of about 25,000 electron-hole pairs per minimum ionizing particle, a noise charge of about 1000 electrons gives good detection efficiency with low noise rate. The load capacitance varies between 1 and 10 pF, depending on the strip length.

Low power consumption. The remote location of the detectors and integration of the VLSI with the temperature sensitive detectors requires low power consumption of the FEE to minimize temperature increase. An upper limit of 2mW/channel was adopted.

Operation with input currents in excess of 2µA. Anticipated radiation damage to the DC coupled silicon microstrip detectors would result in leakage currents of that order per strip, which the FEE inputs have to absorb without large loss of gain.

Pipelined operation. In order to minimize the bandwidth of the readout, the hierarchical trigger structure of ZEUS is used: the data is stored on-chip until a valid second level trigger arrives after about 1ms. This can be achieved by a synchronous first level buffer of about 6µs followed by an asynchronous second level buffer.

Based on a design study, a mixed technology combination of bipolar amplifier-comparator VLSI (for low noise and speed) and a CMOS digital pipeline (built as an SRAM to save power) was selected (see Fig. 1).

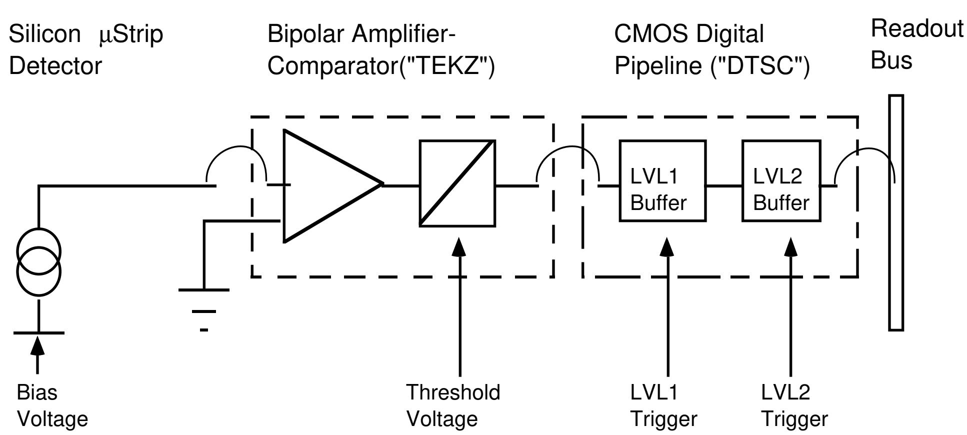

Fig. 1. Block diagram of the FEE system.

Using two chips requires an extra wire bond per channel, but allows optimization of the two chips. The system is binary, i.e,. for every channel a bit is stored in the time slice of the corresponding beam crossing, which is set if the pulse height exceeds a threshold, and is zero otherwise. No other information is kept. The number of channels per chip is 64.

2.1 Bipolar Amplifier-Comparator Chip (TEKZ)

The amplifier-comparator chip was fabricated in the Tektronix SHPi process to a channel width of 72μm. Its design and performance has been described in detail in Ref. [4]. Figure 2 shows the complete circuit diagram for one channel.

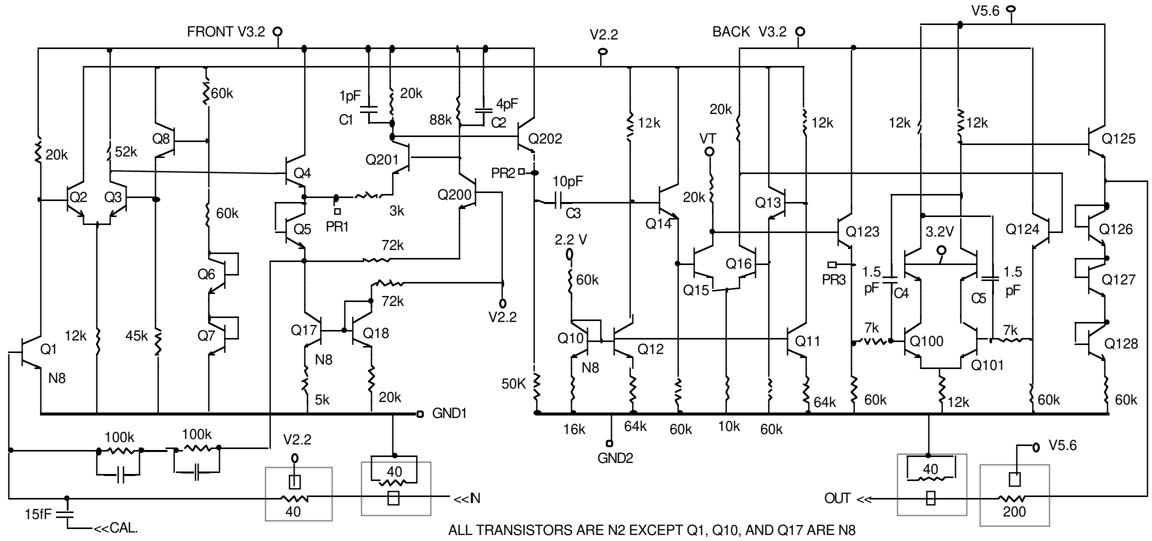

Fig. 2. Circuit diagram for one channel of the bipolar amplifier-comparator chip TEKZ.

We refer to the functional circuit diagram of Fig. 3 to point out the main features of the design. The shaping time is τ_S=32ns, and the overall gain is about 150mV/fC. The comparator is decoupled via a 10pF capacitor, resulting in a high-pass filter above 100kHz. The comparator threshold is set externally and is common to one chip. The comparator requires no reset and has a deadtime of about 150ns after a hit. The outputs are pulses of about 40ns width and 800mV amplitude. The inputs (and outputs) are protected by diode junctions formed between resistor implants and the epi tubs.

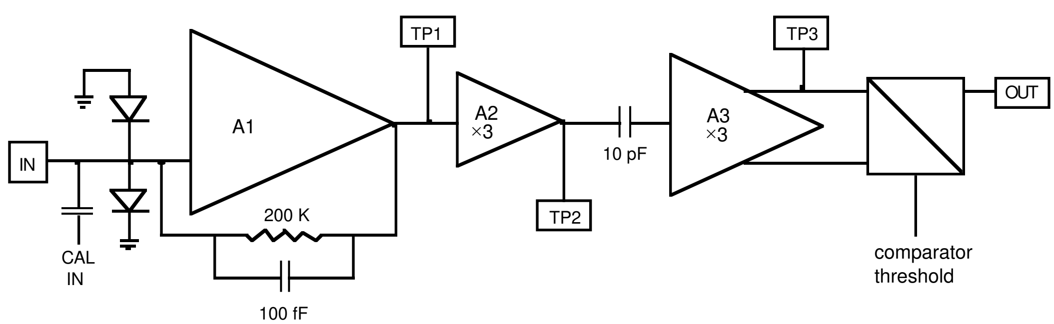

Fig. 3. Functional circuit diagram of the bipolar amplifier-comparator chip TEKZ.

To test functionality and measure gain and noise, test pulses can be injected on four calibration lines, each connected to the calibration capacitors of 16 channels. Several test points allow probing during characterization.

2.2 CMOS Digital Time Slice Chip (DTSC)

The digital output signals from the comparator are stored in the digital buffers until a trigger decision is made. The VLSI chip fulfilling this function is the Digital Time Slice Chip (DTSC), described in detail in Ref. [5]. A block diagram of the DTSC is shown in Fig. 4.

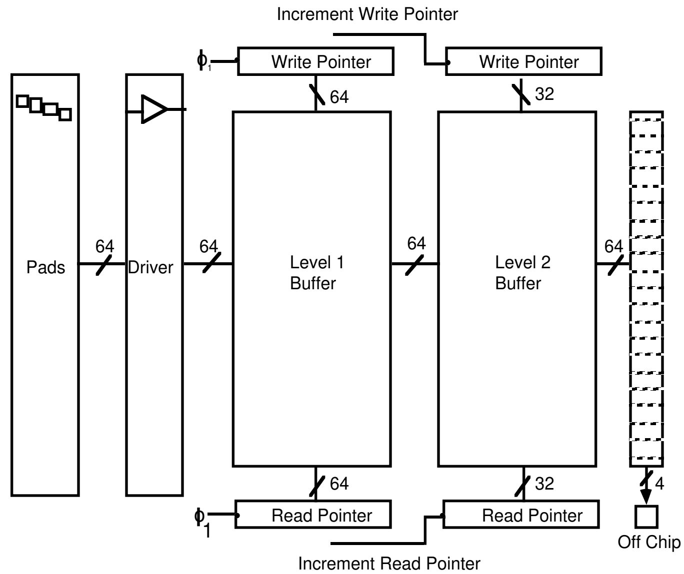

Fig. 4. Block Diagram for the Digital Time Slice Chip DTSC.

An event is clocked as a time slice into the level-1 buffer with 10.4 MHz, the HERA collision frequency. If a valid level-1 trigger occurs after a fixed latency, the time slice is transferred into the level-2 buffer; otherwise, the time slice is overwritten. The level-1 buffer is 64 locations deep, allowing for the ZEUS trigger latency of 6µs, while the level-2 buffer is 32 locations deep to allow for efficient data storage even in case of high level-1 trigger rates. After a valid level-2 trigger, the data is transferred uncompressed serially on four data lines. The DTSC is implemented as a SRAM, i.e., only pointers are moved once the data is strobed into the buffer. Clocks and digital control signals are generated externally and bussed to the chips differentially. The DTSC was manufactured in 1.2µm radiation hard CMOS by United Technologies Microelectronics Center (UTMC) [6]. It contains about 48,000 transistors, and the power consumption is about 2mW per channel at 10MHz.

3. TESTING of the FEE CHIPS

The two chips were tested separately before assembly to minimize rework on the hybrid assemblies. The bipolar chips were tested in the SCIPP laboratories and detailed information about the characteristics and uniformity extracted. The CMOS chips were tested by the foundry, UTMC.

3.1 Testing of the Bipolar Amplifier-Comparator Chip

The bipolar chips were delivered diced and they were tested using a probe card and a test apparatus described in detail in Ref. [7]. We will give below a summary of the method and the results of the testing. The tight spacing of the output pads made a simultaneous testing of all 64 channels impossible, and so we tested only 32 channels at a time. Using the test inputs, the gain and noise of the amplifier chips were determined by injecting through the calibration capacitor pulses of known charge, i.e., 1fC and 2fC, and measuring the synchronous counting rate as a function of threshold, as shown in Fig. 5. The threshold voltage difference of the 50% points is the gain in mV/fC, and the width of the threshold curves gives the noise. Specifically, the threshold voltage difference between the 88% and the 12% occupancy points is equal to the noise FWHM (we actually fit the data with an error function to extract the 50% points and the noise sigma).

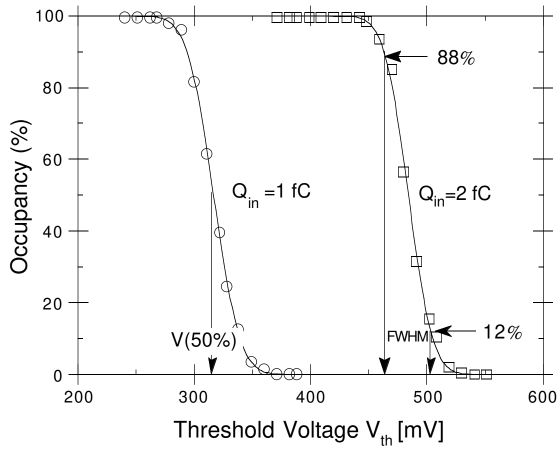

Fig. 5. Extraction of the gain and noise from the occupancy curves with 1fC and 2fC test pulses.

We show in Fig. 6 the distribution of measured gains. The mean is 164 mV/fC, with an RMS of 7mV/fC.

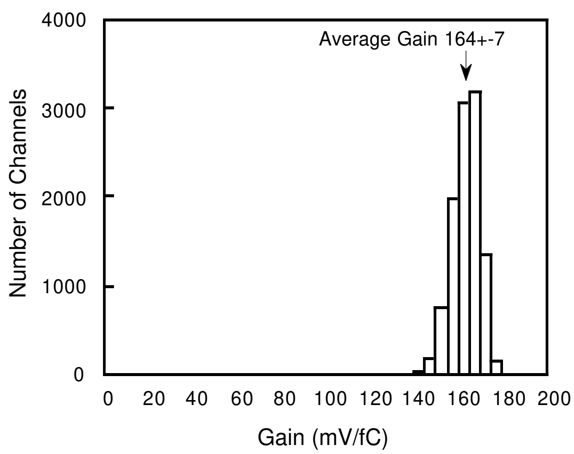

Fig. 6. Distribution of TEKZ gains.

In Fig. 7, we show the corresponding noise sigma's, centered at 17.2mV corresponding to a noise charge of σ_n = 656 e^-.

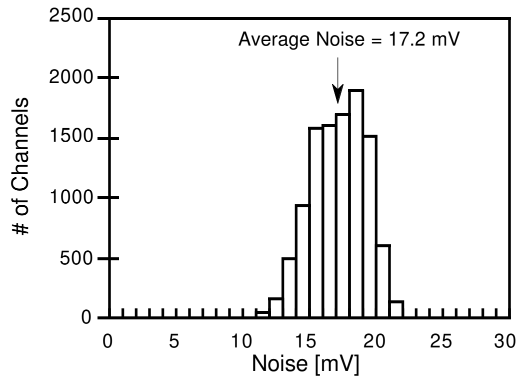

Fig. 7. Distribution of TEKZ noise.

Note that the matching of the gains is much better than a noise sigma, which is important for the operation of many chips with one threshold value only.

Figure 8 shows the yield averaged over the six wafers: we found 72% of the chips had no bad channels.

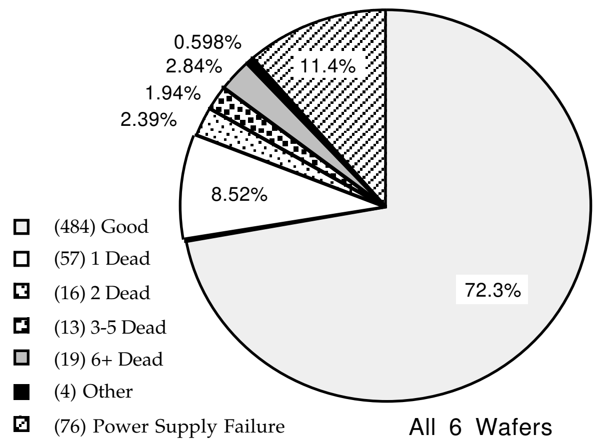

Fig. 8. Yield of 669 TEKZ chips with 32 channels tested.

We cross-checked on a limited number of chips that the remaining 32 channels showed a similar yield profile. For the assembly, we selected chips with no fault on the measured channels, and thus accepted a small number (0.2%) of dead channels on the unmeasured ones.

3.2 Testing of the CMOS Digital Time Slice Chip

The CMOS chips were tested at UTMC using test vectors derived in the simulation of the design. The selection criteria of a fully functional chip was principally based on the measured current draw. Because a few percent of the CMOS chips were found to be defective after bonding, we spot-checked the functionality of about 10% new chips using a HP16500A Logic Analyzer. Based on the fact that all of these tested chips were found to be functional, we concluded that the failures were introduced during the assembling and bonding process and stopped additional testing.

4. ASSEMBLY AND TESTING OF DETECTOR MODULES

The detector modules were assembled on hybrid planes manufactured at CERN in a Cu-INVAR sandwich technology which matches the coefficient of thermal expansion of silicon. Figure 9 shows a drawing of a detector module with its components. Note the large cut-out in the silicon detector which follows the beam profile and allows the placement close to the beam, The width of the ellipse depends on the shape and size of the beam envelope at the detector location. Up to 16 chip pairs servicing 64 channels each are assembled on one hybrid board. To prevent oscillations and pick-up of digital signals, analog and digital signals and power are routed in different planes of the hybrid. Moreover, the power to the amplifier chip is bypassed with filter capacitors at every second chip pair.

The assembly was performed at PROMEX [8], a commercial multi-chip assembly house. Rework was necessary on about 5% of the chips and was done in the SCIPP laboratories. The sequence of extensive tests before, during and after assembly is described in Ref. [3]. Here we want to mention that as a final test after assembly, we performed a laser scan using a penetrating 1064nm laser [9], where dead or noisy channels were identified. These “maps” were used later, after installation in HERA, to verify the integrity of the read-out chain.

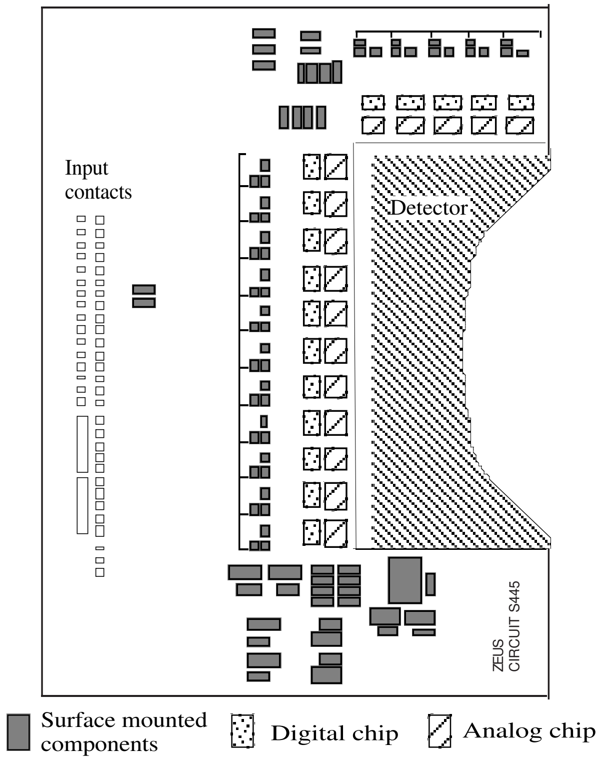

Fig. 9. Schematic of a hybrid board.

5. PERFORMANCE of the FEE DURING ZEUS DATA TAKING

During the 1994 data taking, the LPS, after an initial check-out, took data for a large part of the ZEUS running time. During the remaining time, unstable beam conditions in HERA prevented operation, and about 1/2 hr was spent every fill inserting the pots close to the beams. About 22,000 channels were operational in 26 planes in 6 pots in 3 stations, located about 60m, 80m and 90m along the outgoing proton beam. On-line programs allowed monitoring of the basic parameters, like channel maps, which were a primary tool to detect unsafe beam conditions.

We operated all detectors at a bias voltage in excess of depletion with the same threshold voltage on all planes. Although the control system allowed the use of a different threshold on each plane, we did not have to make use of this provision and set the value of all thresholds to 0.78fC.

5.1 Number of non-operable channels

Loss of efficiency was caused by several effects, with most of them identified by channel maps. Dead electronic channels, due to the fact that we tested only one half of the TEKZ chip, as mentioned above, and bad detector strips which were not bonded amounted to 0.5% of the channels. Then there were channels where the DTSC was “stuck” high. These and excessively noisy channels amounted to about 0.5% of the channels. They were identified at the beginning of each run and masked out during monitoring of the operation.

5.2 Occupancy

The occupancy per strip was measured in different operating conditions, using the LPS and ZEUS DAQ system [10]. With no beams present, threshold scans revealed the intrinsic noise performance of the system. During colliding beams operation, the beam crossing number (BCN) of the event allowed us to distinguish between the different origins of the hits.

Operation without beams:

With no HERA beams circulating and a random ZEUS trigger, the basic noise performance was extracted by varying the threshold voltage from 0.15 to 0.78fC. Figure 10 shows the channel map of one plane with 1024 channels at a reduced threshold of about 1/2 nominal. Like two thirds of the LPS planes, this plane has strips at 45^o relative to the detector sides, and the length of the strips varies from essentially zero (at channels #0 and 1023) to 6.2cm (at channel #387), and this causes the large occupancy fluctuations observed in Figure 10.

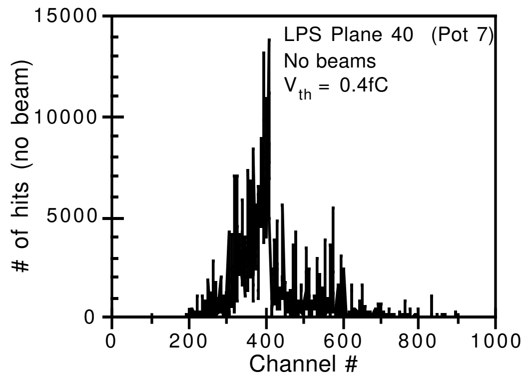

Fig. 10. Channel map for LPS plane 40 without beam at a reduced threshold of 0.4fC.

The reason is that the parasitic capacitance scales approximately with the strip length L and that the amplifier noise σ_n depends linearly on the capacitance C (in pF), as measured in Ref. [4],

$$\sigma_n = 680+40*C \ \ [\ e^-\ ] = 680+40*1.2*L \ \ [\ e^-\ ]\ , \qquad (1)$$

where the capacitance per unit length is taken as 1.2pF/cm, a number which includes additional noise sources like the amplifier noise due to coupling to the neighboring channel. Figure 11 shows the noise for plane 40 as measured with the calibration procedure (cf. Section 3.1) as a function of the strip length L.

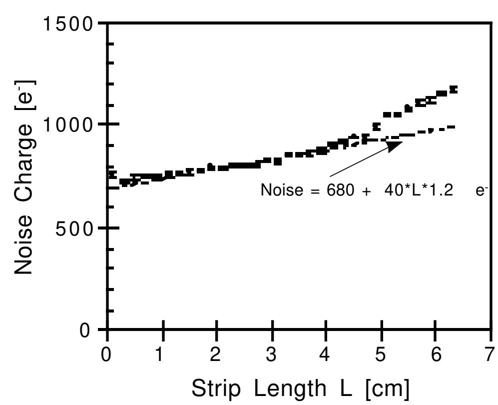

Fig. 11. Noise sigma as function of strip length for LPS plane 40.

The line is calculated using eq. (1). We observe excess noise at small length due to fixed capacitance of the bonding pads, and at large length, where leakage currents add to the noise, as discussed in Section 6.2 below. We can predict the occupancy, i.e., the number of hit strips per trigger, from the threshold V_{th} and the noise sigma σ_n. We have shown in Ref. [11], that the noise rate N is well described by an exponential function of the ratio of threshold voltage to noise voltage:

$$N = N_0 \cdot e^{-\frac{V_{th}^2}{2 \cdot \sigma_n^2}} \tag{2}$$

where N_0 is a function of the shaping time τ_S (for τ_S= 32ns, N_0=4.4MHz). Thus, for a DTSC clock rate of 10MHz, the maximum occupancy is 0.44.

We have extracted separately the occupancy for strips with high and low capacitance, as a function of the threshold voltage. In Figure 12, we show the occupancy as a function of the square of the threshold voltage, expressed in units of charge at the input, for three strips of different length L. The highest threshold shown is 0.68fC, less then the operating point, the lowest is 0.15fC.

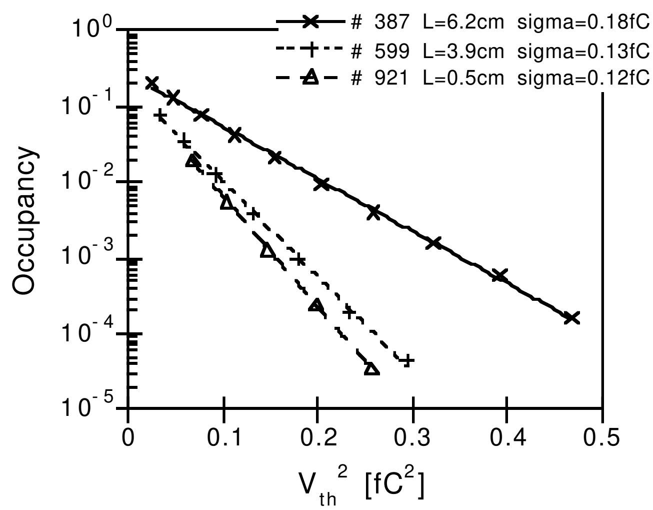

Fig. 12. Occupancy for three strips with different length on LPS plane 40 as a function of the square of the threshold.

Using eq. (2), we can extract the noise sigma σ_n from the slope of the curves in Figure 12 and compare it to the prediction of eq. (1) and the measurements of Figure 11. The values for σ_n are indicated in Figure 12, and in Table 1, where we show the measured and predicted noise sigma's for the three strips of different length.

Table 1. Calculated and measured noise σ_n for different strip length.

Region	Channel#	Striplength [cm]	C [pF]	σ_n[e$^-$],calc. Cap.{eq.(1)}	σ_n[e$^-$],meas Cal.{Fig.11}	σ_n[e$^-$],meas. Occ.{Fig.12}	i_{Leak}[μA] {eq.(3)}
LowC	921	0.5	0.6	704	750	760	≈ 0
MedC	599	3.9	4.7	867	860	825	≈ 0
HighC	386	6.2	7.4	978	1190	1113	1.0

The agreement between the two different methods to measure the noise sigma, calibration and occupancy, respectively, is excellent. The calculated and measured noise RMS agree well for small and medium length, but we observe excess noise for the longest strip, which we attribute to shot noise due to leakage current (see Section 6.2 below).

Operation with colliding beams.

Occupancies in the colliding beam mode were dominated by passage of particles and depended critically on beam conditions. Usually, position changes of the inserted roman pots of a few hundred microns could change rates by factors of 10 or more. Given the fact that serious radiation damage starts at a proton fluence of 10^{12} p/cm^2, strip occupancies in excess of 1% had to be avoided. In Figure 13, the channel map of plane 40 is shown for a luminosity run of 40mA protons on 15mA positrons: the occupancy is now almost directly proportional to the strip length, due to the random nature of both the halo protons and the synchrotron radiation from the positrons.

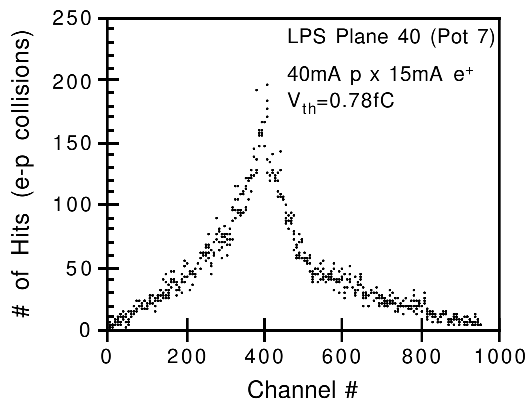

Fig. 13. Channel map for LPS plane 40 with colliding beams at the nominal threshold of 0.78fC.

The average occupancy per plane during luminosity shown in Fig. 13 is larger than that from random noise. By looking at the beam crossing number (BCN) of the events, we can separate the different contribution of protons and synchrotron radiation to the occupancy. About 10% of the BCN are completely empty, and about 10% have protons or positrons only, respectively. In addition, we observed that the synchrotron radiation came from the incoming positron beam, thus preceding the e-p collisions by several beam crossings.

The different contributions to the average strip occupancy are shown in Fig. 14 separately for the 6 LPS planes. They are noise ("No Beams"), noise and synchrotron radiation together ("Synchrotron Radiation only"), noise and single protons ("Protons only"), noise and protons from collisions ("e-p Collisions, no Synchrotron Radiation") and noise, protons from collisions and synchrotron radiation together ("e-p Collisions + Synchrotron Radiation").

As expected, the noise contribution to the occupancy is smallest and varies between 0.5 and $3.5*10^{-4}$. Synchrotron radiation and single protons add about 10^{-4} each. Protons from e-p collisions give larger contribution (3 to $6*10^{-4}$) due to the larger emittance of the colliding bunches. The full colliding beam occupancy can actually be calculated from these separate occupancies, which validates our method. Aside from differences in the noise background, mainly due to leakage currents, we see remarkable similarities in the occupancy rates from different sources in pots of the same station, which have the same distance from the interaction point and from the incoming positron beam (pots 4&5, 6&7, 8&9, respectively).

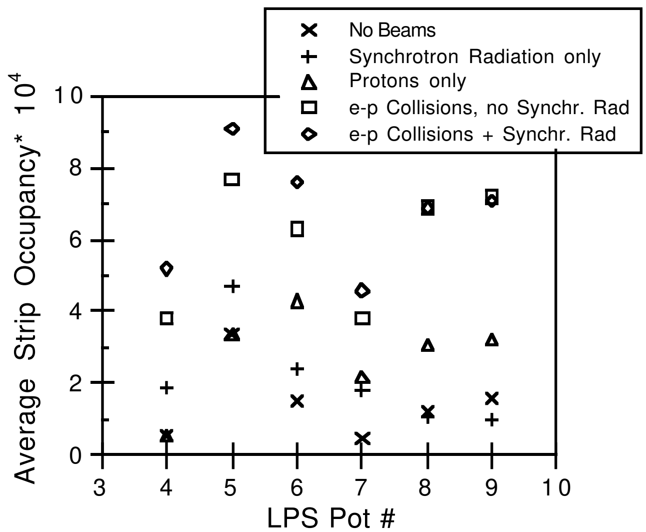

Fig. 14. Average strip occupancy of six LPS pots at the nominal threshold of 0.78fC, extracted from the BCN plots.

5.3 Common Mode Noise

As mentioned above, we have controlled the FEE system with one threshold set to the same value of 0.78fC for all channels. It was maintained with an accuracy of a few percent. We have not seen any common noise problems: the noise rate was constant during the runs and the occupancy was only a function of beam conditions and did not exceed a few % per plane.

We monitored the multiplicity per detector plane, for every roman pot and the whole LPS separately and found no large fluctuations. Figure 15 shows the total number of hits summed over all 26 LPS planes for 58,000 events during a ZEUS data run. As can be seen, the number of events with more than a few hits is small, and decreases exponentially for large numbers of hits (a total of about 300 events have more than 100 LPS hits). The average number of LPS hits for 22k channels is 8.6 hits/event.

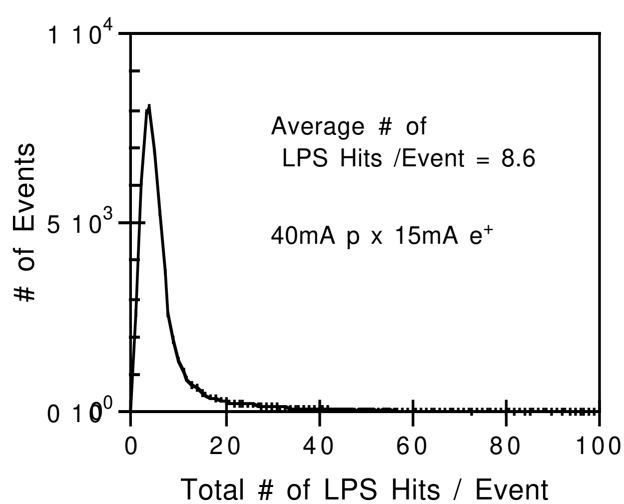

Fig. 15. Hit multiplicity of all 26 LPS planes during a colliding beams run.

6. RADIATION HARDNESS

6.1 FEE

The radiation hardness of the bipolar Tektronix SHPi and the UTMC CMOS process have been extensively tested on the transistor [12] and chip level [13], both with gamma and proton sources up to total doses of 5Mrad and fluences of $1.1*10^{14}$ p/cm. The CMOS devices showed threshold shifts of about 200mV, which ensures reliable digital operation. For the bipolar transistors, we found a degradation of the current gain β at the low level of collector current (100μA) they operate at. This is shown in Figure 16, where the emitter currents are scaled to correspond to 100μA for the N8 transistor.

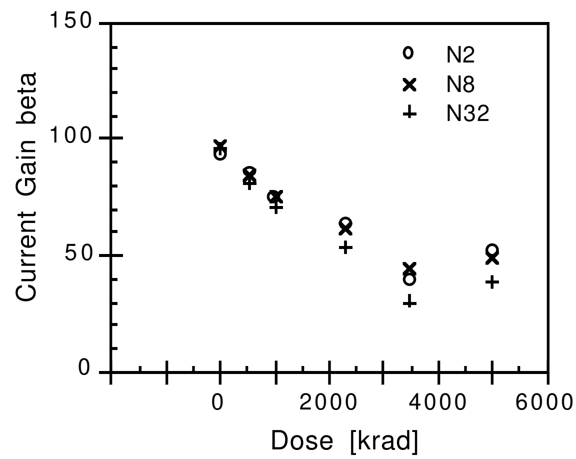

Fig. 16. Current gain β vs. total ionizing dose for three transistor sizes of the Tektronix SHPi process.

After an irradiation of about 5Mrad of gamma's from ^{60}Co, the current gain is reduced by half. The point at a dose of 3.5Mrad is from an irradiation with protons, and shows evidence for displacement damage. The design of the TEKZ amplifier took the β degradation into account and an irradiation of the full chip (Figure 17) showed constant gain and noise up to a gamma dose of 3.6Mrad.

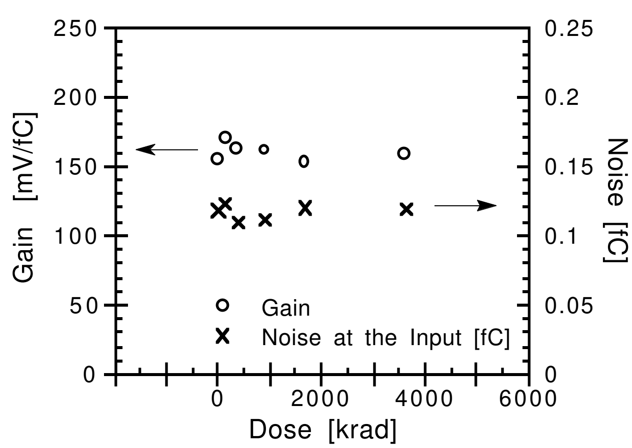

Fig. 17. Gain and noise for the TEKZ amplifier chip during ^{60}C0 irradiation.

During HERA operation, the LPS detectors are subject to irradiation from protons and neutrons from the beam halo and from beam accidents and photons from synchrotron radiation. Radiation levels can be inferred from the increase in leakage currents during proton operations and the occupancies when beams are present. We estimate a total dose of about 40krad at the FEE, with protons and synchrotron radiation contributing about the same amount. At this level of radiation, we do not expect radiation damage to the FEE, and indeed, gain and noise have been constant during operation, as shown by calibration runs.

6.2 Detectors

We have observed short-term radiation damage to the silicon detectors at radiation levels much smaller than anticipated. The damage shows up as increased leakage current during LPS operation close to the beams, but with a short term annealing time of a few hours. The currents were logged continuously for every plane. Large increases were observed when the planes were operated close to the beam, followed by exponential annealing as soon as the detectors were moved out or the beams were turned off.

This increase in leakage current was also observed as an increased electronics noise, both during calibration runs taken right after operations close to the beams and in the occupancy plots as function of threshold, as described in section 5. The noise contribution due to a leakage current i is

$$\sigma_n(i) = \sqrt{\frac{2i\tau_s}{e}} \quad , \qquad (3)$$

which amounts to 630 electrons for $i=1\mu A$, and this noise has to be added in quadrature to the noise sigma of eq. (1). In Table 1, we show the observed noise shortly after LPS operation, and we observe a discrepancy with respect to the expected noise only in the long strips with higher capacitance, which are close to the beams. We deduce from the noise increase a current of about $1\mu A$ per strip, using eq. (3). The sum of the currents of all strips calculated from the excess noise equals the total observed detector current.

7. CONCLUSIONS

We have operated 22,000 channels of fast, low noise, low power FEE in the 26 planes of the LPS at HERA. We control the noise of the binary system with one threshold of 0.78fC. The occupancy is extremely low and is, without beams, strictly a function of detector capacitance and detector leakage current. During colliding beams operation, the average number of hits observed in all 26 planes is 8.6. We do not observe any indication for common mode noise, and attribute this to the careful design of the bipolar FEE.

8. ACKNOWLEDGMENTS

We thank our colleagues from the ZEUS and LPS collaborations for technical help and fruitful discussions. This work was supported in part by the US Department of Energy.

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FIGURE CAPTIONS

Fig. 1. Block diagram of the FEE system.
Fig. 2. Circuit diagram for one channel of the bipolar amplifier-comparator chip TEKZ.
Fig. 3. Functional circuit diagram of the amplifier-comparator chip TEKZ.
Fig. 4. Block Diagram of the Digital Time Slice Chip DTSC.
Fig. 5. Extraction of the gain and noise from the occupancy curves with 1fC and 2fC test pulses.
Fig. 6. Distribution of TEKZ gains .
Fig. 7. Distribution of TEKZ noise.
Fig. 8. Yield of 669 TEKZ chips with 32 channels tested.
Fig. 9. Schematic of a hybrid board.
Fig. 10. Channel map for LPS plane 40 without beam at a reduced threshold of 0.4fC.
Fig. 11. Noise sigma as function of strip length for LPS plane 40.
Fig. 12. Occupancy for three strips with different length on LPS plane 40 as function of the square of the threshold.
Fig. 13. Channel map for LPS plane 40 with colliding beams at the nominal threshold of 0.78fC.
Fig. 14. Average strip occupancy of six LPS pots at the nominal threshold of 0.78fC, extracted from the BCN plots.
Fig. 15. Hit multiplicity of all 26 LPS planes during a colliding beams run.
Fig. 16. Current gain β vs. total gamma dose for three transistor sizes of the Tektronix SHPi process.
Fig. 17. Gain and noise for the TEKZ amplifier chip during ^{60}C0 irradiation.