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Testing the Yield of an Amplifier-Discriminator Chip Fabricated in Tektronix SHPi*

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Abstract

In Fall, 1992, over 600 TEK-Z amplifier/comparator chips were received from Tektronix for use in the ZEUS LPS system [1,2]. The yield was tested by looking for different failure modes, including excessive current draw, dead channels, and poor gain. A probe card connected 32 of the 64 outputs, plus power supplies and four calibration inputs. 484 chips had no flaws, while 184 were found to have at least one dead channel, short circuited power supplies, or low gain (72% yield). Average gain among functional chips was 167 ± 7 mV/fC, and average noise was 660 ± 80 electrons. This note discusses the test method, failure modes encountered, and overall yield.

I. TEST SETUP

Figure 1 shows the test electronics. The primary test for the TEK-Z chip was made using the 4 built-in calibration lines, each of which is attached to the input line of 16 amplifiers through a capacitor of approximately 14 fF. The calibration pulses are generated by a custom pulse shaper/multiplexer unit which can select any one of the four calibration lines and select between a 70 mV and 140 mV test signal. A CAMAC output register allowed the Macintosh software to select calibration line and signal size.

A start command to the gate generator produces the calibration signal. This signal is shaped into a 70 or 140 mV high, 2 ns rise step function, and sent to one of the four TEK-Z calibration lines.

The digital TEK-Z outputs are designed to drive a high-impedance CMOS chip using short bond wires. We did not have space on the probe card for amplifiers, so we simply placed series resistors on the outputs (120 ohms) and capacitively coupled into a 50-ohm ADC input. A Transiac multimeter module ("SAM") was used to measure the DC offset of each channel (before the capacitor). With the 120 ohm resistors, the signal at the ADC was typically 50 mV high and 40 ns wide, and the output impedance seen by the TEK-Z was large enough to prevent damage.

An HP 6624A power supply was used to provide three voltage supplies (5, 3.2, and 2.2 volts) and the threshold voltage, with a resolution of about 6 mV.

The standard test procedure was as follows. We select 25 chips from one wafer and place them on a aluminum waffle, which has 25 indentations milled in its surface for the dice and vacuum to hold the chips in place. The waffle is placed on the chuck of an automatic probe station, which is connected via GPIB to the Macintosh. The software on the Mac controlled automatic probe station movement, providing a more efficient method of placing the probe card on the chip.

Aligning the probe on the pads is a demanding task since there are four degrees of freedom: two horizontal translations, the angle between probe card and chip, and the vertical distance between probe card and the chip. The waffle was used because the chips had been diced by the manufacturer. Once diced, the chips are considerably more difficult to probe using automatic methods. Die placement cannot be ensured to better than 100 µm even when carefully placed in the waffle, so final probe alignment must be done manually using the microscope for each die. The advantage of the automatic probe station, therefore, was to simplify bookkeeping, and to reduce the time required to manually align the probe on the die.

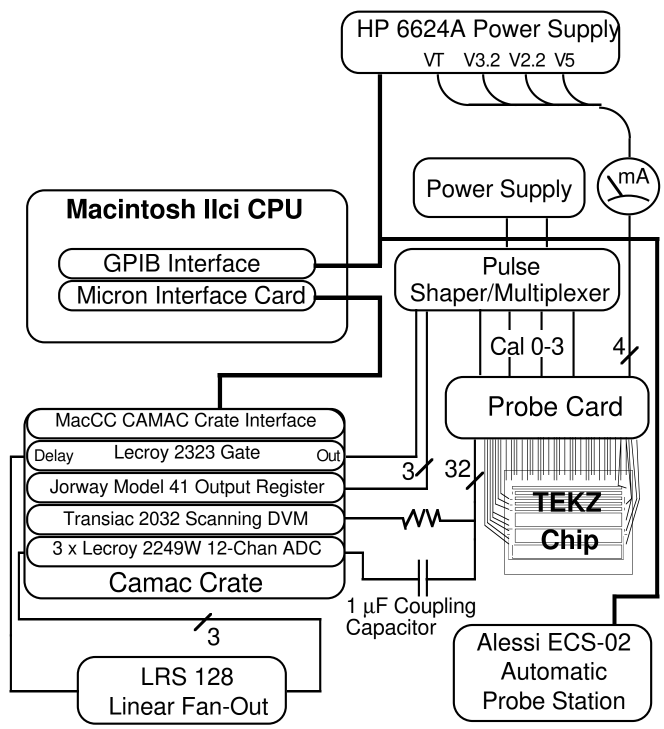


Fig. 1. Electronics for collecting data on TEK-Z chips.

Once the probe card is lowered onto the chip, a Macintosh program

- checks and records current and voltage for all supplies
- checks and records offset voltages for all output channels
- measures occupancy for each channel using 70 mV input pulse (i.e., about 1 fC), as a function of threshold voltage. Occupancy is the number of positive responses

divided by the number of gates, where a gate is sensitive to at most one response. Gates are 300 ns wide and each corresponds to one calibration signal. Typically 200 calibration signals are used to determine one value of occupancy.
- repeats the occupancy measurement for each channel using 140 mV input pulse (i.e., about 2 fC), as a function of threshold voltage.

Time required to test one chip was typically 1 minute to load and unload the die from the waffle pack, 1 minute to align the pads to the probe card, and 2 minutes for the test program to run.

In general, a plot of occupancy vs. threshold voltage closely approximates an error function, as shown in figure 2. Each set of these data was fit using a least-squares algorithm to an error function, defined by

$$\frac{1}{2}erfc\left(\frac{v_t - v_{off}}{\sqrt{2}\sigma}\right) = \frac{1}{\sqrt{\pi}}\int_{\frac{v_t - v_{off}}{\sqrt{2}\sigma}}^{\infty} e^{-t^2}\,dt \qquad (1)$$

where σ is a measure of the noise and v_{off} is the comparator offset plus the charge injected. σ can also be approximated by subtracting the 88% occupancy point from the 12% occupancy point (to obtain the FWHM for the corresponding gaussian) and dividing by 2.1.

The formula for the gain is

$$gain = \frac{\Delta V_{50\%}}{\Delta V_{cal} \times C_i} \qquad (2)$$

where $\Delta V_{50\%}$ is the difference between the two 50% occupancy thresholds of the chip, ΔV_{cal} is the difference between the pulse heights of the two calibration signals (70 mV in this case), and C_i is the calibration capacitance for this channel. Gain is expressed in mV/fC. Noise is determined by dividing σ from the 2 fC occupancy curve by the gain, and is typically expressed in electrons.

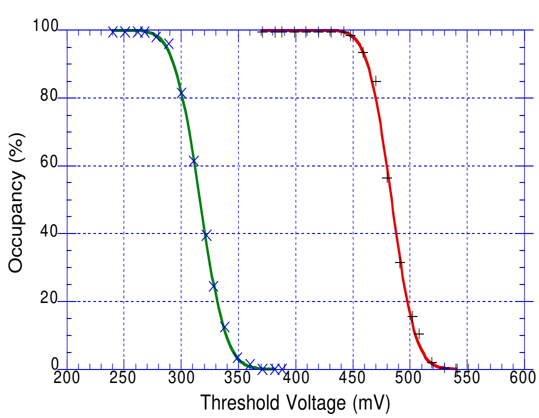


Fig. 2. Occupancy plot as a function of threshold voltage for input charges of 1 and 2 fC. The curve fits are error functions.

For example, figure 2 shows a typical TEK-Z response, in this case for the chip from wafer 13, row 6, column 10. In this diagram, the occupancy for channel 24 is plotted for two different calibration pulses, one at 70 mV and one at 140 mV. The curve fit is an error function. For this particular channel, the curve fits determined the 50% points to be at 316.6 and 484.1. The sigma values for the error function were 17.9 mV and 16.5 mV, indicating that the gain is 167.5 and the noise is 616 e^-. This analysis was repeated for each of the (~10^5) channels tested. Differences due to binomial statistics on the occupancy can be seen; this is the primary limitation on the precision with which noise can be measured.

II. Calibration Capacitors

The calibration capacitors for the TEK-Z varied by about 20%. Fortunately, these variations are caused by the mask of the chip, and thus seem to remain constant between different chips. Calibration capacitor values were measured for one chip, as shown in table I, using an HP 4284A Precision LCR meter.

Table I: Calibration Capacitances
Measured calibration capacitor values for 64 channels of the TEK-Z chip, in femtoFarad

0	14.7	16	13.0	32	12.6	48	12.5
1	14.5	17	15.2	33	13.3	49	13.2
2	14.9	18	15.2	34	12.9	50	12.8
3	17.1	19	17.1	35	12.2	51	13.2
4	14.8	20	13.0	36	12.5	52	12.5
5	14.8	21	15.1	37	13.0	53	13.1
6	13.1	22	13.4	38	12.8	54	12.8
7	17.2	23	12.7	39	13.7	55	15.1
8	14.8	24	14.7	40	12.5	56	12.5
9	13.3	25	15.3	41	13.2	57	13.2
10	13.3	26	15.2	42	12.7	58	13.0
11	17.4	27	13.2	43	13.1	59	15.0
12	14.9	28	14.6	44	12.7	60	12.3
13	15.1	29	15.1	45	13.1	61	13.2
14	15.2	30	13.0	46	12.9	62	13.1
15	17.2	31	12.8	47	13.3	63	12.5

The uncorrected gain, averaged over all of the chips tested, is compared to the measured calibration capacitances in fig. 3. The correlation is quite good, indicating that the calibration capacitance measurements shown above can be trusted to about the 3% level.

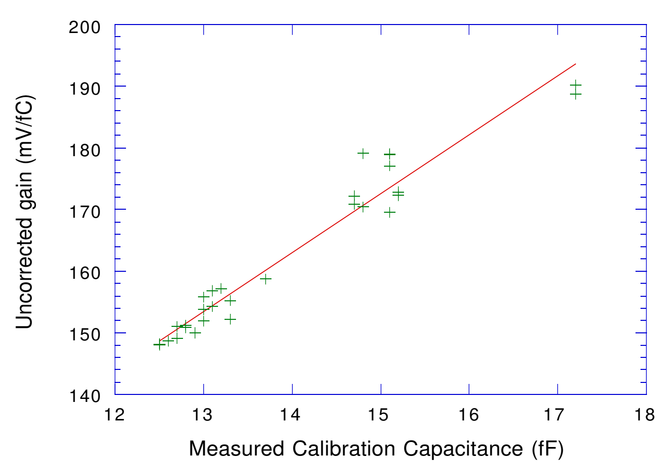


Fig. 3. Calibration capacitors.

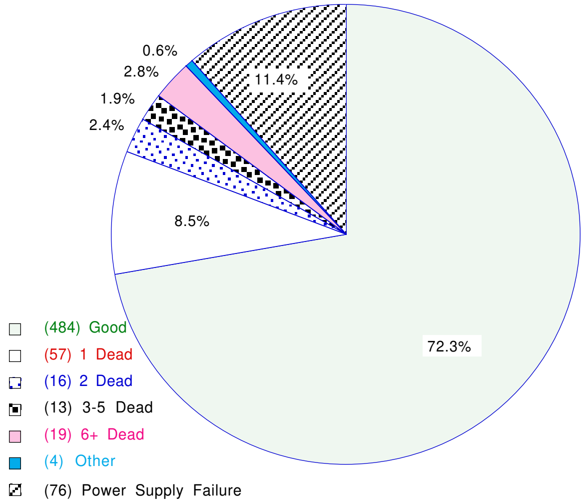


Fig. 4. Failure modes encountered. Most of the power supply failures occurred on wafers 9 and 10.

III. YIELD

One run produced 6 wafers of chips which were tested as described above. We were pleased to find that more than 70% tested without problems. The pie chart shown in figure 4 shows frequency of various problems. Performance varied by wafer as well, as shown in figures 5 and 6. The worst two wafers, 9 and 10, had many chips with power supply failures near the edges.

We predict that another ~8% of the chips which are presently listed as "perfect" would be found to have an additional channel dead if the other channels on these chips were tested, and perhaps 10 chips would have 2 dead channels. This assumes that the failure rate of .65%/channel holds for the other 32 channels.

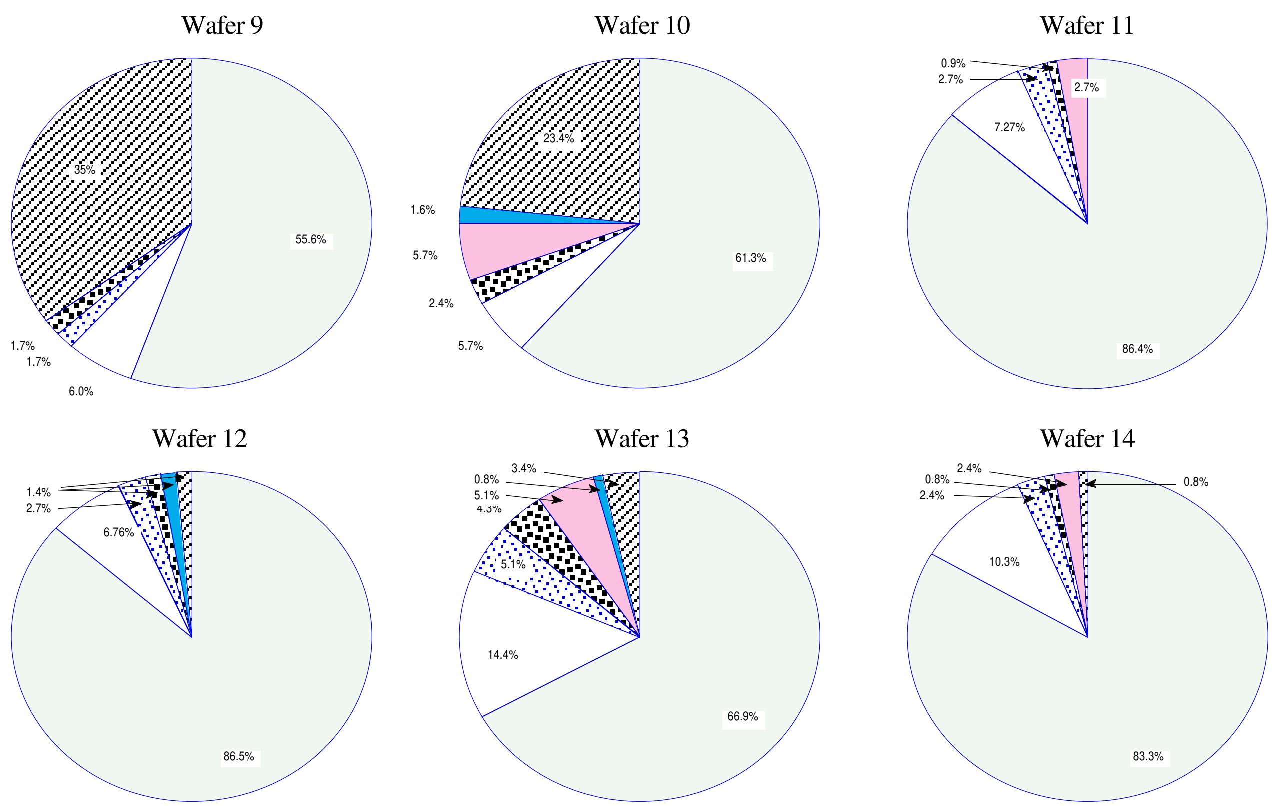


Fig. 5. The yield varied considerably between different wafers. See fig. 4 for a description of the failure modes.

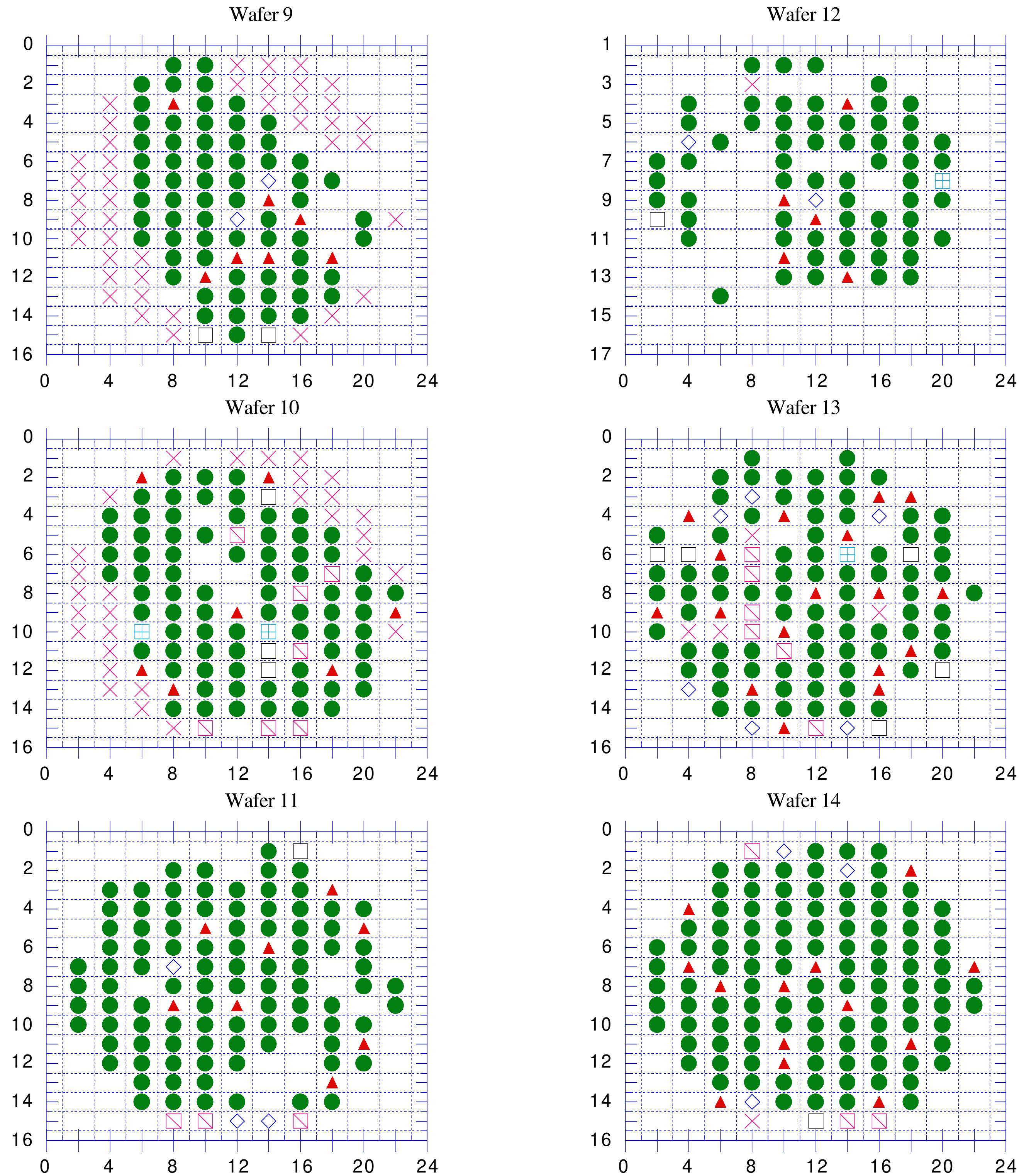
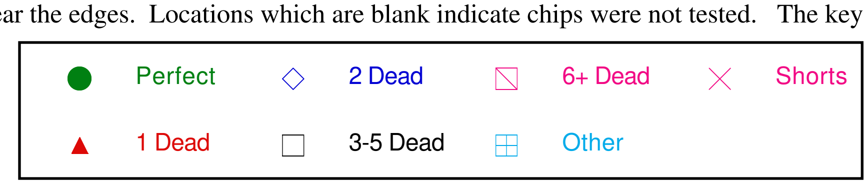


Fig. 6. These maps of TEK-Z wafers show the locations where failures were discovered. Notice that failures in wafers 9 and 10 were clustered near the edges. Locations which are blank indicate chips were not tested. The key is shown below:



IV. DATA

Figures 7 and 8 show the distributions of measured gain and noise for TEK-Z chips. These distributions indicate that a typical TEK-Z channel will have a gain of 167 ± 7 mV/fC and a typical noise of 656 ± 77 electrons. The variation in gain is mostly due to differences in TEK-Z gain and calibration capacitors, while the variation in noise is due to the testing method which has low precision for determining noise.

The noise measurement agrees remarkably well with the SPICE simulation run for the TEK-Z chip, which predicted 630 electrons of noise.

Power consumption of the chips is shown in table II, and their distribution in fig. 9. Power consumption was typically 121.5 mW and never exceeded 130 mW for the chip. We hoped that power consumption could be used to indicate the whether all channels were working on a chip, but unfortunately we did not observe a correlation between power consumption and number of working channels.

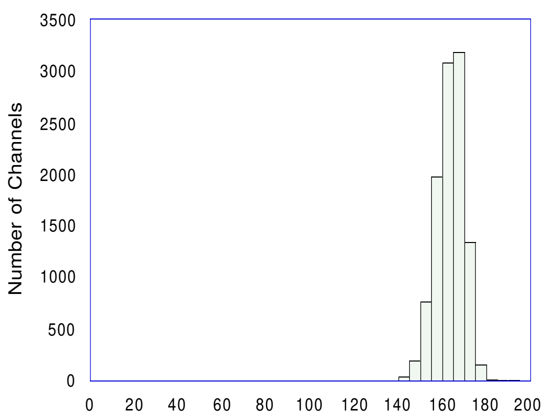


Fig. 7. Histogram of gains measured for TEK-Z chips.

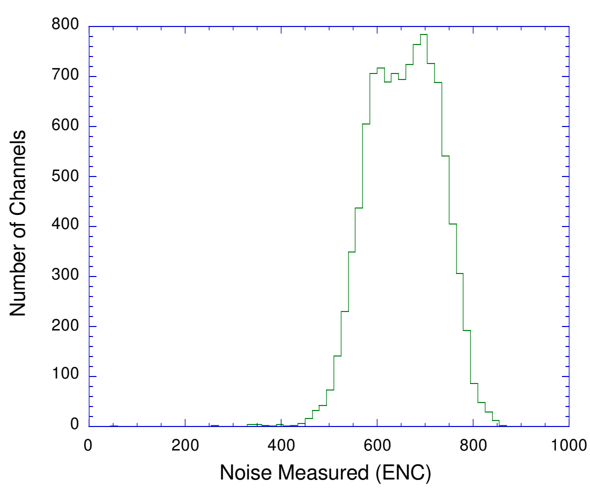


Fig. 8. Distribution of measured noise values.

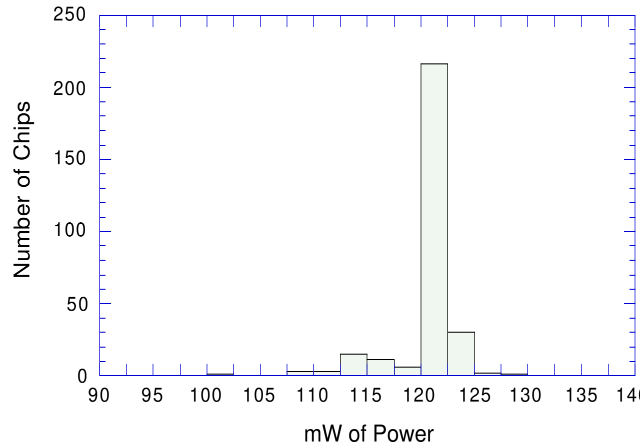


Fig. 9. This diagram shows the distribution of power consumed by the TEK-Z.

Table II
Power consumption by supply for TEK-Z chip

Power Supply Voltage	Median Current	Maximum Observed Current
VT	-2.0 mA	-3 mA
V2.2	8.7 mA	10 mA
V3.2	22.0 mA	24.0 mA
V5	6.4 mA	7 mA

V. FURTHER TESTS

A probe card for testing the other 32 channels is available, but it is unlikely that all chips will be tested with it. Instead, about 50 will have been tested, and no unexpected results were found. Two additional wafers of TEK-Z have arrived, with six more to arrive shortly; these will be tested in the near future.

VI. REFERENCES

* Research Supported by Texas National Research Laboratory Commission.

[1] E. Barberis, *et al.* "A Fast Shaping Amplifier-Comparater Integrated Circuit for Silicon Strip Detectors." *IEEE Nucl. Sci. Symp.*, Orlando, FL Oct. 27-31 1992.

[2] E. Barberis, *et al.* "A Low Power bipolar Amplifier Integrated Circuit for the ZEUS Silicon Strip System." *3rd Int. Conf. on Adv. Tech. and Part. Phys.*, Como, Italy, June 22-26 1992.