VME Trigger Card Manual

Erik Blaufuss
University of Maryland

December 5, 2002

Abstract

This memo provides an introduction to and information about the VME trigger card in use at Milagro. Hardware settings and software settings sections are included. Information on accessing the data output to the latch and recorded in the Milagro data structure is also included.

UPDATED: November 27, 2002 for v2.0 of card.

1 Introduction and overview

The VME Trigger Card has been designed as a replacement to the previous CAMAC discriminator trigger. In addition to being able to function as a computer-programmable discriminator, the trigger card has the ability to reject or accept triggers based on the measured risetime of the analog sum pulse. The ability to pre-scale any trigger type is also included. Front panel inputs for external triggers (e.g. calibration) and for trigger veto signals are also included. An LED on the front panel is on each time the card issues a trigger to the DAQ.

The primary function of the card is to monitor the analog sum signal from the front-end boards and generate triggers based on what it sees. The card operates with an 80MHz clock, therefore monitors the analog sum pulse with a time resolution of 12.5 ns. When the analog sum pulse exceeds a "pretrigger" condition, a programmable level, the card then latches a FIFO containing 25 entries (a 312.5 ns long snapshot of the analog pulse sum). Each entry of the FIFO contains the output of the A-D converter in units

of 5mV "card units" (roughly corresponding to 5/6 of a tube in the analog sum). The FIFO is filled with 10 entries that occurred before the pretrigger condition was exceeded and 15 entries that occurred after.

For each pretrigger seen, the card finds the peak value in the FIFO, as well as the risetime. The risetime is defined as the number of FIFO entries it takes for the analog sum pulse to rise from 12.5% to 88.5% of the peak value. The risetime and peak value found are then compared the programmed levels in the card and a trigger is issued if the risetime and peak values exceed the programmed levels. While the risetime and peak values are being found, the card is dead to other activity on the analog sum pulse. If a pretrigger is found, but no detector trigger is formed, the card is dead for 1.5 μsec. If a trigger is issued, the card is dead until the DAQ inhibit signal is removed (typically 10-20 μsec). The removal of the inhibit signal clears the card, and all latch outputs, preparing the card to search for the next trigger.

To monitor the total detector dead time, the card also outputs a "busy" signal, which is gated with the 10 MHz signal from the GPS clock and is counted on a scaler channel. This is used to measure the total dead time of the experiment and this measured value is on the EMS homepage as the "VME Trigger Dead Time". The "busy signal" is started once a pretrigger is found and the card is no longer monitoring the analog sum. The signal is cleared by either the card (if no trigger is generated) in 1.5 μsec or by the falling edge of the DAQ inhibit signal, after the previous trigger's data has been buffered. This busy signal is inverted (busy is low), and is only "on" when the card is available for triggers. Therefore, when the card is powered off, the deadtime will be measured to be 100%.

The card can accommodate up to 16 unique trigger types, which can consist of programmable triggers based on the analog sum, and/or based on information from daughter cards, and/or information from front panel external trigger inputs and the veto input. Each trigger type has a unique trigger bit in a 16 bit trigger word. The trigger ID, as well as the measured PMT count and risetime of the analog pulse that generated the trigger are output to the front panel ECL output to be latched in the FSCC crate and are included in the raw data structure.

The front panel also has 3 inputs available for future daughter cards. These daughter cards could be designed to measure any quantity and pass that information to the trigger card for consideration in the trigger decision. Currently no daughter cards are installed, but work is underway to build daughter cards that count the number of muon layer tubes above a fixed

threshold. This value then can be used in the trigger decision in the programmable trigger logic. More spots are available, so if you have a good idea for a special trigger, please talk to me.

The Altera chip at the center of the trigger card is programmable, so that as new ideas are developed, the trigger algorithm can be changed. This programming is not performed over VME, but rather with special Windows software from Altera. Currently, the card is programmed with 5 different triggers based on threshold and risetime. Each of these triggers has its own VME programmable threshold, risetime, prescale factor and veto accept/ignore flag.. Information on these settings can be found later in this memo.

2 Hardware settings

The card is installed in the VME crate near the DPM modules. This section covers installation and proper connection of the card. Also included are information about changing the VME memory address of the card and instructions for adjusting the DC offset of the card. Figure 1 shows the trigger card in the VME crate. Figure 2 shows the trigger card from a side view and shows the configuration switch bank and programming port.

2.1 Installation in the VME crate

Normally, the VME trigger should already be installed in the VME crate with all connections already made. The card can be inserted in any open slot of the VME crate (except slot 1, which is reserved for the VME crate controller). Make sure that the power to the VME crate is off when inserting and that the card is fully seated before turning the crate on. Please use the lock screws when putting the card into the crate to prevent it from coming loose.

The following cables need to be attached for proper operation. Each of these cables has a labeled location on the VME trigger card:

- Analog Sum- A copy of the analog sum pulse from the front-end boards is input to the trigger card in the "Analog Sum" input. Currently, this input is capacitively coupled to remove any DC offset.

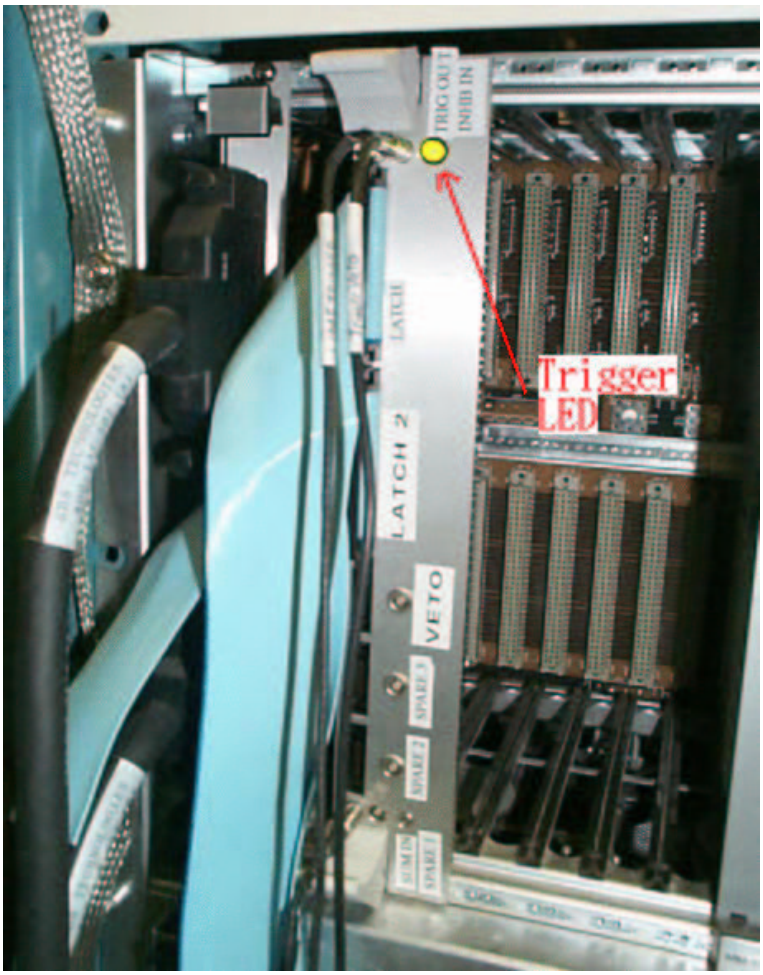

Figure 1: VME trigger card in crate. Trigger LED is on each time a detector trigger is issued.

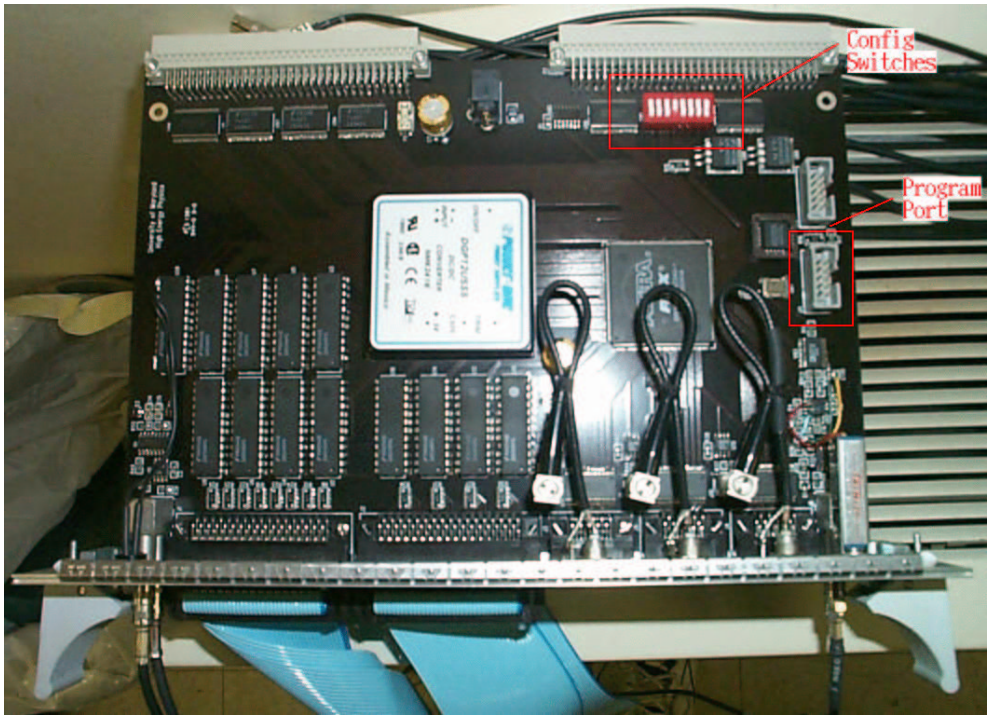

Figure 2: VME trigger card. Shown are the set of configuration switches and the programming port to reprogram the Altera chip.

- Trigger Inhibit- This input tells the trigger card when the DAQ is busy and can not accept another trigger. The falling edge of this busy signal clears the VME trigger card and starts it looking for another trigger. This is also used to monitor the detector DAQ deadtime.

- Trigger Out- The output to the DAQ global trigger. Issues common stops and starts the digitization process on the TDCs.

- Ext Trgs- The card has 3 external trigger inputs on the front panel. If a NIM level pulse is sent into any of these inputs, all information about the current analog sum levels are lost and a trigger is issued 100 ns later.

- Latch Output 1- This 32 bit output to the FastBus latch carries the measured risetime, PMT count and trigger type for the current trigger. All this information is latched in the raw event data structure and some of it is stored in the REC data.

  The bits output are assigned in the following manner on Latch Output 1:

  - 0-15: 16 unique trigger IDs. Each bit corresponds to one numbered trigger. Currently 0-4 are the 5 programmable triggers and 13-15 are the 3 front panel external trigger IDs.
  - 16-20: 5 bits of risetime information. 16 is LSB. 20 is MSB.
  - 21-22: Are only used for development diagnostics and should be ignored.
  - 23-31: Are the 9 bits of PMT count information, corresponding to the size of the peak in the analog sum pulse in 5mV counts. 23 is LSB and 31 is MSB.

- Latch Output 2- This is an additional channel to output information. Currently it contains a 16 bit event counter and the "Busy" signal from the card. Additionally, the 5 programmable trigger types are mirrored on this output for counting in the scaler system. The event counter is currently not implemented due to a lack of free latch space.

  Only 16 bits of this 32 bit output are used. These bits are sent to an ECL-NIM converter near the scaler system. The bits are assigned as follows:

  - 0 bit: BUSY signal. When this bit is high when the card is ready to trigger and low when busy. The busy signal is gated with the 10 MhZ GPS clock pulse and counted in the scaler system.
  - 1-5 bits: Output bits for the scaler system for the 5 programmable triggers. Bits are scaled each time a trigger is issued with that trigger ID active.
  - 6-15 bitsAre only used for development diagnostics and should be ignored.

- Veto In- Front panel connector where a NIM level pulse can be applied to veto selected triggers. The decision to veto triggers is made trigger by trigger depending on the value of the trigger veto word programmed over VME. A veto must be asserted <200 ns after the pretrigger level is passed and held for at least 500 ns to be properly registered.

The Analog sum pulse, trigger inhibit, and trigger out need to be attached in order for the DAQ to operate properly. Check these cables if triggers are not being properly generated.

2.2 VME address setting

The VME address is set on the switch bank ("Config Switches") shown in Figure 2. Switches 1-4 are used to set the most significant bit of the VME address. These switches are "true" when in the "off" position.

The default value of the VME address is set to `0xE0000000`. The switch settings to generate this address are Sw1:On; Sw2,Sw3,Sw4: Off. Please contact me if you find a reason why the VME address should be changed. This value is needed by the DAQ computer system that reads out the VME crate.

2.3 DC offset adjustment

The card uses an ADC to sample the size of the analog sum pulse as a function of time. The analog sum pulse, when not capacitively coupled, can have a DC offset, which can effect the trigger thresholds. The trigger card has a front panel adjustment to account for this DC offset. The adjustment needs to be checked every now and then. The adjustment procedure depends

on if a capacitor is being used in the analog sum pulse input to the trigger card.

If a capacitor is used:

1. Remove the analog sum from the front panel.

2. Monitor the Trigger Out signal with a scope.

3. Toggle switch #5 on the switch bank to "Off". This places the card in "calibration mode". In this mode, the card will repeatedly trigger if the DC offset of the ADC is found to be greater than zero. If you need to remove the trigger card from the VME crate to make this change, be sure to turn off the crate power.

4. Adjust the front panel adjust screw until the triggers seen on the scope start to stop. This means you are near the zero point of the ADC. If you adjust too far past this point, you will create a negative offset. You want to be just at the point where the triggers stop.

5. Return switch # 5 to the "On" position (for regular mode) and reattach the Trigger Out line to the rest of the DAQ.

If no capacitor is used, you should leave the analog sum pulse in place (step 1), but turn off the high voltage to all tubes. Then follow the above procedures to make the adjustment. This will allow you to take into account any DC offset in the Fan-Ins that generate the analog sum pulse might have.

2.4 Delayed trigger output

Starting with version 2.0 of the card firmware, the option to delay the trigger by 750 ns has been included. This feature should be on to ensure all outrigger edges are properly registered before the trigger is issued. This feature is turned on by setting Toggle Switch 6 on switch bank to the ON position. This should be the default setting.

3 Software setting

The trigger levels, risetime cut values, veto and prescale information are all programmed into the card at run start time over the VME interface. Once a

run is going, it is not possible to change these settings, as it interferes with the readout of the DPMs. The settings programmed into the card set the criteria for each trigger. This section discusses how and where to set the programmable levels in the card. Instructions for flashing a new program into the Altera chip are also included. The instruction set for the Altera chip only need to be updated to add new functionality.

3.1 Programmable levels

The trigger card needs 17 values programmed over the VME interface at run start time to configure the 5 programmable trigger levels. These values are stored on kahuna in:
`/INFO/setup/VMETrig.txt`.
The file `/INFO/setup/VMETrig.txt.EXAMPLE` contains an an annotated version of the file and is useful when editing this file. Please keep in mind that all pmt trigger thresholds are measured in 5mV per tube counts. In the analog sum pulse, each tube really contributes about 6.1 mV per tube hit. The file contains:

- Entry 1 Pretrigger level: The level where the card starts looking for triggers. Needs to be lower than the lowest trigger level (one count difference is enough). The value of this determines the pretrigger condition. Figure 3 has the deadtime incurred by the DAQ from pretriggering only (with a fixed 4.5% readout deadtime) as a function of pretrigger level.

- Entry 2-6 Trigger thresholds for triggers 1-5: The threshold for the 5 programmable triggers, in order (5mV/tube).

- Entry 7-11 Risetime cut values for triggers 1-5: The measured risetime must be less than or equal to these set values to generate a trigger. For no risetime cut, set to 31.

- Entry 12-16 Prescale factor for triggers 1-5: The number of valid events of this trigger type to skip between generating a detector trigger. Useful for prescaling samples. Set to 0 to accept all of a trigger type. A value of 100 will skip 100 events between triggers, and will end taking 1 out of 101 triggers.

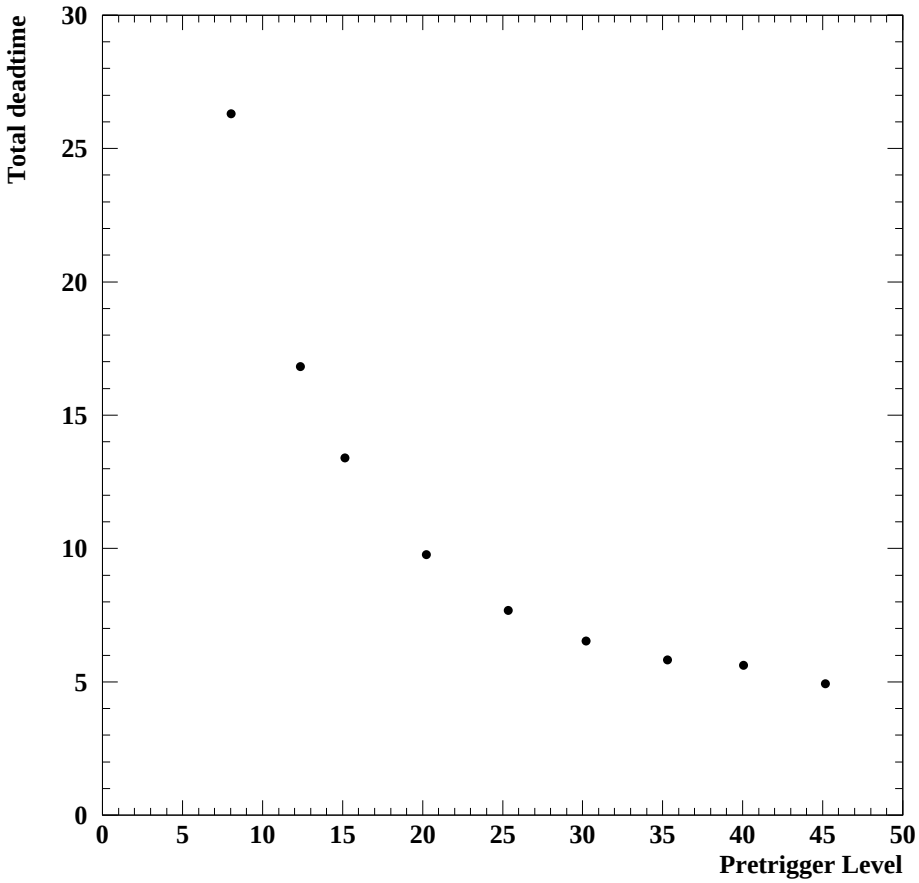

Figure 3: Deadtime in percent due to pretriggering as a function of the pretrigger level. The DAQ readout deadtime is fixed at 4.5% here.

- Entry 17 Prescale mask for all programmable triggers: Set the appropriate bit to "On" to have a a trigger use look at the "Veto IN" input on the front panel when considering the trigger logic. If the veto mask is set to "4", then programmable trigger 3 and only this trigger can be vetoed by the front panel veto, and all other programmable triggers will ignore the veto input.

3.2 Flashing the Altera chip

The Altera chip at the center of the trigger card is re-programmable. To add new functionality to the trigger card, a new set of code can be flashed into the card. This reprogramming is done with special software from Altera. The new program will be in the form of a filename.pof. To load this into the card:

1. Turn off the VME crate, remove the trigger card from the VME crate and attach the Byte Blaster cable to the programming port on the card shown in Figure 2. You do not need to remove the cables from the card.

2. Attach the other end of the cable is attached to the parallel port on the computer with the hardware key.

3. Put the VME trigger card back in the VME crate and turn the crate power on.

4. Start the computer and start the Altera MaxPlus software. Select the Programmer tool by clicking the icon on the toolbar with the ribbon cable in it (7th icon from right).

5. Once the programming tool is started, select the File Menu and choose the "Select Programming file..." option. Choose the .pof file to load into the card.

6. Choose the "Program" button. The new program will be loaded into the PROM on the card. It can take a couple of minutes.

7. Turn off the VME crate, remove the Byte Blaster cable, and return the card to the crate. Turn the VME crate back on. The VME crate power must be cycled to force the new program to be loaded into the Altera chip.

4 Information output to Milagro data structure

The information output to the latch is recorded into the data structure of each event. Some of this information is also saved in the Rec data. You need to be using offline version 57 or greater.

4.1 Raw Data

In the raw data structure, the trigger type, the risetime and the number of tubes found in the peak of the analog sum are recorded. This data is saved in the raw cmpEvent structure:

- risetime- `eventData.cmpEvent.trig.risetime`
  The risetime in counts. It is only 5 bits, and can range from 0-31 counts. Each count is 12.5 ns.

- PMT count- `eventData.cmpEvent.trig.count`
  The number of PMTs found as the peak size in the analog sum. It is 9 bits, and can range from 0-511. Please remember that this count is measured in 5mV "card tubes".

- Trigger type- `eventData.cmpEvent.trig.VMEword`
  The trigger type identified by the trigger card. This is a 16 bit integer that is made from the 16 available trigger types, each one representing one bit. A trigger VMEword of 9 corresponds to trigger IDs 1 and 4 being on for this event.

This information is also copied to the calibrated data structure: `eventData.calEvent.calData.trig.xxxx` after CalibrateRaw() has been called.

4.2 Rec Data

Due to size limitations of the rec data structure, only some of the information from the card for each event is currently saved in the Rec format. Eventually the size of the rec data will be increased to accommodate all trigger card information. The information currently in the rec data includes:

- Risetime- `eventData.recEvent.reconInfo.trig.risetime`
  The full 5 bits of risetime information are saved, and this value can range from 0-31 counts (12.5 ns/count).

- Trigger Type- `eventData.recEvent.reconInfo.trig.VMEword`
  The first 5 bits of the trigger word, which are the 5 programmable trigger types, are kept in the rec data.