An Amplifier-Discriminator Chip for the GLAST Silicon-Strip Tracker

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Abstract

An amplifier-discriminator circuit has been designed for reading data from the silicon-strip detectors of the Gamma Large Area Space Telescope (GLAST). For the 38 pF expected detector loading, an equivalent noise charge (ENC) of 1600 electrons has been demonstrated on a 32-channel chip with a power consumption of under 150 μW per channel and a 1 μs time constant. The typical rms threshold variation was under 750 electrons ENC. These results satisfy the requirements of the GLAST mission.

I. INTRODUCTION

The Gamma Large Area Space Telescope [1] is a satellite mission that is currently in its research and development phase, with a construction phase projected to begin around the end of the year 2000. GLAST is a gamma-ray pair conversion telescope that operates in much the same way as the EGRET experiment on the Compton Gamma Ray Observatory [2]. As a successor to EGRET, however, GLAST is intended to improve upon EGRET's sensitivity to astronomical point sources by factors of 10 to 100. That is accomplished primarily by taking advantage of silicon-strip detector technology developed during the past decade for applications in elementary particle physics experiments [3].

The GLAST detector consists of a square array of nearly identical tower modules, as indicated in Fig. 1. Each tower has a scintillator veto counter on the top (and on the sides for the edge towers), followed by a multilayer silicon-strip tracker and, finally, a cesium iodide calorimeter. Each of the tracking layers has two planes of single-sided silicon-strip detectors with strips oriented at 90 degrees with respect to each other. All but the bottom few layers have a thin lead foil preceding the detector planes, to convert the incident gamma-ray photons into electron-positron pairs, which are subsequently tracked by the remaining detector layers to determine the photon direction. Finally, the calorimeter absorbs the electrons and thereby measures the photon energy.

Besides providing optimal angular resolution for this type of device, the silicon-strip technology is fast, yielding a system with very little dead time, provides excellent multi-track separation, which is important for background rejection, and can be made self triggering. The latter two points eliminate the need for a time-of-flight system, such as used by EGRET for triggering, and thereby result in a very compact instrument with a wide, almost 2π steradian, field of view. The silicon-strip technology is by now well developed, is known to be robust, requires no consumables, such as gas, and operates at a relatively low voltage, compared with spark or drift chambers. It therefore appears to be ideally suited for space applications.

The GLAST instrument design has more than a million silicon-strip channels. Two clear limitations on operating such a system in space are the availability of power for the electronics and the difficulty of dissipating the resulting heat. Previous silicon-strip systems, designed for operation in ground-based experiments, or in space with a small number of readout channels, have not needed to contend with such severe power limitations. For those reasons, a principal goal of the research and development effort within the GLAST collaboration has been to design and test readout electronics that can meet the signal-to-noise requirements with minimal power dissipation.

II. TRACKER ELECTRONICS REQUIREMENTS

The limited power levels readily available from solar panels, together with the necessity of transporting heat from the instrument interior to radiators on the satellite periphery, dictate that the tracker readout electronics should not consume more than about 200 μW of power per channel. That includes the digital processing and data transmission as well as the amplifiers and discriminators.

Pulse-size analysis is not needed for GLAST, so the power restrictions naturally lead to a binary readout, with a simple single-threshold discriminator for each channel. The tracker must be self-triggering, however, so the electronics must produce a fast logical-OR of each entire detector plane, to be used as input to the trigger logic.

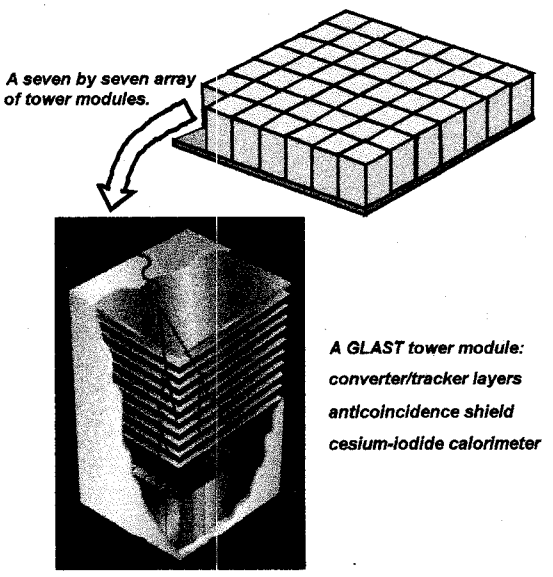

Figure 1: The GLAST detector concept.

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The noise occupancy for an instrument of so many channels should be low, 0.01% or less, to avoid overloading the data stream and trigger with noise hits. For the 400 μm thick detectors proposed for GLAST, that roughly translates into the requirement that the equivalent noise charge (ENC) not be more than about ¼ fC (1560 electrons). Also, since the discriminator threshold can realistically only be adjusted at one common level for each 64-channel chip, the channel-to-channel variation in threshold across a chip must be commensurate with the size of the stochastic noise.

The radiation exposure in the GLAST orbit will be modest compared with the environment of detectors in contemporary accelerator beams, with only about 1 kRad per year expected. However, it is crucial that the electronics be immune to latch-up that might be induced by impulses of radiation. It is also important that redundancy be built into the readout system, to avoid the possibility of catastrophic single-point failures.

It is desired that the readout system be able to accommodate trigger rates as high as 10 kHz with minimal dead time. This necessitates clocking out of data from the chips while the amplifier inputs are active. The amplifiers themselves must have a shaping time the order of 1 μs. That roughly balances the shot noise from detector leakage current (at end of life) against the amplifier noise and also insures an adequately short coincidence window for the trigger.

III. Prototype Chips

Two CMOS chips have been designed, fabricated, and tested at U.C. Santa Cruz for the GLAST tracker electronics development program. The first was a 16-channel amplifier-discriminator prototype, while the second was an improved 32-channel version, of which 59 have since been used in an extensive beam test run at the Stanford Linear Accelerator Center during October 1997.

Each channel includes a charge sensitive preamplifier, followed by an RC/CR shaping amplifier, a comparator, a digital mask, and a latch. The latches are arranged as a shift register, such that the latched data can be read out serially. In addition, there is a logical OR of the comparator outputs after the mask, to be used as a fast trigger, and a set of four calibration busses, each one coupled via a small capacitor to every fourth preamplifier input. The comparator threshold is set via external pads. Unlike the ultimate GLAST readout chips, these chips are not intended to be clocked while the amplifiers are actively acquiring data.

The principal issues in the design were power, noise, and threshold uniformity and stability. Because of the binary nature of the readout, there were no stringent requirements on linearity and dynamic range, and the speed requirements were modest. The architecture was roughly modeled after the front-end amplifiers of the BaBar SVT readout chip [4]. However, to save power and to match the GLAST bandwidth requirements, the active cascodes were replaced by simple cascodes, and the number of amplifier stages was reduced to two.

The first stage integrates the charge with a time constant that is determined by the input-impedance requirements and is short relative to that of the second stage. The second stage has roughly equal integration and differentiation time constants of about 1 μs. Its output pulse is unipolar, although the long reset time constant of the first stage results in some undershoot.

We expected a threshold variation of about 10 to 15 mV rms, so the overall amplifier gain was chosen to be 125 mV/fC. The noise goal then translates into 32 mV rms at the comparator input. If we require that the threshold be at least 4σ above the noise for 99% of the channels, then a threshold range of 160±30 mV (1.0 to 1.5 fC) is safe. On the other hand, even a 1.8 fC threshold ensures essentially 100% efficiency, assuming a signal from a minimum of 200 μm of silicon (2.6 fC) and taking into account Landau fluctuations.

Given the 38 pF detector capacitance, about half of which is between strips, the input impedance of the preamplifier must not be more than about 5 kΩ in order to avoid unacceptable cross talk and loss of charge collection. That translates into a rise time of about 200 ns for the preamplifier output. The feedback capacitance was chosen to be 0.14 pF, which results in a reasonable gain requirement of about 20 for the second stage and a gain-bandwidth product requirement of about 230 MHz for the preamplifier. The latter was achieved with a dominant pole at 150 kHz and a transconductance, for the input transistor, of about 700 μS.

The input MOSFET is *p*-channel and has a length of 1.2 μm and a width of 2500 μm. Prior to the design, noise and transconductance measurements were made on transistors with a variety of lengths and widths. The minimum length of 0.8 μm was not chosen, due to excessive $1/f$ noise. With 50 μW of power budgeted for the input transistor, the transconductance measurements indicated that the 2500 μm width was near the optimum for the anticipated detector capacitance.

The preamplifier is composed of a folded cascode amplifier followed by a source follower output stage, as illustrated in Fig. 2. The folding of the cascode minimizes the power dissipation by allowing the input transistor to be biased with only 2 volts, while the remainder of the circuit is operated on a 5 volt supply. The input-transistor bias current is set by an external resistor.

The amplifier must operate asynchronously, so a continuous baseline restoration is necessary. The DC feedback

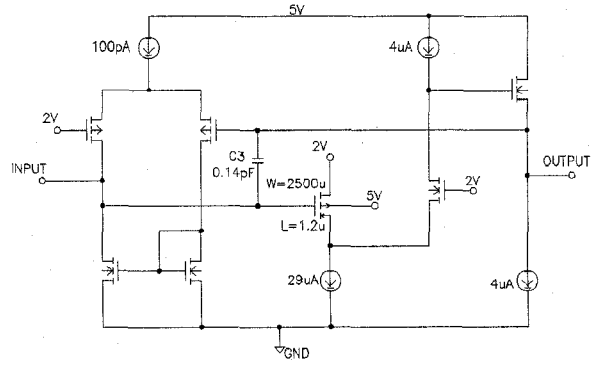

Figure 2. Preamplifier schematic.

network provides a current of up to about 100 pA to the input for that purpose. It operates in the same fashion as the shaping amplifier feedback described below. Simulations indicated potential problems with sensitivity of this small current to process variations. The current source was sized to stay well away from the extremes at which problems occur, and the results have been satisfactory in the three prototype runs made so far, with a typical time constant of 20 μs. The small current contributes negligible noise compared with the noise from the input transistor and the detector leakage current. Simulations predict that the total preamplifier noise is 9% greater than the noise due to the input transistor alone, with the second largest contributor being the current source for the input transistor.

The preamplifier is AC coupled to the shaping amplifier, which is a cascode amplifier with a source-follower output stage, as illustrated in Fig. 3. It has an 18 MHz gain-bandwidth-product with the principal pole at 20 kHz, which was adjusted to give a simulated rise time of about 1 μs.

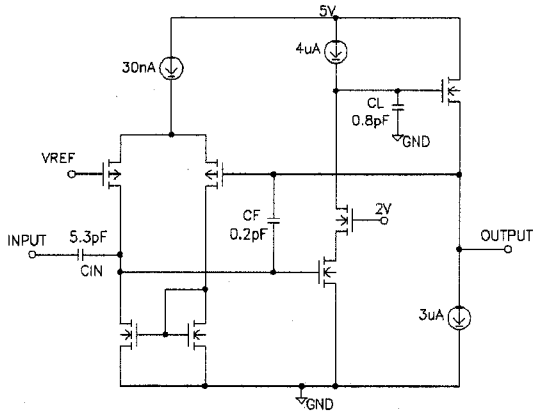

Figure 3. Shaping amplifier schematic.

The feedback scheme is modeled on that used in previous chips, such as the Kipnis-Zimmermann design for the SVX-II preamplifier [5]. The differential amplifier serves to adjust the bias point of the input transistor such that the output baseline (which is the comparator input) is fixed at the reference voltage. Transistor mismatch in this amplifier is the main contributor to the threshold dispersion, with it being most sensitive to the current-mirror load transistors. The low current density in the feedback circuit makes the matching problematic. We chose the sizes to ensure an rms variation of less than 15 mV at the shaper output, using the measurements of Ref. [6] for guidance.

The DC feedback network also provides the differentiation function of the shaping amplifier. However, for input charges greater than about 1 fC the baseline restoration tends to be current limited, rather than having the exponential decay that would be characteristic of a linear network. Therefore, the output looks like the result of a true RC/CR filter only for small pulse heights.

The shaper is DC coupled to the comparator, which is a conventional two-stage design—a differential amplifier followed by an inverting amplifier. The tail current of the first stage is about 3 μA. Judging from the data of Ref. [6], the contribution to the threshold dispersion from the transistor pairs in the comparator is negligible compared with that from the shaper feedback network.

The chips were fabricated in the Hewlett-Packard CMOS26G process (0.8 μm minimum feature size and 3 levels of metal interconnect) via the MOSIS VLSI fabrication service [7]. This process has no provision for making good linear capacitors, so with the exception of the calibration capacitors, MOSFET gates were used to implement the capacitors in the design. That works well as long as the bias potential across the capacitor is kept larger than a few tenths of a volt.

IV. Amplifier Performance

For the measurements presented here, the bias current of the input transistor was set to 21 μA. The signals at the output of the shaping amplifier, observed via internal probe pads, had a peaking time of 1.6 μs in the 16-channel chip, which was deliberately reduced to about 1.3 μs in the 32-channel version. The overall gain is 115 mV/fC in the 32-channel chip, which is close to the desired value. The input impedance of the preamplifier was measured to be 5.8 kΩ, very close to the Spice prediction. Figure 4 shows some measurements of the shaping amplifier output waveform with no load on the preamplifier input. With the input bonded to a 38 pF capacitor the peaking time increases by about 20%. However, we are not able to make a reliable measurement of the pulse shape in that condition, due to coupling between the probe tip and the nearby bond wire. Figure 4 illustrates the effect of the nonlinearity in the shaper feedback network. The peaking and zero-crossing times increase significantly with large signals.

The power consumption was measured to be 140 μW per channel in the 32-channel chip, including the bias circuitry (which is common to all channels). The noise was measured both by integrating the power spectrum (obtained by connecting a spectrum analyzer to the shaping amplifier output via a probe) and by measuring threshold curves. In the latter case the threshold was held constant while the input calibration charge was varied. A plot of efficiency versus input charge yielded an error function, for which the rms noise was the width σ. In addition, the noise was measured both with capacitors attached to the inputs and with actual silicon-strip detectors attached. All measurements gave consistent results. The data taken for the 16-channel chip with external capacitors fit well to a straight line: ENC=174 + 32×C electrons, with C in pF.

For the GLAST tracker, we plan to gang sets of 5 6.4 cm square detectors together in series to give strips that are effectively 32 cm in length, with a total capacitance of about 38 pF per strip. Measurements made on a beam-test module with 5 detectors in series gave a noise of 1600 electrons, which is reasonably consistent with the measurements on the 16-channel chip, when the difference in peaking time is taken into account.

A 16-channel chip connected to a single detector showed an rms threshold variation across its 16 channels of 6.5 mV, or

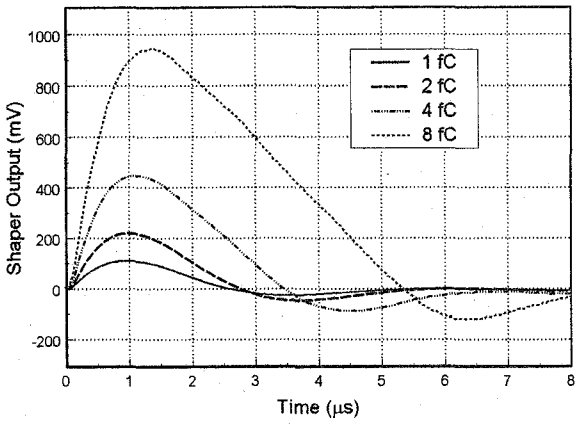

Figure 4. Measurements of the shaping amplifier output waveform for four values of injected charge. There was no load on the preamplifier inputs. The measurements were made by probing an internal pad of the 32-channel chip.

325 electrons ENC. Similar threshold scans made on all channels of 59 32-channel chips, with no detectors connected, gave a 6 mV variation per chip on average, but with a few chips showing variations as large as 16 mV rms. The 32-channel chips used in the beam test were arranged in 6 identical modules, with 12 chips per module (except for a single module with one dead chip). The threshold variation across any set of six chips located in identical positions in the modules was always consistent with the channel-to-channel variation within single chips. However, the variation across the 12 chips of a single module was significantly larger and systematic, which we now understand to be due to problems with the module design. In the final GLAST instrument, the thresholds will be set separately on each readout chip, using internal DACs, so that chip-to-chip variations may be removed, if necessary.

The shaping amplifier output saturates for input charges greater than about 20 fC, or 4 minimum ionizing particles at normal incidence. Nevertheless, the output still recovers gracefully at a rate dictated by the 30 nA current source in the feedback network. Except for input charges less than about 1 fC, the time-over-threshold of the shaping amplifier output is approximately a linear function of the input charge. The slope is approximately 1 μs/fC. We plan to take advantage of this feature by digitizing the time-over-threshold of the fast-OR output of each detector plane (not the individual channels) to obtain some information on the level of ionization. That will enhance the gamma-ray background rejection and may also be of interest for studies in cosmic-ray physics.

V. Digital Readout

The chips fabricated so far for this project include only enough digital logic to facilitate bench testing and operation in the test beam. However, we are now building a full prototype tower of the GLAST instrument that requires electronics meeting the full set of specifications. A 64-channel readout chip with 195 μm channel pitch has been designed but not yet tested.

The complete design incorporates the amplifiers and discriminators described in this paper. In addition, it has an 8-event-deep FIFO buffer, 7-bit DACs for both the threshold level and the calibration level, a 64-bit calibration mask, to allow calibration of any subset of channels, and separate masks for the fast-OR output and the data. It is controlled via dual redundant serial command decoders, and the output shift register and fast-OR are doubled for redundancy (the chip can pass data and trigger signals to either the left or the right). Finally, all external signals are transmitted via low-voltage-swing differential lines.

VI. Conclusion

Using conventional technology and standard CMOS design techniques, we have developed and tested an amplifier-discriminator chip that meets the power, noise, and threshold-stability requirements of the GLAST silicon-strip tracker. Fifty-nine of those chips, with a total of 1888 channels, recently operated successfully in a test beam over a period of one month without developing any problems.

The present design consumes less than 150 μW per channel, leaving sufficient power in the budget for the remaining digital processing and data transmission that will be needed in the full-scale GLAST tracker. The noise level and threshold variation are small enough that we can confidently anticipate achieving essentially 100% detection efficiency for minimum ionizing particles passing through live detector regions, while still maintaining an acceptable noise occupancy level of 0.01% or less.

VII. Acknowledgements

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