Tracking Detector Material Issues for the sLHC

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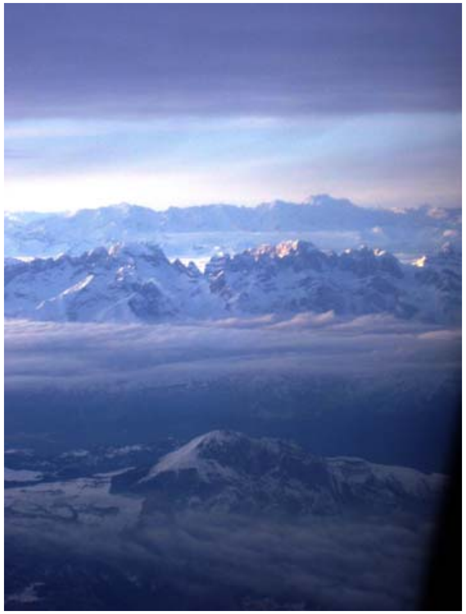
Outline of the talk

- Motivation for R&D in new Detector Materials
- Radiation Damage
- Initial Results with p-type Detectors
- Expected Performance
- R&D Plan

- Much of the data from RD50 http://rd50.web.cern.ch/rd50/
- In collaboration with Mara Bruzzi and Abe Seiden



- Presumably this is relevant for both strips and pixels
- Will not discuss 3-D detectors here

Announcement:
2nd Trento Workshop on Advanced Detector Design
(focus on 3-D and p-type SSD)
Feb 15. –16. 2006

Motivation for R&D in New Detector Materials

- The search for a substitute for silicon detectors (SSD) has come up empty.
- Radiation damage in SSDs impacts the cost and operation of the tracker.

- What is wrong with using the p-on-n SSD a la SCT in the upgrade?
    - Type inversion requires full depletion of the detector
    - Anti-annealing of depletion voltage constrains thermal management
    - Large depletion voltages require high voltage operation
    - Slower collection of holes wrt to electrons increases trapping

- What is wrong with using the n-on-n SSD a la ATLAS pixels in the upgrade?
    - Cost: double-sided processing about 2x more expensive
    - Type inversion changes location of junction
      (but permits under-depleted operation)
    - Strip isolation challenging, interstrip capacitance higher?

-Potential solution: SSD on p-type wafers (“poor man’s n-on-n”)
    - Single-sided processing, no change of junction
    - Strip isolation problems still persist

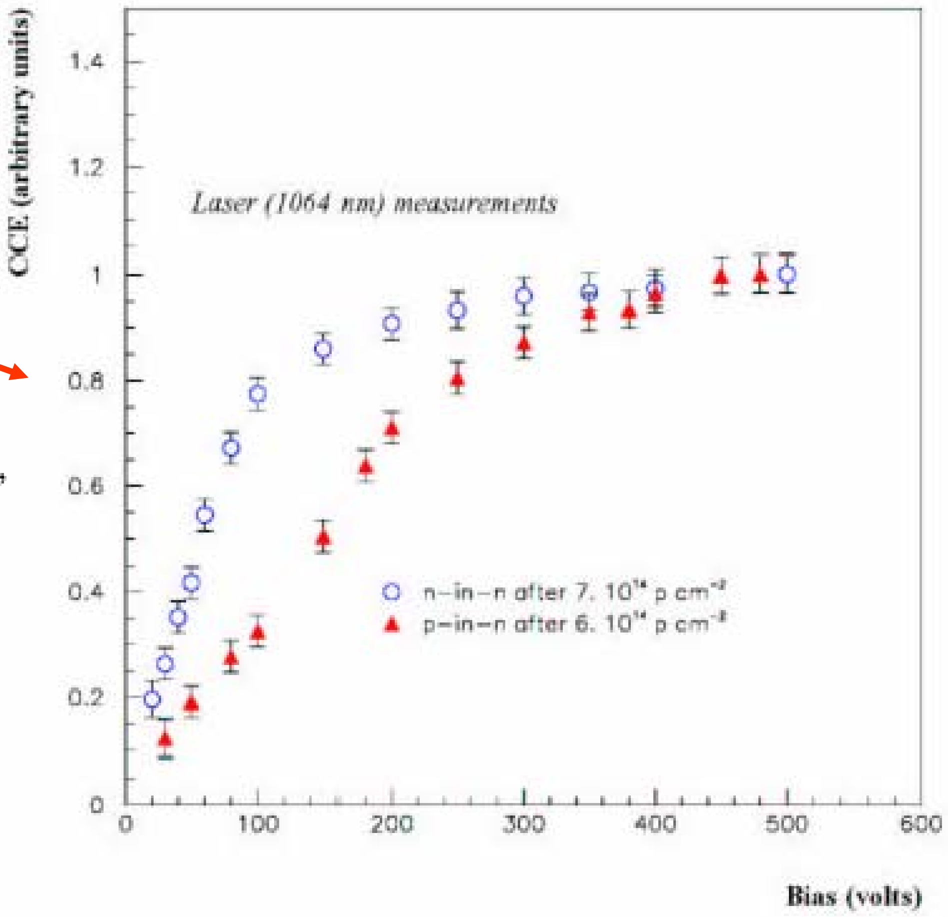
- Need to change the wafer properties to reduce the large depletion voltages: MCz

Charge collection efficiency CCE on n-side

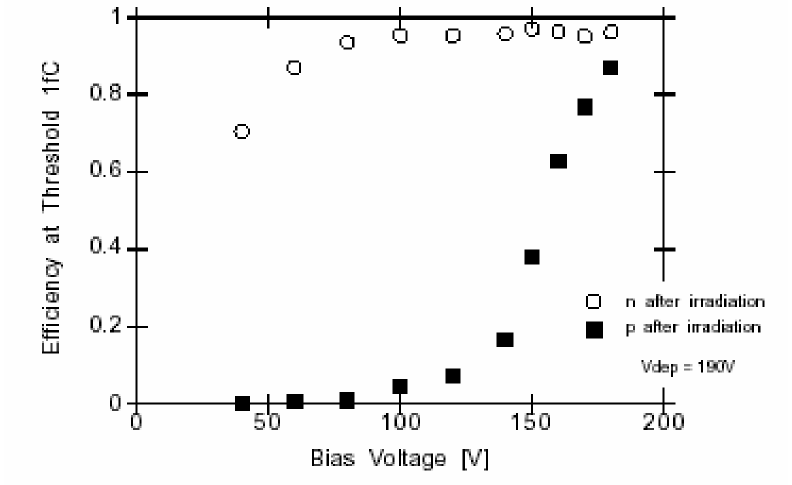
G. Casse, 1st RD50 Workshop, 2-4 Oct. 2002

n-side read-out after irradiation.

1060nm laser CCE(*V*) for the highest dose regions of an n-in-n (7.10^{14}p/cm^2) and p-in-n (6.10^{14}p/cm^2) irradiated LHC-b full-size prototype detector.



T. Dubbs *et al.*, *Nucl. Instr. Meth.* A383, 174 (1996),



Radiation Effects in Silicon Detectors

Basic effects are the same for n-type and p-type materials.

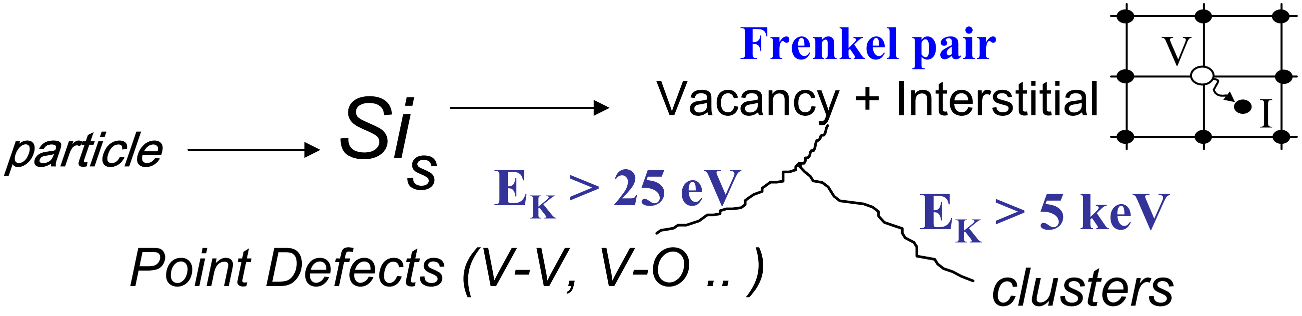
- Increase of the leakage current.
- Change in the effective doping concentration (increased depletion voltage),
- Shortening of the carrier lifetimes (trapping),
- Surface effects (interstrip capacitance and resistance).

The consequence for the detector properties seems to vary widely.

- An important effect in radiation damage is the annealing, which can change the detector properties after the end of radiation.
- The times characterizing annealing effects depend exponentially on the temperature, constraining the temperature of operating and maintaining the detectors.

- Fluence dependent effects normalized to equivqlent neutrons ("neq"), We use mostly proton damage constants and increase the fluence by 1/0.62.

Radiation Induced Microscopic Damage in Silicon



particle → Si_s → **Frenkel pair** Vacancy + Interstitial

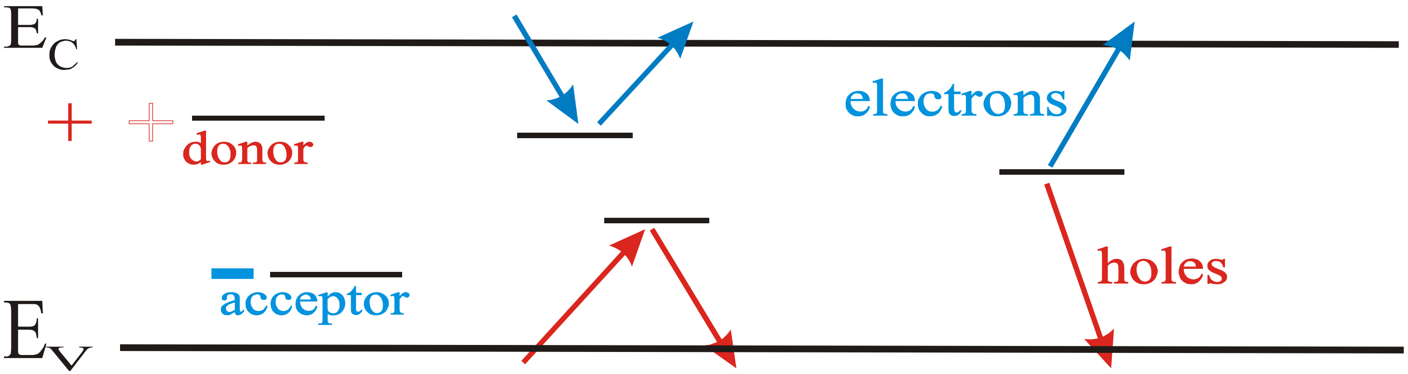
$E_K > 25$ eV

Point Defects (V-V, V-O ..)

$E_K > 5$ keV

clusters

Influence of defects on the material and device properties



charged defects

⇒ N_{eff} , V_{dep}

e.g. donors in upper and acceptors in lower half of band gap

Trapping (e and h)

⇒ CCE

shallow defects do not contribute at room temperature due to fast detrapping

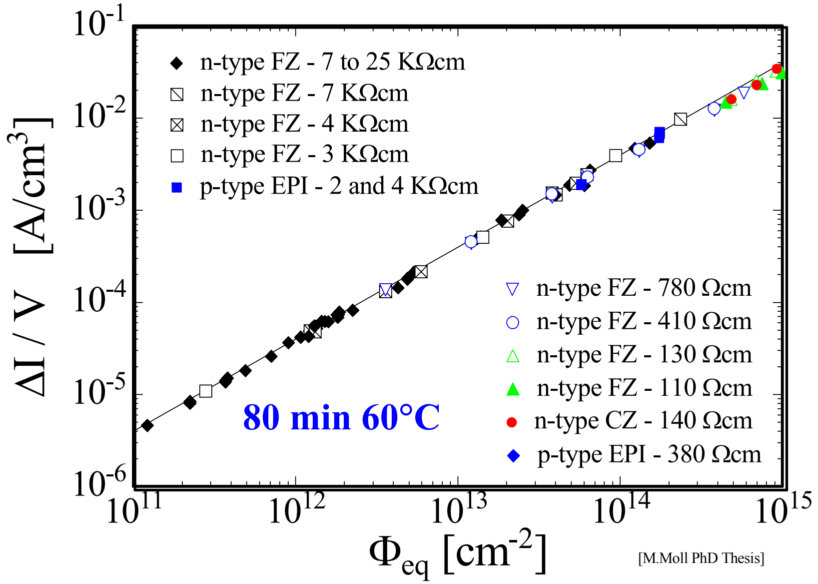
generation

⇒ leakage current

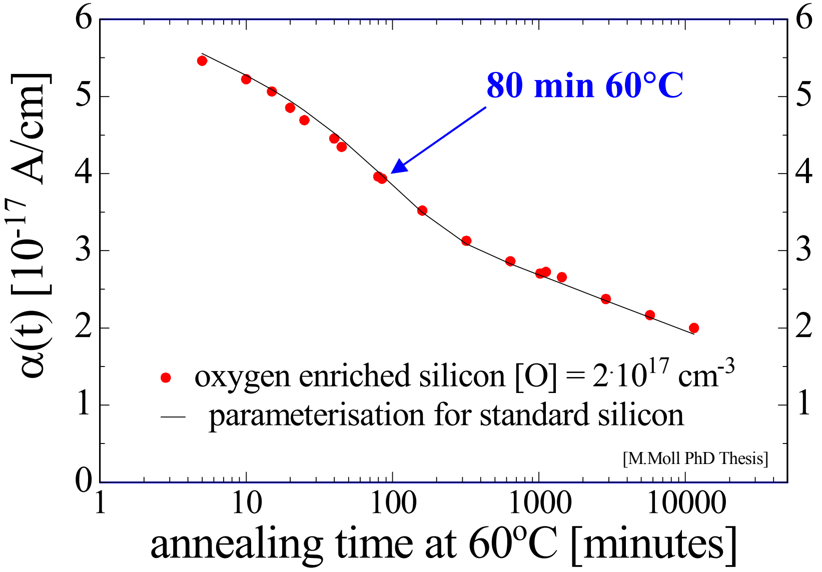
Levels close to midgap most effective

Leakage Current

Hadron irradiation



Annealing



M. Moll, Thesis, 1999

- **Damage parameter α (slope)**

$$\boxed{\alpha = \frac{\Delta I}{V \cdot \Phi_{eq}}}$$

- **α independent of Φ_{eq} and impurities**
  - ⇨ **used for fluence calibration (NIEL-Hypothesis)**

- **Oxygen enriched and standard silicon show same annealing**
- **Same curve after proton and neutron irradiation**

V_{dep} and N_{eff} depend on storage time and temperature

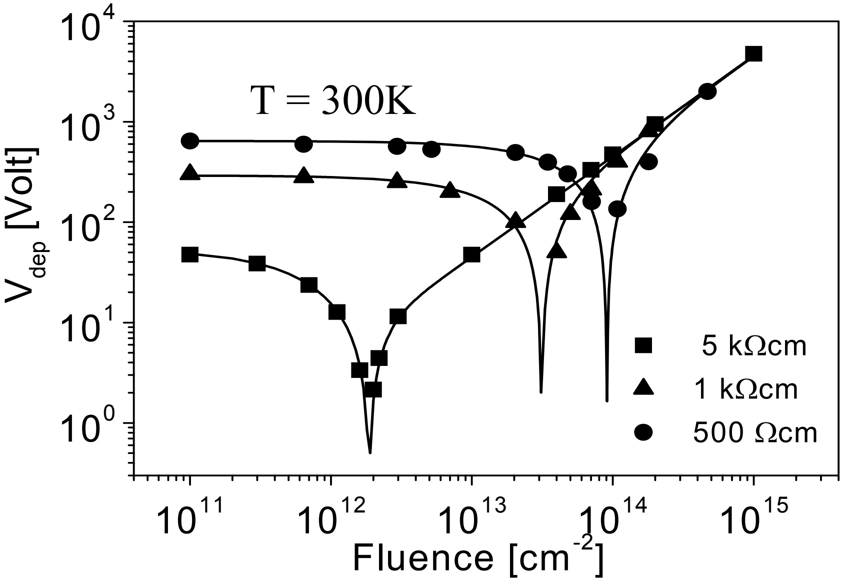
Stable Damage

$$\Delta N_{eff} = N_{C0}(1-e^{-c\cdot\phi}) + [g_c + g_a e^{-\frac{t}{\tau_a(T)}} + g_y(1-e^{-\frac{t}{\tau_y(T)}})]\phi$$

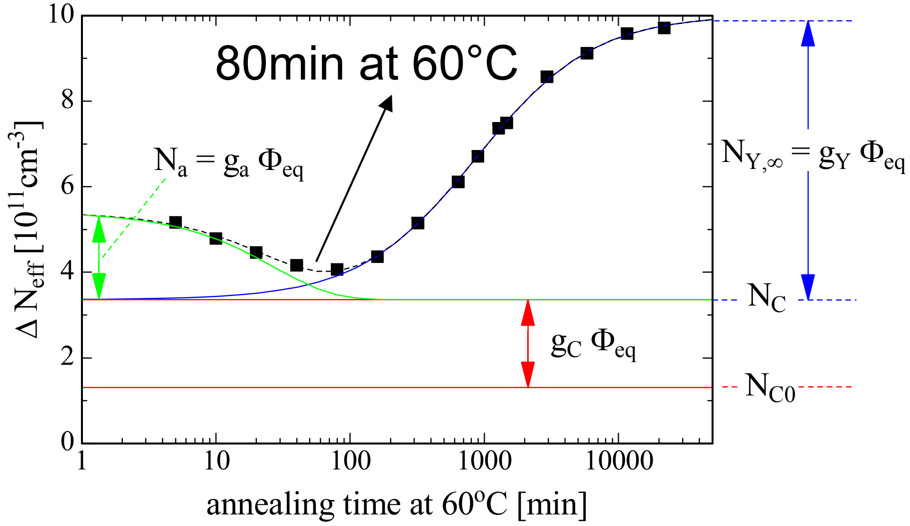
Beneficial Annealing

Reverse Annealing

ShallowDonor Removal



M. Bruzzi, Trans. Nucl. Sci. (2000)



G.Lindstroem et al, NIMA 426 (1999)

- **Short term: "Beneficial annealing"**
- **Long term: "Reverse annealing"**
  time constant : ~ 500 years (-10°C)
  ~ 500 days (20°C)
  ~ 21 hours (60°C)
  30min (80°C)

after inversion and annealing saturation $N_{eff} \sim \beta \cdot \phi$

Charge Collection Efficiency

Limited by:

- **Partial depletion**
- **Trapping at deep levels**
- **Type inversion (SCSI)**

Collected Charge:

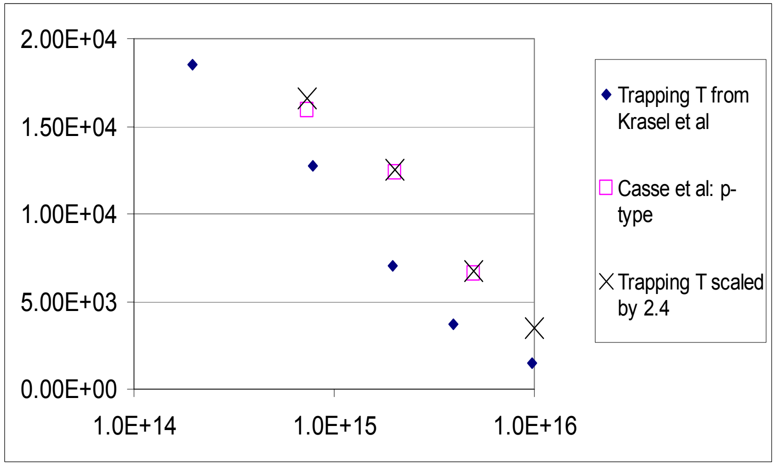
$$Q = Q_o \cdot \varepsilon_{dep} \cdot \varepsilon_{trap}$$

$$\varepsilon_{dep} = \frac{d}{W}$$

$$\varepsilon_{trap} = e^{-\frac{\tau_c}{\tau_t}}$$

W: Detector thickness
d: Active thickness
τ_c : Collection time
τ_t : Trapping time

$$\mathbf{1/\tau_{e,h} = \beta_{e,h} \cdot \Phi_{eq} [cm^{-2}]}$$



From TCT measurements within RD50:

$\tau_t \sim \mathbf{0.2}{*}10^{16} / \Phi$, $\tau_t \sim$ **0.2 ns for** $\Phi = 10^{16}$ **cm^{-2}**

Luckily this is excludedby CCE measurements:

→ $\tau_t \sim \mathbf{0.48}{*}10^{16} / \Phi$

Fluence Φ [neq/cm²]	$3\cdot10^{14}$	$5\cdot10^{14}$	$1\cdot10^{15}$	$3\cdot10^{15}$
Trapping time [ns]	16	9.6	4.8	1.6

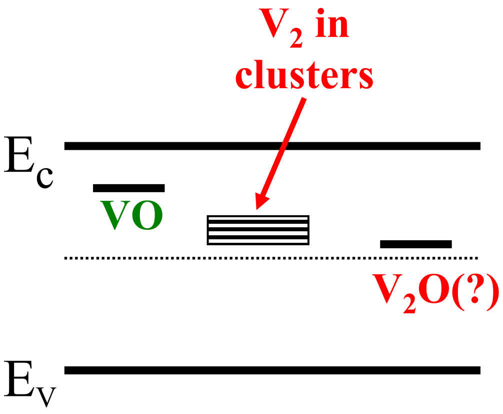
Defect Engineering of Silicon

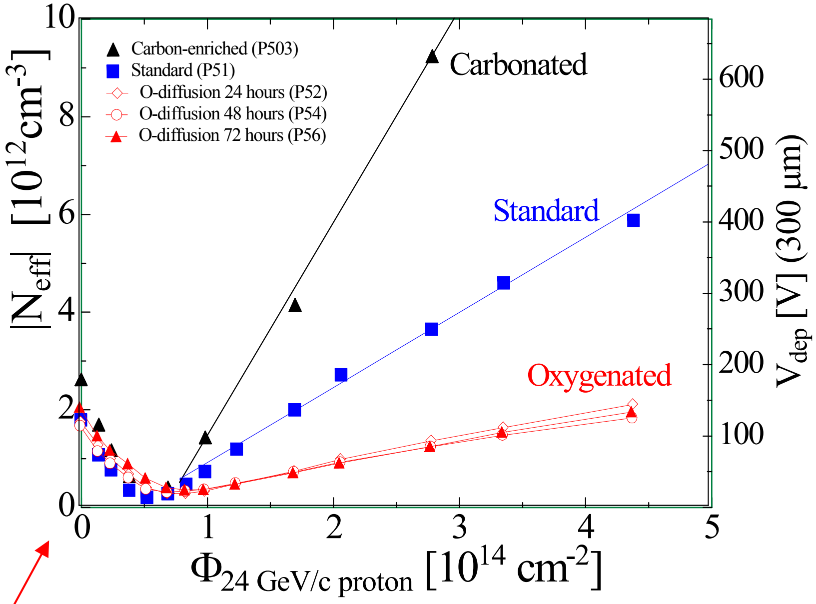
Influence the defect kinetics by incorporation of impurities or defects: Oxygen

Initial idea: **Incorporate Oxygen to getter radiation-induced vacancies**
⇒ prevent formation of Di-vacancy (V_2) related deep acceptor levels

•Higher oxygen content ⇒ less negative space charge
One possible mechanism: V_2O is a deep acceptor

V → O → VO (not harmful at RT)
V → VO → V_2O (negative space charge)

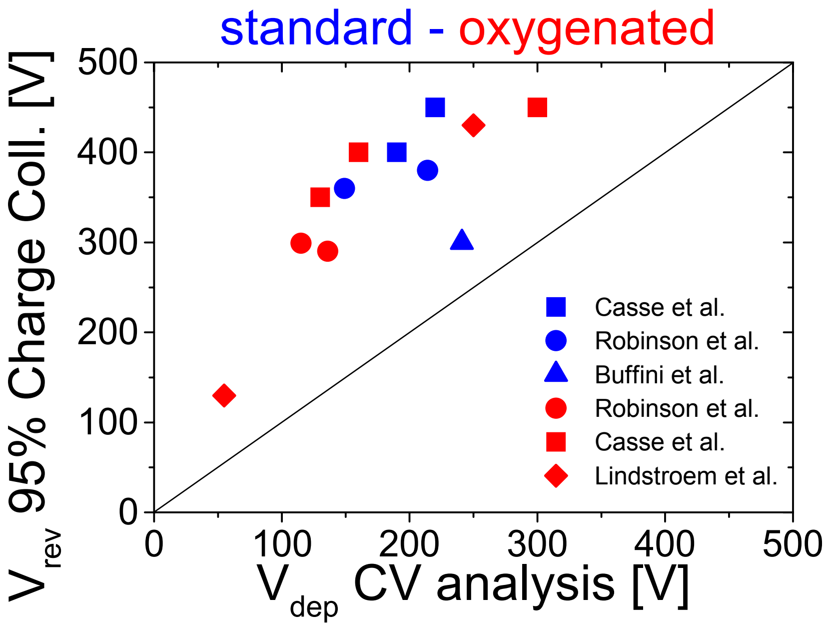




DOFZ (Diffusion Oxygenated Float Zone Silicon) RD48 NIM A465 (2001) 60

Caveat with n-type DOFZ Silicon

Discrepancy between CCE and CV analysis observed in n-type (diodes / SSD, ATLAS / CMS, DOFZ / Standard FZ)



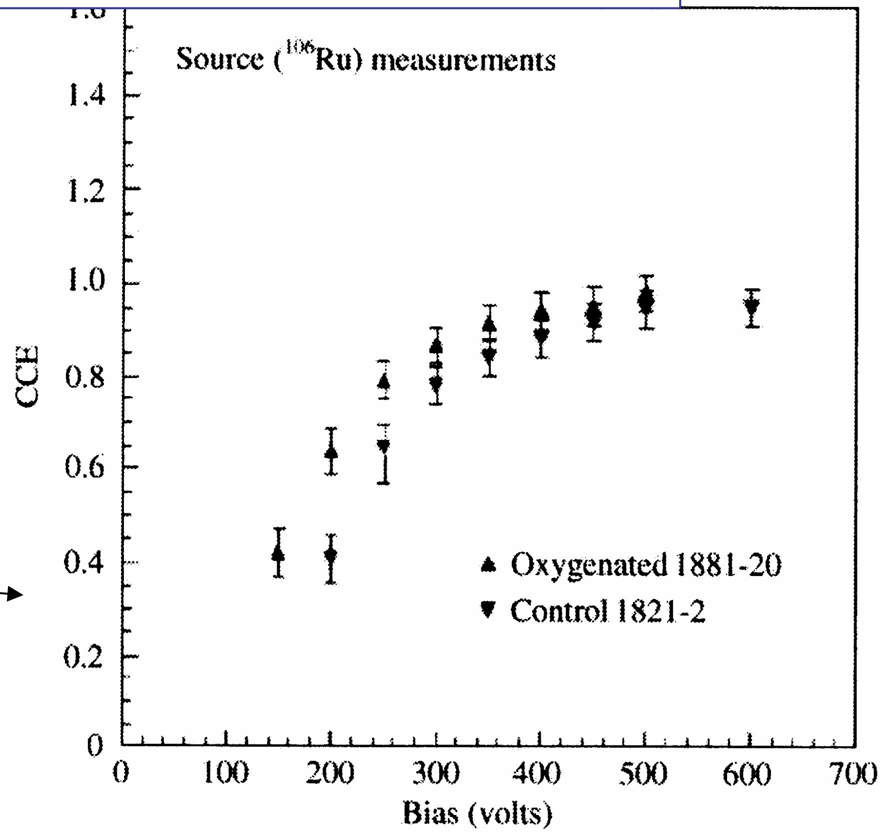
	Author	radiation	Exp.	material
●	Robinson et al., NIM A 461 (2001)	$3\text{x}10^{14}$ 24GeV p/cm^2	ATLAS	Oxygen. + standard
■	Casse et al., NIM A 466 (2001)	$3\text{-}4\text{x}10^{14}$ 24GeV p/cm^2	ATLAS	Oxygen. + standard
◆	Lindström et al., NIM A 466 (2001)	$1.65\text{x}10^{14}$ 24GeV p/cm^2	ROSE	Oxygen. <100>
▲	Buffini et al., NIM A (2001)	$1.1\text{x}10^{14}$ 1MeV n/cm^2	CMS	Standard <111>

To maximise CCE it is necessary to overdeplete the detector up to :

$$V_{bias} \sim 2\ V_{dep}$$

Caveat:
The beneficial effect of oxygen in proton irradiated silicon microstrip almost disappear in CCE measurements

G.Casse et al. NIM A 466 (2001) 335-344



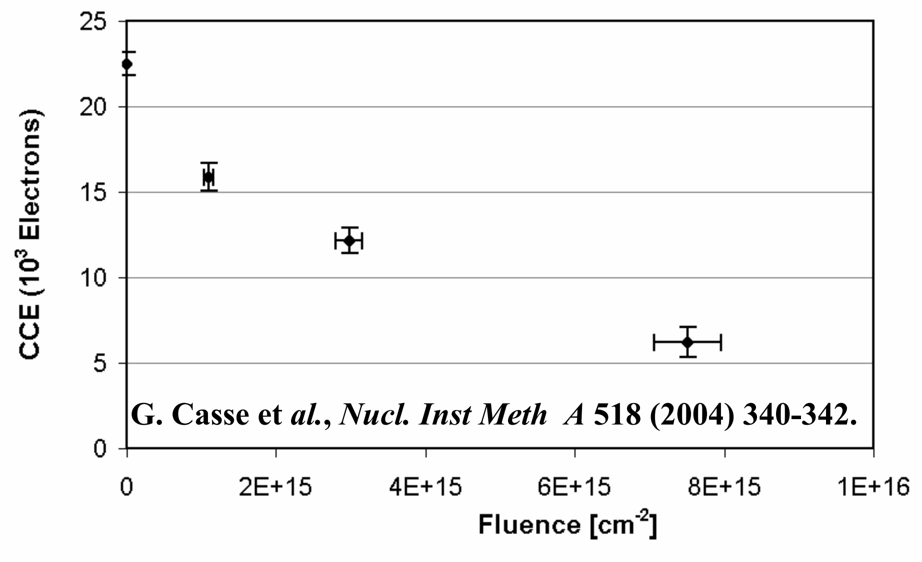
ATLAS microstrip CCE analysis after irradiation with $3\mathrm{x}10^{14}$ p/cm^{2}

CCE n-in-p microstrip detectors

- **Miniature n-in-p microstrip detectors (280µm thick) produced by CNM-Barcelona using a mask-set designed by the University of Liverpool.**
- **Detectors read-out with a SCT128A LHC speed (40MHz) chip**
- **Material: standard p-type and oxygenated (DOFZ) p-type**
- **Irradiation: 24GeV protons up to 3 10^{15} p cm^{-2} (standard) and 7.5 10^{15} p cm^{-2} (oxygenated)**

CCE ~ 60% after 3 10^{15} p cm^{-2} at 900V(standard p-type)

CCE ~ 30% after 7.5 10^{15} p cm^{-2} 900V (oxygenated p-type)



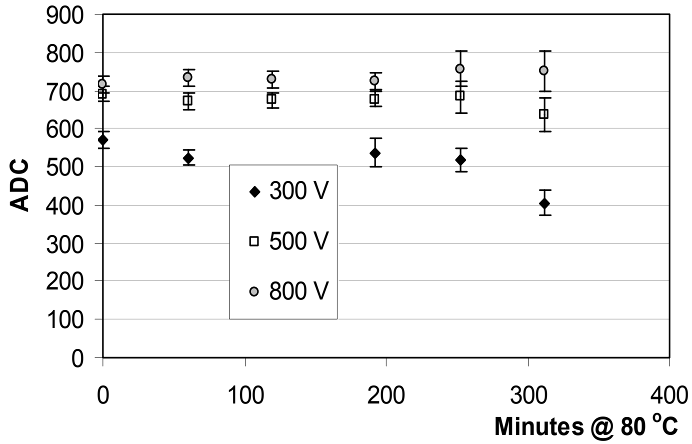
G. Casse et *al.*, *Nucl. Inst Meth A* 518 (2004) 340-342.

At the highest fluence Q~6500e at V_{bias}=900V. Corresponds to: ccd~90µm, trapping times 2.4 x larger than previously measured.

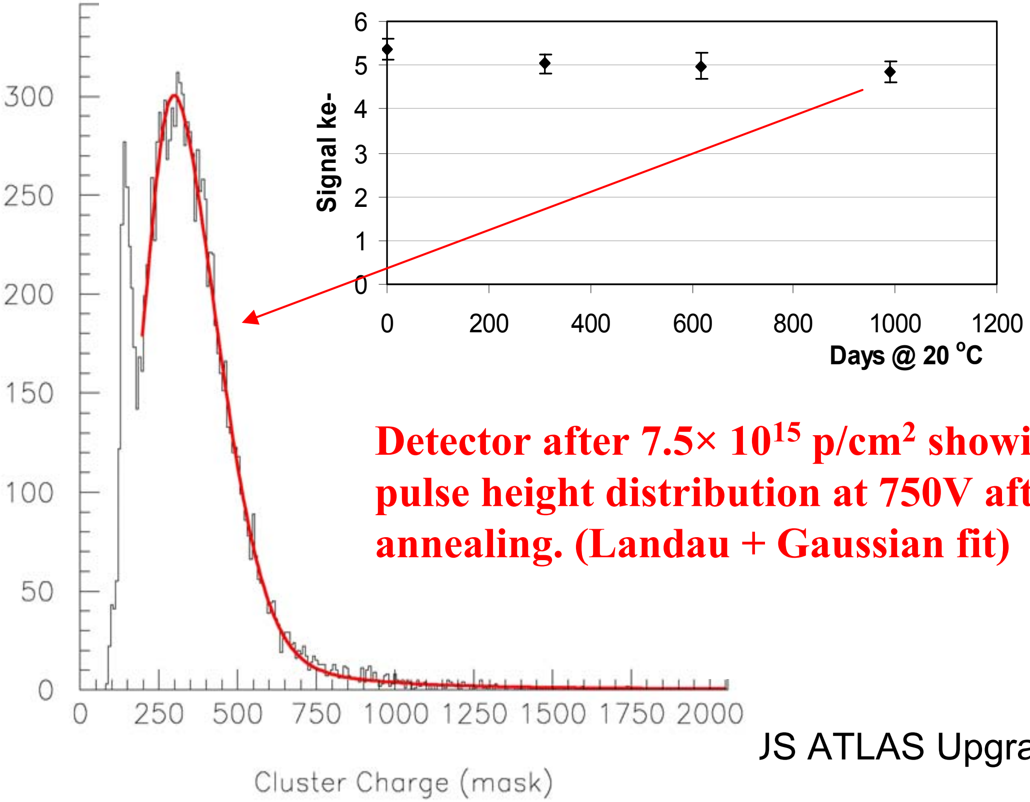
Recent n-in-p Results

Important to check that there are no unpleasant surprises during annealing.

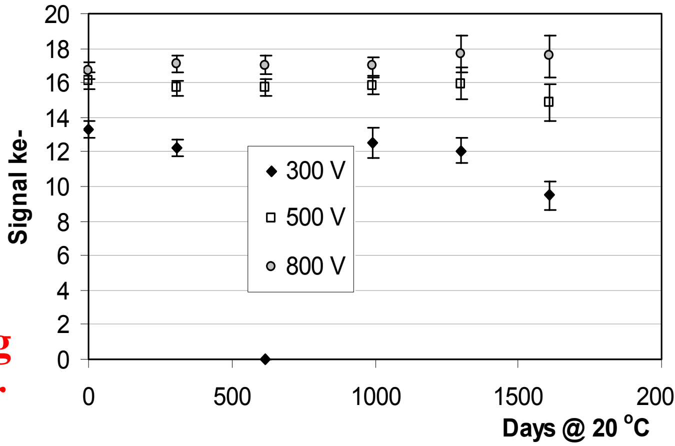
Minutes at 80°C converted to days at 20°C using acceleration factor of 7430 (M. Moll).



G. Casse et *al*., 6th RD50 Workshop, Helsinki June 2-4 2005 http://rd50.web.cern.ch/rd50/6th-workshop/.



Detector after 7.5× 10^{15} p/cm^2 showing pulse height distribution at 750V after annealing. (Landau + Gaussian fit)



Detector with 1.1× 10^{15} p/cm^2

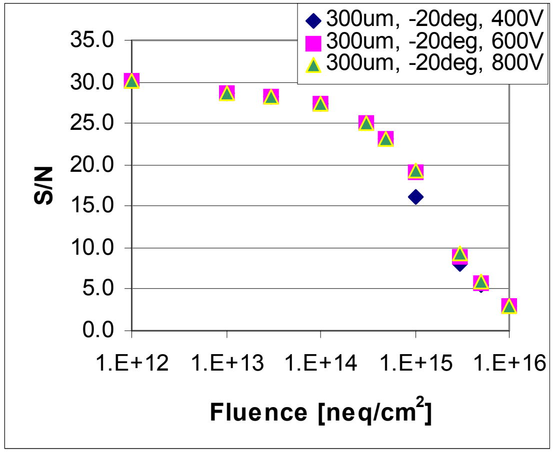
Expected Performance for p-type SSD

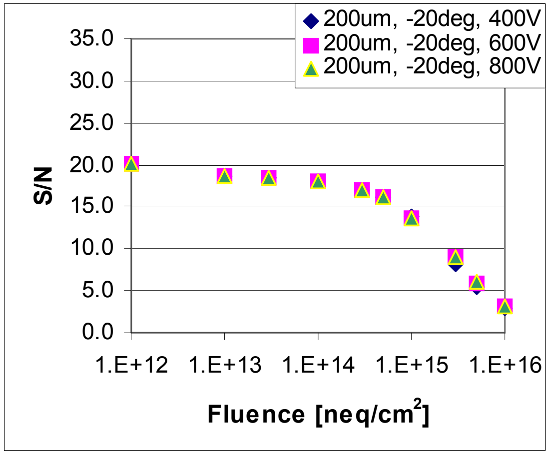
Details in : “Operation of Short-Strip Silicon Detectors based on p-type Wafers in the ATLAS Upgrade ID
M. Bruzzi, H.F.-W. Sadrozinski, A. Seiden, SCIPP 05/09

Conservative Assumptions:

$\alpha_p = 2.5\cdot10^{-17}$ A/cm (only partial anneal)
$C_{total} = 2$ pF/cm
$V_{dep} = 160V + \beta*\Phi$ (with $2.7*10^{-13}$ V/cm^2) (no anneal)
(= 600V @ $\Phi = 10^{16}$ neq/ cm^2)
$\sigma^2_{Noise} = (A + B\cdot C)^2 + (2\cdot I\cdot\tau_s)/q$ A = 500, B = 60

S/N for Short Strips for different bias voltages:





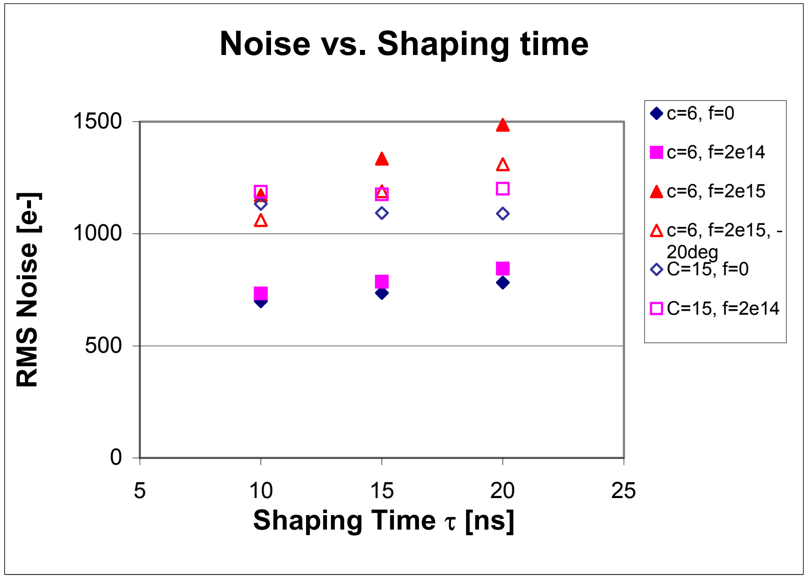
no need for thin detectors, unless n-type: depletion vs. trapping 600V seems to be sufficient

Expected Performance for p-type SSD, cont.

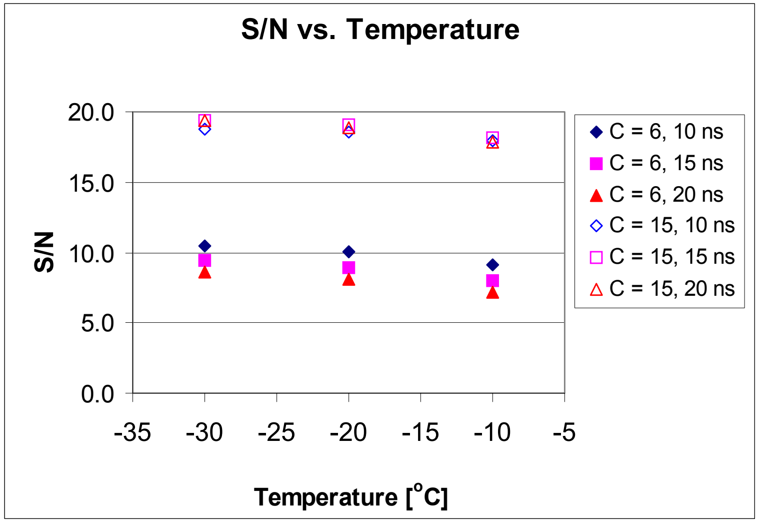
Noise for SiGe Frontend
(see talk by Alex Grillo)

Leakage current important:
Trade shaping time against operating temperature
(20 ns & -20 °C vs. 10 ns & -10 °C)

Temperature:
-10 deg C



Fluence:
$2.2\cdot10^{15}$ neq/cm^2 (short strips) $2.2\cdot10^{14}$ neq/cm^2 (long strips)
The maximum bias voltage is 600 V



Expected Performance for p-type SSD, cont.

Heat Generation in 300 µm SSD

$$I(T) = I(T_0)\left(\frac{T}{T_0}\right)^2 \exp(\frac{E_b}{2K}\left(\frac{1}{T_0} - \frac{1}{T_0}\right))$$

Temperature [^{o}C]	20	0	-10	-20	-30
α(T)/ α(20)	1	0.197	0.0797	0.0300	0.0104

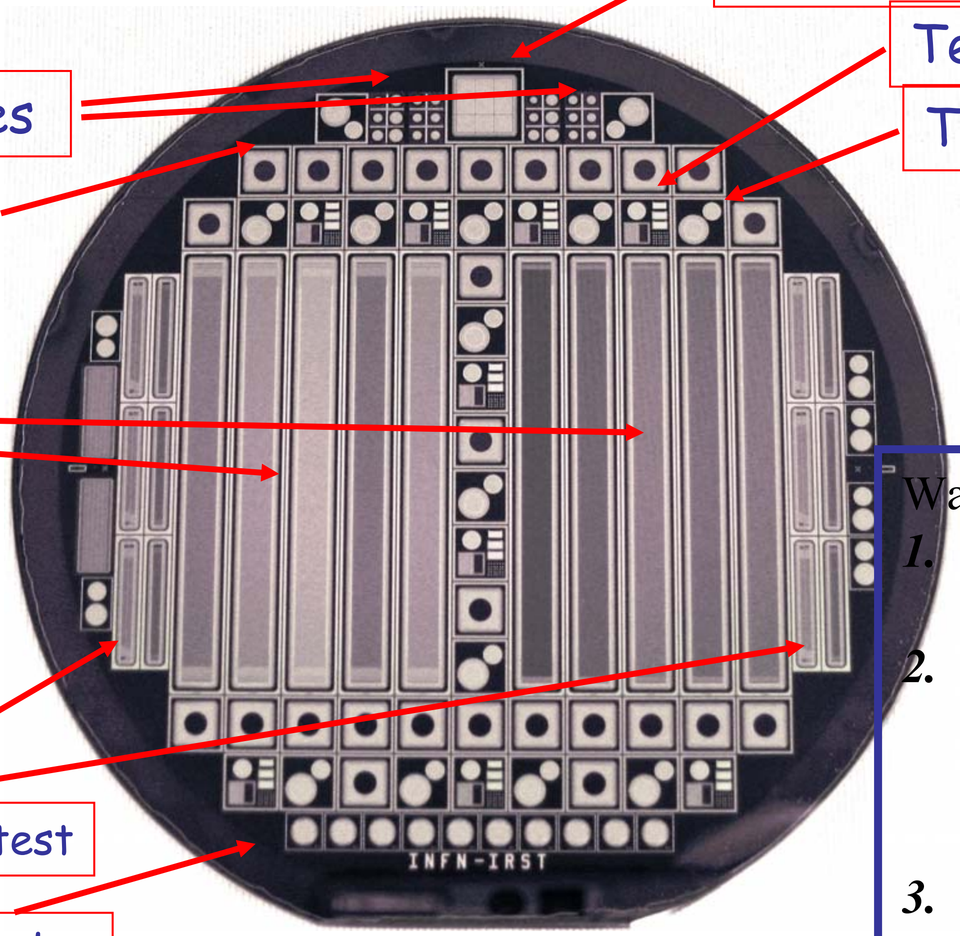
Only from active volume

$$\frac{I}{Volume} = \alpha \cdot \Phi$$

			Generated Heat Flux [W/cm^2]			
Φ neq	Vbias [V]	w [µm]	T = 20°C	T=-10°C	T=-20°C	T=-30°C
3E+14	290	300	1.05E-01	6.75E-03	2.35E-03	7.54E-04
5E+14	376	300	2.27E-01	1.46E-02	5.09E-03	1.63E-03
1E+15	400	247	3.98E-01	2.55E-02	8.90E-03	2.85E-03
1E+15	591	300	7.15E-01	4.59E-02	1.60E-02	5.13E-03
3E+15	400	157	7.62E-01	4.89E-02	1.70E-02	5.46E-03
3E+15	600	193	1.40E+00	8.99E-02	3.13E-02	1.00E-02
3E+15	800	223	2.16E+00	1.38E-01	4.82E-02	1.55E-02

An Italian network within RD50: INFN SMART

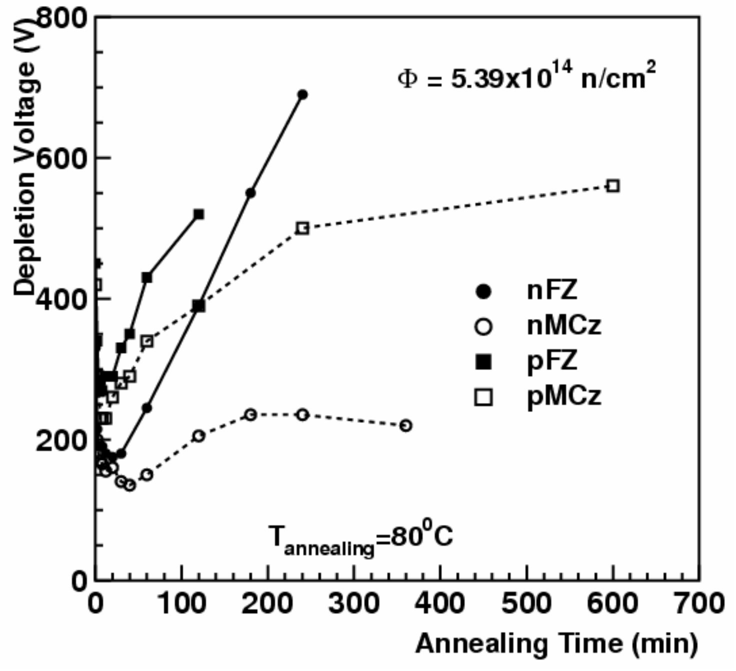
n-type and p-type detectors processed at IRST- Trento



Wafers Split in:

1. ***Materials***: **(Fz,MCz,Cz,EPI)**
2. ***Process***:
   - **Standard**
   - **Low T steps**
   - **T.D.K.**
3. ***Isolation***:
   - **Low Dose p-spray**
   - **High Dose p-spray**

SMART News: Annealing behaviour of MCz Si n- and p-type



G. Segneri et al. Submitted to NIM A, presented at PSD 7, Liverpool , Sept. 2005

V_{dep} variation with fluence (protons) and annealing time (C-V):

Beneficial annealing of the depletion voltage:

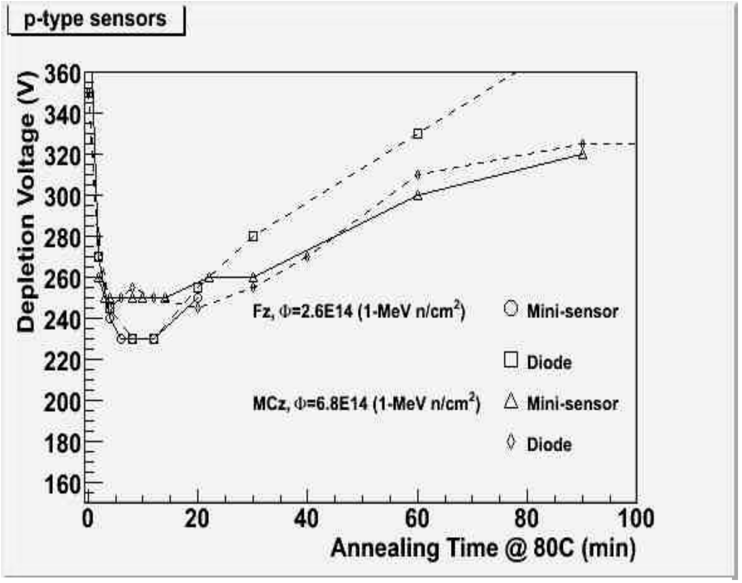
14 days at RT, 20 min at 60 °C. 3 min at 80 °C.

Reverse ("anti-") annealing starts

in p-type MCz: at 10 min at 80 °C , 250 min (=4 hrs) at 60 °C,
>> 20,000 min (14 days) at RT,

in p-type FZ : at 20 min at 60 °C

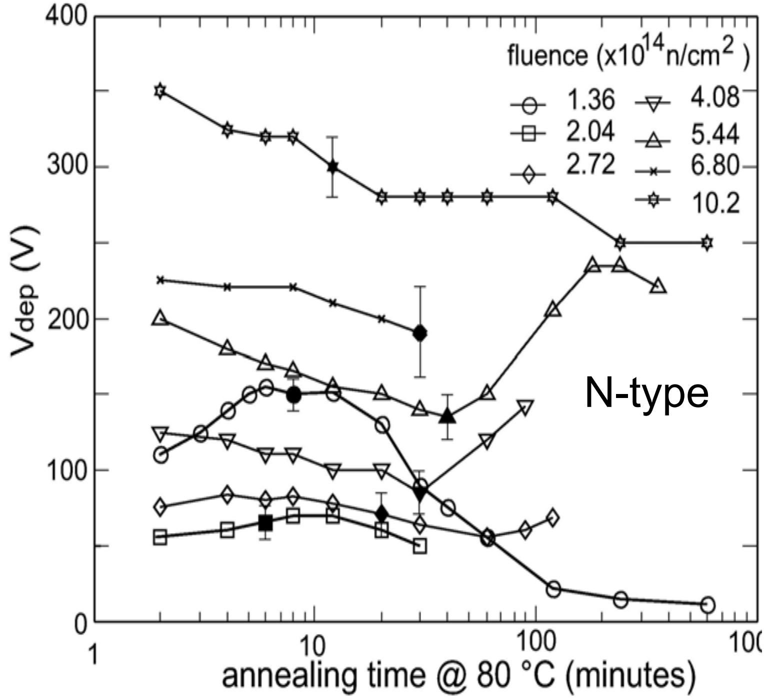
in n-type FZ: at 120 min at 60 °C.

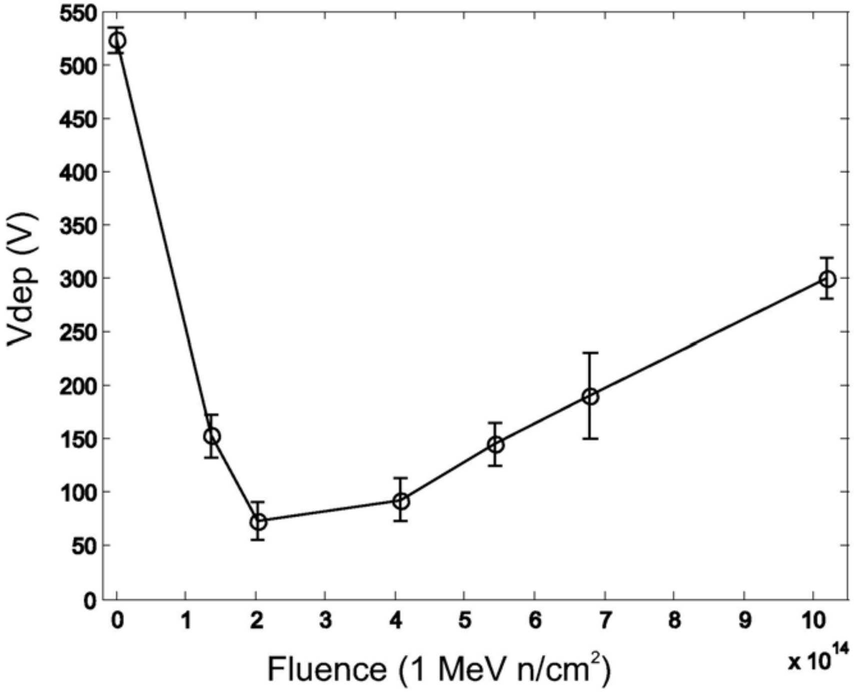


A. Macchiolo et al. Submitted to NIM A, presented at PSD 7, Liverpool , Sept. 2005

SMART News: Annealing behaviour of n- type MCz Si

(is n-type MCz inverted?)





M. Scaringella et al. presented at Large Scale Applications and Radiation Hardness Florence, Oct. 2005

A. Macchiolo et al. Submitted to NIM A, presented at PSD 7, Liverpool , Sept. 2005

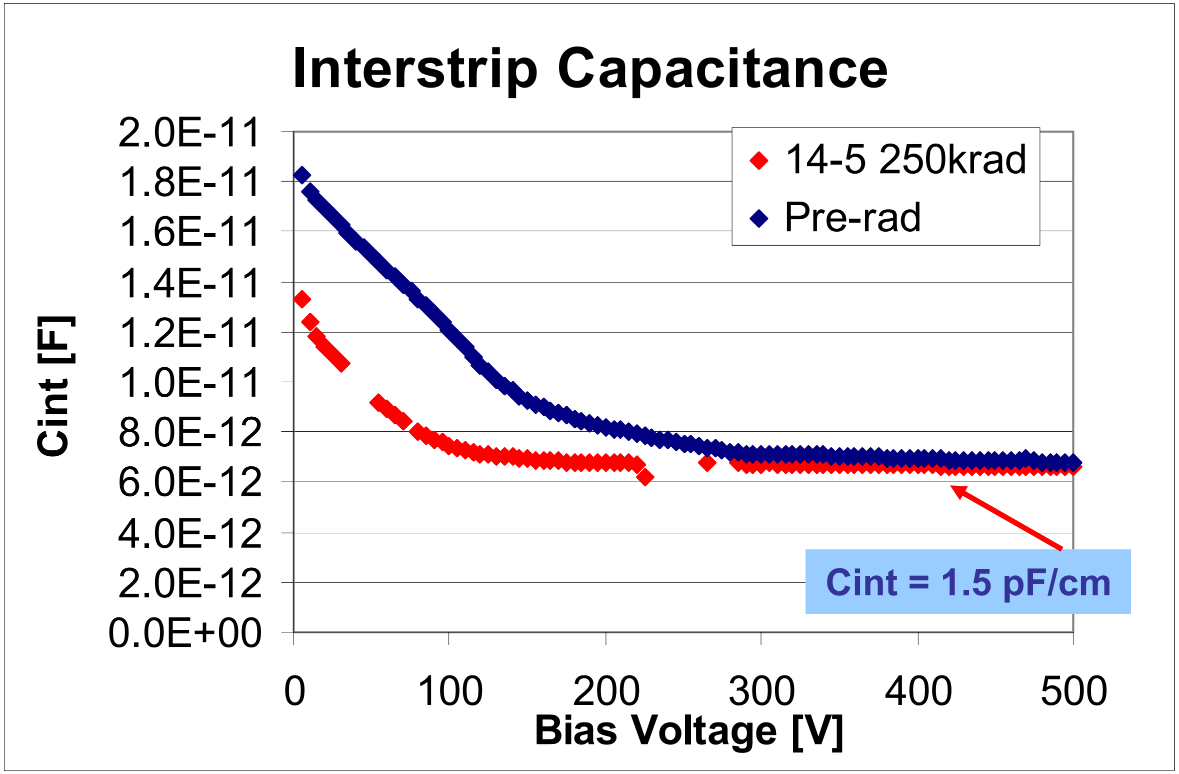
Inter-strip Capacitance

One of the most important sensor parameters contributing to the S/N ratio

Depends on the width/pitch ratio of the strips

and on the strip isolation technique (p-stops, p-spray).

Observe large bias dependence on p-type detectors, due to accumulation layer.



SMART 14-5
p-type FZ
low-dose spray
w/p = 15/50
V_{dep} = 85 V
(I. Henderson,
J. Wray,
D. Larson,
SCIPP)

Irradiation with ^{60}Co reduces
the bias dependence,
as expected.

Status

- Radiation hard materials for tracker detectors at SuperLHC are under study by the CERN RD50 collaboration. Fluence range to be covered with optimised S/N is in the range 10^{14}-10^{16}cm^{-2} . At fluences up to 10^{15}cm^{-2} (Mid and Outer layers of a SLHC detector) the change of the depletion voltage and the large area to be covered by detectors is the major problem.

- High resistivity MCz n-type and p-type Si are most promising materials.

- Quite encouragingly, **at higher fluences results seem better than first extrapolated from lower fluence**:

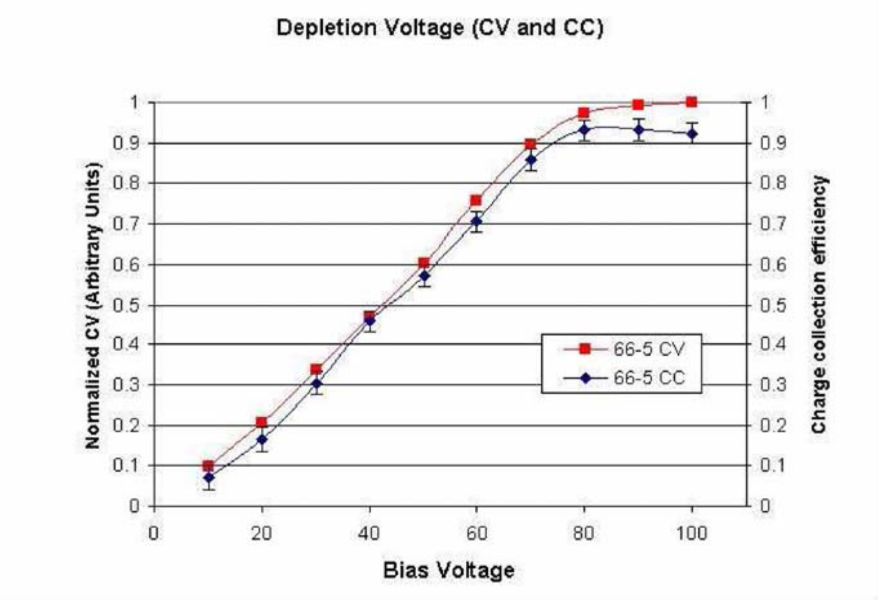
  longer trapping times (p-FZ, p-DOFZ)
  delayed and reduced reverse annealing (MCz SMART)
  sublinear growth of the V_{dep} with fluence (p - MCz&FZ)
  delayed/supressed type inversion (p- MCZ&FZ, MCz n- protons)

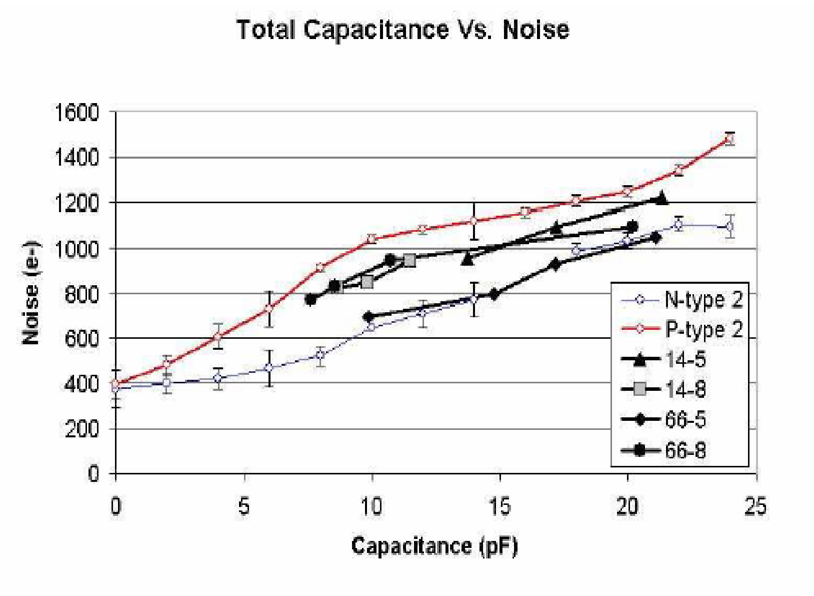
- The annealing behavior in both n- and p-type SSD needs to be verified with CCE measurements.

R&D Plan:

- Need to confirm findings of C-V measurements
- Fabricate SSD on MCz wafers, both p- and n-type.
- Optimize isolation on n-side.
- Measure charge collection efficiency (CCE) on SSD,
  pre-rad, post-rad, during anneal.
- Measure noise on SSD pre-rad, post-rad, during anneal.

Un-irradiated SMART SSD





R&D Plan

Submission of 6” fabrication run within RD50

Goals:

-a. P-type isolation study
-b. Geometry dependence
-c. Charge collection studies
-d. Noise studies
-e. System studies: cooling, high bias voltage operation,
-f. Different materials (MCz, FZ, DOFZ)
-g. Thickness

Wafer	bulk	#	Thickness [um]	SSD
MCz	p	7	300	n-on-p
DOFZ	p	5	300	n-on-p
FZ	p	5	300	n-on-p
MCz	n	3	300	p-on-n +n-on-n (no backside
Fz	n	2	300	p-on-n +n-on-n (no backside
MCz	n	3	200	p-on-n +n-on-n (no backside