ATLAS ID Upgrade R&D Plan: Development of a Short-Strip Silicon Detector Module and a Frontend Readout ASIC

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Summary:

We propose an R&D program that will contribute to the identification of the optimum technology and layout of the tracking detectors for the upgraded ATLAS ID. The goal of this program is to construct a short-strip silicon detector module with sufficient radiation hardness for the intermediate tracking region in the upgraded ATLAS ID. We anticipate that much of the work would then also be applicable to the tracking detectors at larger radii. There is already a vigorous program in place to search for sensor materials with sufficient radiation hardness. Our contribution will be to help to select the most promising materials, build a module with a silicon detector of the appropriate geometry and evaluate the charge collection efficiency and signal-to-noise performance before and after irradiation. We will start by using existing readout electronics, and then move to newer electronics as these are developed in parallel with the detector options. The readout electronics for this upgraded ATLAS ID requires selection of a successor to the biCMOS process used for the ATLAS strip detectors. A relatively new silicon-germanium (SiGe) biCMOS process appears to have advantages over straight CMOS and this will be evaluated with the help of a DoE Advanced Detector Research grant. Again, the goal is to have a front-end ASIC that meets the upgraded ID requirements. In addition, we will work on sensor and ID layout issues, and on the reduction of service and data lines.

We envision three phases for this work. The first, during FY05, 06, and 07 will involve initial tests and design. This will include measurements of radiation performance as well as finding limits to detector and electronics choices based on signal-to-noise and cost. The second, during FY08 and 09, will involve further development of the most promising choices for detector and readout, including realistic estimates of layout, material and cabling constraints. Work during this period can make use of the knowledge gained during initial LHC running to provide input from the technical performance of ATLAS as well as first physics results. The final period in FY10 will aim at resolving final R&D issues and preparing for a detector construction activity.

1. R&D Plan

1.1. Silicon Strip Detectors on p-type Substrate

The performance of detector material is constrained by the large particle fluences expected at the collider, leading to radiation damage. We are interested in particular to evaluate p-type substrates, which have been shown to yield adequate charge collection

after high fluences (see Fig.1), and have the added advantage of permitting under-depleted operation. But there is really little experience with silicon strip detectors fabricated on p-substrates.

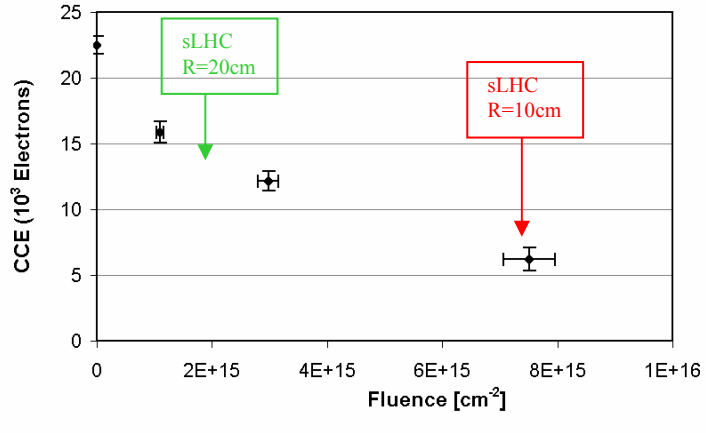


Fig.1 Charge collection efficiency of p-type test detectors as a function of fluence. The 5 year sLHC fluence is indicated (Data from G. Casse et al, VCI 2004)

There is only limited data on tracking efficiency for MIPs in irradiated p-type strip detectors. Much data has been accumulated with pad detectors and 5 MeV α particles, and in n-type materials. We propose to work on the evaluation of the charge collection efficiency and signal-to-noise performance of different silicon tracking detectors before and after irradiation, using particle telescopes and radioactive sources. (This would be in addition to the evaluation using standard electrical parametric tools.) This type of methodology has been very useful in the past in the development of the ATLAS SCT detectors, and can then be backed up by a much more elaborate beam test, once some of the choices are narrowed down.

The geometry of tracking detectors is constrained mainly by instantaneous particle rates, and in the intermediate tracking region between the radii of 20 cm and 50 cm, relatively short strips will be needed. There are several proposals how to arrange these, and we will work on single-sided strips of 3 cm length (Fig. 2), which give a resolution of about 1 cm along the strips, and can be arranged in small-stereo back-to-back fashion similar to the ATLAS SCT, if better resolution is needed. In addition, this geometry can directly be extended to longer strips and single coordinate measurements needed for the outer layers of the silicon tracker, where the hybrid could service pairs of much longer strips.

The first phase of the R&D program will proceed in the following way:

Year 1: In the first year, we will concentrate on evaluating the performance of small test detectors fabricated within the RD50 framework to confirm the data on charge collection and trapping in p-type and n-type substrates. We will use readout boards with low-noise electronics, which allows us to detect the expected small signals after irradiation.

Year 2: In the second year, we will produce short-strip silicon strip detectors in the

geometry appropriate for the intermediate region of the ATLAS upgrade ID, and construct single detector modules with fast low-noise readout. This will require new hybrids, which will be based on the successful ATLAS SCT hybrid design. The modules will also be a test bed for the ASICs based on SiGe technology (see Section 1.2)

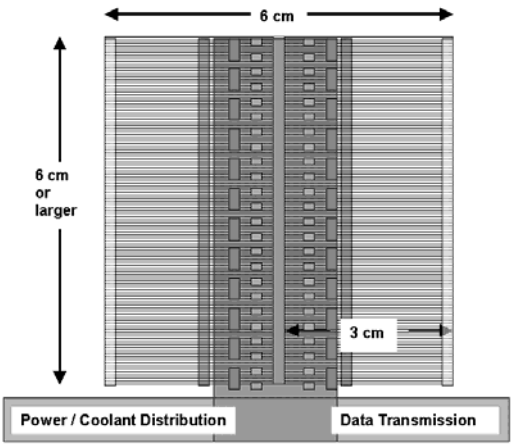
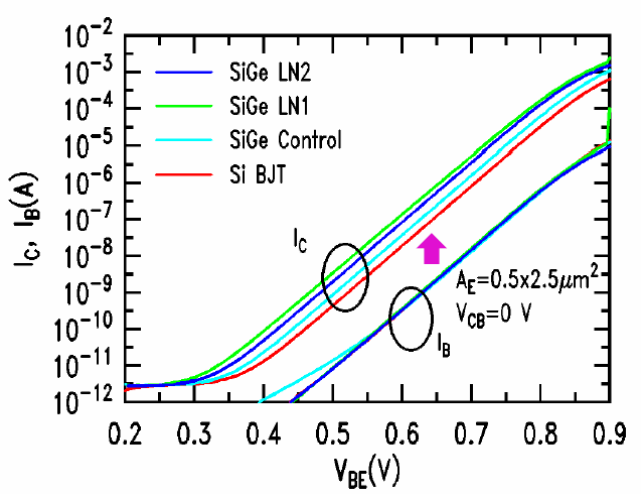


Fig.2 Single-sided short strip module of pairs of 3 cm long strips. The hybrid arrangement is similar to the ATLAS SCT modules.

We are planning to collaborate with US groups (BNL, Hawaii) and international partners on developing, irradiating and characterizing test structures and prototype detectors, and the design and fabrication of hybrids and readout DAQ. The UCSC work will be done under the supervision of Prof. H. Sadrozinski and a postdoc.

1.2. Readout ASICs in SiGe technology

We propose to investigate SiGe biCMOS processes for the readout of silicon strip detectors in the ATLAS upgrade ID. Two of these processes make use of the 0.25μm and 0.18μm CMOS processes that have already been used for readout in HEP detectors. Initial studies have convinced us that the SiGe bipolar process added to these CMOS processes offers many advantages in analog performance compared to a straight CMOS solution. The current gains are in excess of 300, about 3 times higher than older silicon (without Ge) processes (see Fig. 1, from J. Cressler's talk at 2003 Frontend Meeting in Snowmass). We have shown that a SiGe front-end has the potential for a factor of 3 to 4 in power savings. This would have a large impact for silicon trackers with large numbers of channels, and for individual long strip detectors. The SiGe processes have been tested up to fluences of 5×10^{13} cm^{-2} and show every indication of working at far higher fluences, but this needs to be verified. The other important aspect of the process that needs evaluation is transistor-to-transistor matching, which is very important for the application in a multi-channel ASIC. Our research plan aims to quantify these characteristics.



Fig, 3 Current – Voltage (I-V) characteristics of SiGe processes, indicating a current gain of about 350.

The work for the first two years of the program will break down in the following way:

Year 1: Design and fabrication of test structures and simple circuit elements, followed by testing of matching, radiation hardness (including degradation of β and noise increase) and other parameters. Spice simulation of amplifier circuits using the insights from the radiation and matching studies.

Year 2: Design and fabrication of a front-end ASIC for readout of silicon strip detectors and thorough characterization.

We are planning to collaborate with Prof. John Cressler's group at the Georgia Institute of Technology, which has been working with SiGe technologies for many years. The ASIC design work will be done by Prof. D. Dorfan and Mr. Ned Spencer, our experts in low power ASIC design and layout.

1.3. Hybrids and Integration

The main activity will be developing hybrids to be able to read out detectors and acquire the data from the ASICs. We will also develop test boards to be able to characterize the SiGe ASICs electrically. Here the considerable experience of our staff in interfacing SSD and ASICs will be invaluable. We will build hybrids and assemble a DAQ system to read out first the test structures, and then develop a hybrid for reading out an entire short strip detector. In addition, we will collaborate with the group developing larger silicon strip detector assemblies, i.e. "staves", which will embed single detectors into a mechanical and electrical super-structure. We will contribute our experience and convey our needs to this effort, and in turn use principles developed in the stave design to guide our hybrid concepts.

2. Milestones

Year 1

SSD test structures characterized	4/1/2005
DAQ and source telescope working	4/1/2005
SSD test structure board constructed	4/1/2005
SiGe test structures characterized	4/1/2005
SiGe test structures irradiated	5/1/2005
SiGe technology files updated	6/1/2005
Efficiency measurements with SSD test structures	10/1/2005
Layout of short-strip SSD	10/1/2005

Year 2

Layout of SiGe ASIC	12/1/2005
Layout of SiGe test board	2/1/2006
Layout of short SSD hybrid	3/1/2006
Short strip SSD fab'd	4/1/2006
Short SSD hybrid fab'd	4/1/2006
SiGe ASIC fab'd	4/1/2006
SiGe test board fab'd	4/1/2006
SiGe ASIC characterized	10/1/2006
Efficiency measurements on short strip SSD	10/1/2006

3. Funding and Resources

We show below the costs for a two year program. All labor rates include fringe benefits. The off-campus overhead rate of 24.4% is used. Tasks performed by physicists and grad students are shown as $0 in the budget. The travel budget is for trips to US Upgrade meetings, to visit collaborating institutions and suppliers and to perform irradiations. The equipment budget is for the DAQ system, test equipment and a digital oscilloscope. The SSD and SiGe fabrication runs are cost shared with collaborating institutions.

FY 2005 Budget

		FY 2005						
		Labor			M+S			Total
	Activity	hrs	$/hr	Labor	num	cost/part	M+S	
1.1	**SSD**							
1.1.1	**Test structures Module**							
1.1.1.1	SSD Samples				4	$1,000	$4,000	$4,000
1.1.1.2	RC Chips				1	$1,000	$1,000	$1,000
1.1.1.3	Electrical Characterization	320	$12.00	$3,840				$3,840
1.1.1.4	Assembly	100	$32.38	$3,238				$3,238
1.1.1.5	DAQ	480	$12.00	$5,760	2	$1,500	$3,000	$8,760
1.1.1.6	Efficiency Measurements	320	$12.00	$3,840				$3,840
1.1.2	**Short strip SSD Module**							
1.1.2.1	SSD Samples	160	$52.27	$8,363	1	$10,000	$10,000	$18,363
1.1.2.3	Electrical Characterization	320	$12.00	$3,840				$3,840
1.2	**FEE**							
1.2.1	**Test structures**							
1.2.1.1	Samples							
1.2.1.2	Mounting on DC boards	41	$32.38	$1,328	3	$500	$1,500	$2,828
1.2.2	**ASIC**							
1.2.2.4	ASIC layout	130	$75.00	$9,750				$9,750
1.3	**Integration / Interconnects**							
1.3.1	**SSD test structure board**							
1.3.1.1	Design and layout	200	$52.27	$10,454				$10,454
1.3.1.2	Fab				1	$2,300	$2,300	$2,300
1.3.1.3	Parts				1	$200	$200	$200
1.3.1.3	Test	20	$35.80	$716				$716
1.3.1.4	Assembly	160	$32.38	$5,181				$5,181
1.3.2	**ASIC test board**							
1.3.2.1	Design and layout	40	$52.27	$2,091				$2,091
Total Direct				**$58,400**			**$22,000**	**$80,400**
Indirect 24.4%								**$19,618**
Total 2005								**$100,018**

FY 2006 Budget

		FY 2006						
		Labor			M+S			Total
	Activity	hrs	$/hr	Labor	num	$/part	M+S	
1.1	**SSD**							
1.1.2	**Short strip SSD Module**							
1.1.2.1	SSD Samples				1	$40,000	$40,000	$40,000
1.1.2.2	RC Chips				1	$5,000	$5,000	$5,000
1.1.2.3	Electrical Characterization	320	$35.80	$11,456				$11,456
1.1.2.4	Assembly	160	$32.38	$5,181				$5,181
1.1.2.5	DAQ			$0				$0
1.1.2.6	Efficiency Measurements			$0				$0
1.1.2.7	Irradiations			$0				$0
1.1.2.8	Electrical Characterization	160	$35.80	$5,728				$5,728
1.1.2.9	Efficiency Measurements			$0				$0
1.2	**FEE**							
1.2.2	**ASIC**							
1.2.2.1	Work on technology file							
1.2.2.2	ASIC design	160	$75.00	$12,000				$12,000
1.2.2.3	ASIC simulation	160	$75.00	$12,000				$12,000
1.2.2.4	ASIC layout	320	$75.00	$24,000				$24,000
1.2.2.5	ASIC fab				1	$54,000	$54,000	$54,000
1.2.2.6	ASIC test	160	$75.00	$12,000				$12,000
1.3	**Integration / Interconnects**							
1.3.2	**ASIC test board**							
1.3.2.1	Design and layout	160	$52.27	$8,363				$8,363
1.3.2.2	Fab				1	$2,500	$2,500	$2,500
1.3.2.3	Parts				1	$800	$800	$800
1.3.2.4	Test	20	$35.80	$716				$716
1.3.2.5	Assembly	100	$32.38	$3,238				$3,238
1.3.3	**Short-strip hybrid**							
1.3.3.1	Design and layout	200	$52.27	$10,454				$10,454
1.3.3.2	Fab				1	$10,000	$10,000	$10,000
1.3.3.3	Parts				1	$2,000	$2,000	$2,000
1.3.3.4	Test	50	$35.80	$1,790				$1,790
1.3.3.5	Assembly	320	$32.38	$10,362				$10,362
	Total Labor and M+S			**$117,288**			**$114,300**	**$231,588**
1.4	**Travel**							
1.4.1	Domestic travel				4	$1,500	$6,000	**$6,000**
1.4.2	Foreign Travel				3	$2,500	$7,500	**$7,500**
1.5	**Equipment**							**$30,000**
	Total direct							**$275,088**
	Indirect 24.4%							**$59,801**
	Total FY2006							**$334,889**

4. **Manpower**

David Dorfan	Physicist	ASIC design
Hartmut Sadrozinski	Physicist	SSD coordination & evaluation
Abraham Seiden	Physicist	Physics, layout, rates, system
Alex Grillo	Physicist	ASIC coordination & evaluation, system
Ned Spencer	EE Eng.	ASIC design and layout, system aspects
Sergei Kashiguine	CAD Eng.	Hybrid layout, electrical measurements
Forest Martinez-McKinney	EE Tech.	Bonding, electro-mechanical integration
Max Wilder	EE Tech.	Interfaces, hybrids, characterization
TBD	Post-doc	DAQ, measurements
Jessica Metcalfe	grad. stud.	Irradiations, ASIC characterization
John Wray	student	Efficiency measurements
Jason Heimann	student	DAQ, SSD measurements

5. **Collaborating Institutions**

Institution / Principal Contacts	Activity	Industrial Partner
Georgia Institute of Technology John Cressler	SiGe characterization	IBM
Helsinki Inst. of Physics, Finland Jaakko Haerkoenen	p-type test structures / SSD Characterization of structures / SSD	HIP
University of Florence, Italy Mara Bruzzi	p-type test structures / SSD Characterization of structures / SSD	IRST
Liverpool University, UK Gian-Luigi Casse	p-type test structures / SSD Characterization of structures	Micron
Hiroshima University, Japan Takashi Ohsugi	p-type SSD	HPK