

Status Report “Development of Short-Strip Silicon Detectors and Hybrids and a Frontend Readout ASIC”

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Summary of Project Goals:

- Identification of the optimum technology and layout of the tracking detectors for the upgraded ATLAS ID and construction of a short-strip silicon detector (SSD) module with sufficient radiation hardness for the intermediate and outer tracking region in the upgraded ATLAS ID.
- Evaluation of integrated circuit technologies for the readout of the upgraded ATLAS ID, in particular the evaluation of new SiGe biCMOS technologies and the design of a prototype readout IC.

1. Summary of 2005 R&D Plan and Results

FY2005 goals:

Electrical characterization of test structures and short SSD fabricated on different wafers.

Integrate SSD with readout to determine signal and noise.

Development of efficiency measuring set-up.

Evaluation of the radiation hardness of SiGe technologies.

Milestones for Year 1

SSD test structures characterized	4/1/2005	Y
DAQ and source telescope working	4/1/2005	Y
SSD test structure board constructed	4/1/2005	Y
SiGe test structures characterized	4/1/2005	Y
SiGe test structures irradiated	5/1/2005	Y
SiGe technology files updated	6/1/2005	in progress
Efficiency measurements with SSD test structures	10/1/2005	Y
Layout of short-strip SSD	10/1/2005	in progress

The milestones have been met or there is good progress to meet them during this year.

2. Detailed Results

2.1. SSD

Based on the charge collection results from RD50 [1], we anticipate p-type detectors will be the main contender for the SSD technology in the intermediate region at the LHC upgrade. In that region with radius from ~ 20 to ~ 55 cm, occupancy considerations dictate

the use of short strip detectors of about 3 cm length. If proven to be reliable, affordable (single-sided processing!) and supported by high-volume manufacturers, p-type might get used in the long strips in the outer region of the upgrade detector beyond a 55 cm radius as well.

In addition to the leakage current increase, which can be minimized by cooling, radiation damage causes a change in the doping concentration, i.e. increased depletion voltage, and a shortening of the trapping time, i.e. loss of signal. Like the more expensive n-on-n detectors used in the ATLAS Pixel System, SSDs produced on p-type wafers allow operation after heavy radiation damage with moderate loss of performance: the signals are collected on the junction side, and thus the detector can be operated under-depleted, i.e. the bias voltage does not have to exceed the depletion voltage to be efficient, as in the p-on-n detectors after type inversion. For example, after a fluence level one wants to plan for in the short strip region, i.e. $3 \cdot 10^{15}$ neq/cm², the depletion voltage of 300 μ m thick detectors is about 1500V, much larger than the voltages one would like to apply. With a bias voltage of 800V, about 216 μ m are depleted, and this length can be used to collect charge, but only with p-type detectors, and not with p-on-n detectors, which require full depletion. Trapping of the charge during drift to the electrodes adds to the loss of charge, and here the p-type detectors have the advantage of collecting electrons, which have higher mobility. After a fluence of $3 \cdot 10^{15}$ neq/cm² and with a bias voltage of 800V, the collected charge is 40% of the one generated in 300 μ m thick detectors. Thus while the inability to deplete the detector leads to a charge collection efficiency of 72%, trapping results in only 56% of the charge being collected from the depleted region. For a fluence of $3 \cdot 10^{14}$ neq/cm², characteristic for the outer-most tracker region, the detector can be depleted with a bias voltage of 400 V, and the charge loss due to trapping is about 10%.

The main emphasis of RD50 has been the investigation of pad detectors, and bulk parameters like the depletion voltage have been measured with C-V and global charge collection methods. This helped identify potential choices for the p-type wafer material, and both float zone (FZ) and magnetic Czochralski (MCz) are under investigation. Very little is known about the behavior of p-type strip detectors. Examples are the dependence on the wafer material and processing steps of surface parameters like the interstrip capacitance and the strip isolation, both pre- and post-rad.

The performance of a tracker is characterized by the signal-to-noise ratio S/N, and we have started to investigate the dependence of the detector noise on the wafer material. The noise RMS σ_{Noise} is parameterized in the form $\sigma_{\text{Noise}} = a + b \cdot C$ where C is the total capacitance, for which the interstrip capacitance is the major contributor (additional contributions also come from leakage current and the bias resistance). The interstrip capacitance is influenced by the geometry of implants, the starting material (n-type vs. p-type) and the way the surface is processed, for example p-stop implants vs. p-spray and the p-spray dose. With many of these details still under investigation for the final detector fabrication due to the limited experience with p-type detectors, we have started to investigate the noise contribution of different materials (n- and p-type FZ, MCz). We are measuring the interstrip capacitance as a function of bias voltage, and in the same SSD the noise after integration to an ASIC (PMFE) with reasonably short shaping time (100 ns). We expect soon to switch over to an ASIC with 20 ns shaping time, appropriate for

LHC. The present ATLAS SCT readout ASIC (ABCD) can't be used because it requires positive signals. In addition it is not sufficiently radiation-hard for the LHC upgrade.

2.1.1. Strip Test Detectors

We have teamed with the Italian SMART collaboration within RD50 and received strip test detectors for measurements, both FZ and MCz made on p-type wafers. We have taken I-V and C-V measurements, which are in good agreement with the studies by Italian institutions. The pre-rad leakage currents on these detectors are a factor 50 higher than on high quality n-type SSD. After irradiation, the detectors currents will be 1000 times larger than pre-rad, similar to n-type, and the initial current level might only be of interest to identify surface problems. We will continue to collect data on the leakage currents of p-type detectors to understand if their origin is wafer dependent or due to processing. Recently we received a few strip detectors irradiated at KFZ Karlsruhe, and we will perform parametric electrical studies and noise and charge collection studies in the fall.

2.1.2. Noise and Interstrip Capacitance

The noise RMS σ_{Noise} and the interstrip capacitances are well correlated. In Fig. 1, we show the noise RMS curve for the PMFE with external capacitors. The curve is well described by a linear relationship $\sigma_{\text{Noise}} = 295 + 35 \cdot C$. In the same plot, the RMS noise from an old n-type detector with fairly wide implants (thus large interstrip capacitance) [2], [3] and from a shorter p-type SSD are shown. The agreement between the measured noise values and the expected values from the capacitance is good.

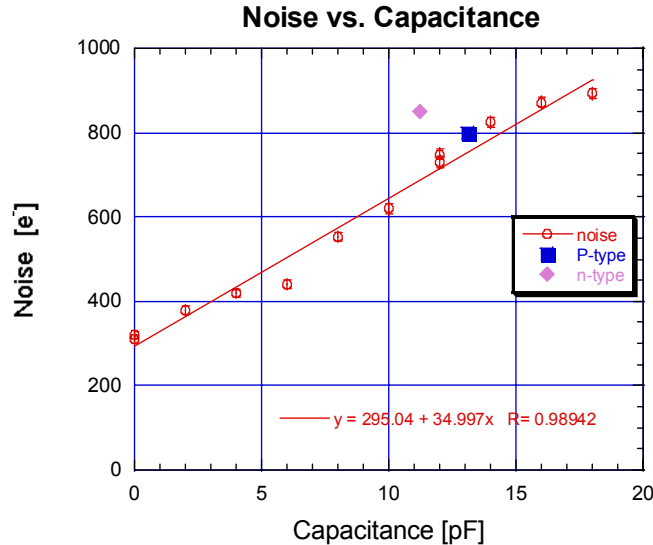


Fig. 1: Noise RMS σ_{Noise} in the PMFE ASIC as a function of external capacitance (circles), and in two detectors of different layout: a n-type detector (diamonds) and a p-type detector (squares).

2.1.3. Bias Voltage Dependence of the Interstrip Capacitance

A surprising effect in p-type is the large bias voltage dependence of the interstrip capacitance, not observed in n-type detectors. This is shown in Fig. 2. This has been observed on all p-type detectors pre-rad, resulting in high interstrip capacitances at low bias voltages. The interstrip capacitance continues to change with the bias voltage well beyond the depletion voltage (about 80V), in some cases reaching saturation only at bias voltages of 400V. At the same time the interstrip capacitance decreases with bias, the interstrip resistance decreases. This points to the existence of an electron layer on the surface, which gets depleted at much higher bias voltage than the depletion voltage. The interstrip capacitance saturates fastest in the SSD with large pitch.

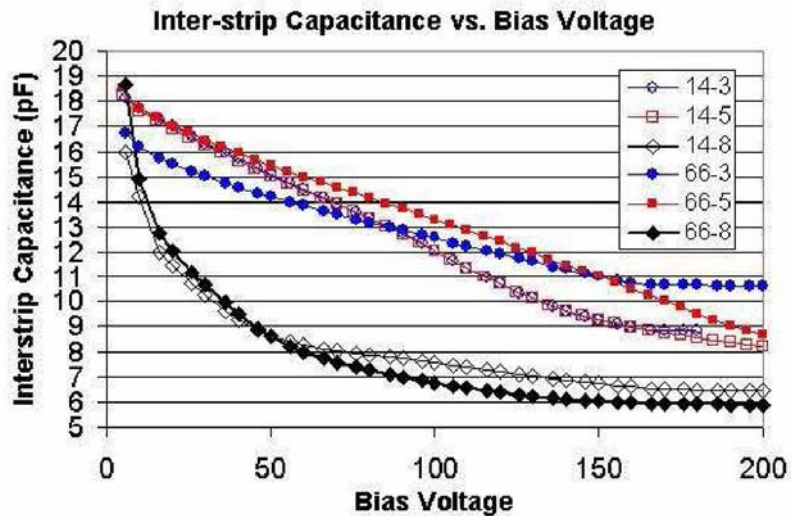


Fig. 2 Interstrip capacitance as a function of bias voltage for several p-type SSD of 4.46 cm length. SSD 14-8 and 66-8 have 100 μm pitch, wafer 14 is FZ, 66 is MCz.

There are indications that the interstrip capacitance is lower and more constant after irradiations [4]. We will investigate this by irradiating with ^{60}Co gammas a few of the SMART detectors we tested before and see if the interstrip capacitance has decreased, after the generated interface charges compensate the charges from the p-spray. At the same time we will measure the interstrip resistance and see if the strip isolation improves with radiation.

2.1.4. Interstrip Capacitance of Different Wafer Materials

The very strong bias voltage dependence of the interstrip capacitance makes a comparison between different materials difficult since the bias dependence is material dependent. In addition, p-type detectors with different doping density show different breakdown behavior. With this caveat, we have compiled a first comparison of the total capacitance of different materials. This is shown in Fig. 3, which should be used only as an indication of what kind of information can be extracted from the interstrip capacitance / noise studies. As seen before [2], the geometry of the strips, i.e. the strip width over strip pitch ratio plays a crucial role.

Another preliminary conclusion is that MCz detectors have about the same strip capacitance as FZ p-type detectors.

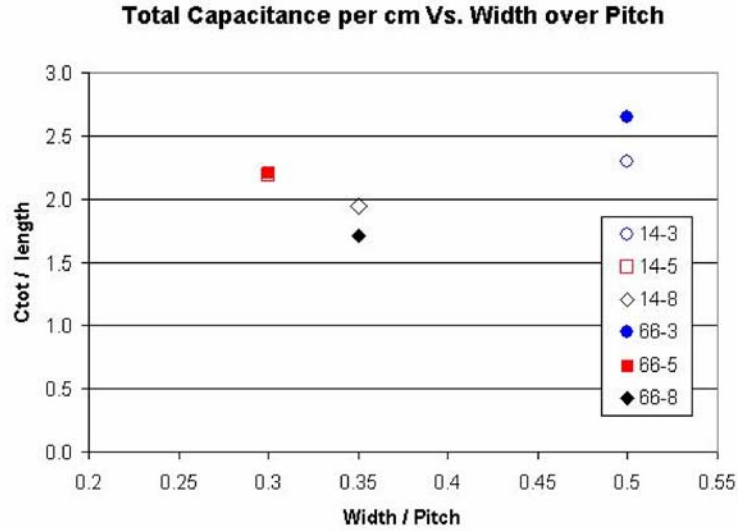


Fig. 3 Total capacitance per unit length at 200V bias for several p-type SSD as a function of strip width over pitch ratio (wafer 14 is FZ, wafer 66 is MCz).

2.1.5. Efficiency Measurements

Our electron telescope using a ^{90}Sr source permits to measure the charge collection efficiency CCE, yielding information on depletion voltage (independent and more relevant to detector operation than C-V) and trapping. As shown in Fig. 4, pre-rad both CCE and CV give the same depletion voltage of 80V. After irradiation, we expect this still to hold for the p-type SSDs, while p-on-n SSDs require then large over-depletion. A cold box is being constructed for measurements on irradiated detectors.

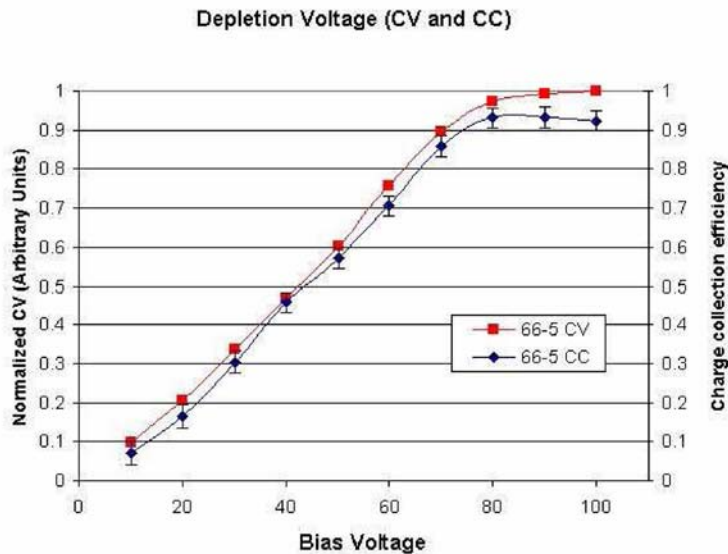


Fig. 4 Bias dependence of the charge collection efficiency (CCE) and the back-plane capacitance (CV) of a p-type SSD.

2.1.6. Preparation of short-strip SSD Fabrication

A next submission within RD50 for production of test SSD is being prepared. Important is the transfer of the technology to a commercial foundry with 6" wafers. The following questions will be addressed:

- a. P-type isolation study (p-spray vs implants, modified p-spray)
- b. Geometry dependence (minimize w/p)
- c. Charge collection studies
- d. Noise studies
- e. System studies: cooling, high bias voltage operation,
- f. Different materials (MCz, Epi)
- g. Thickness

2.2. Frontend ASIC

Test structures of a SiGe biCMOS process were irradiated with protons to several fluences up to 1×10^{16} p/cm². Reasonable electrical performance was measured after irradiation demonstrating that the SiGe bipolar devices can be quite radiation hard. Several different SiGe fabrication processes are now being studied. A prototype, proof-of-principle, front-end circuit is now being designed to be ready for fabrication in fall 2005.

2.2.1. Irradiation of Test Structures

We obtained test structures from one of the commercial SiGe biCMOS (IBM 5HP) processes from our collaborators at the Georgia Institute of Technology. Each set of test structures was a collection of several transistors and other components arrayed on a wafer chip. We selected several transistor sizes and some matched transistor pairs for testing. The devices were characterized in Santa Cruz, then brought to CERN for irradiation with protons and then returned to Santa Cruz for re-testing after sufficient time for the activation to reach safe levels. The irradiations were carried out by our graduate student, Jessica Metcalfe, in the RD50 irradiation setup at the CERN PS in the fall of 2004.

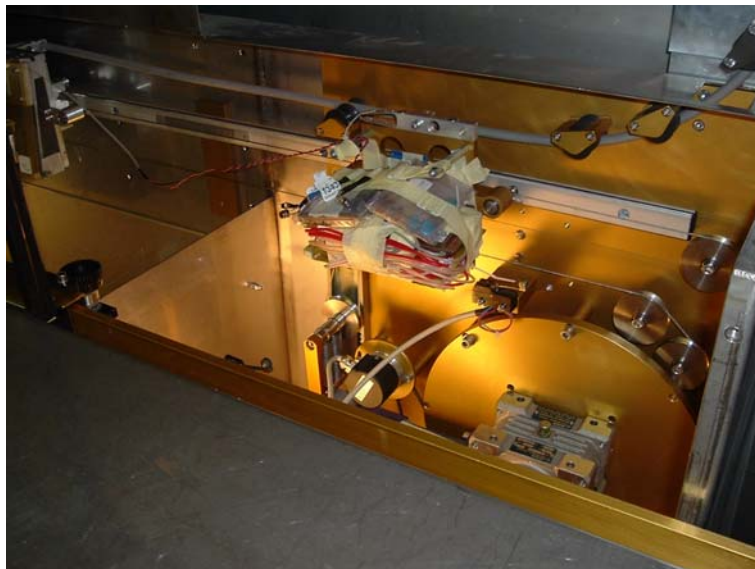


Figure 5: RD50 Shuttle for Irradiating Samples at the CERN PS

The shuttle system developed by the RD50 group to move samples into the PS beam line is shown in Figure 5. The test structure arrays mounted on printed circuit boards for testing are shown in Figure 6 after they have been irradiated.

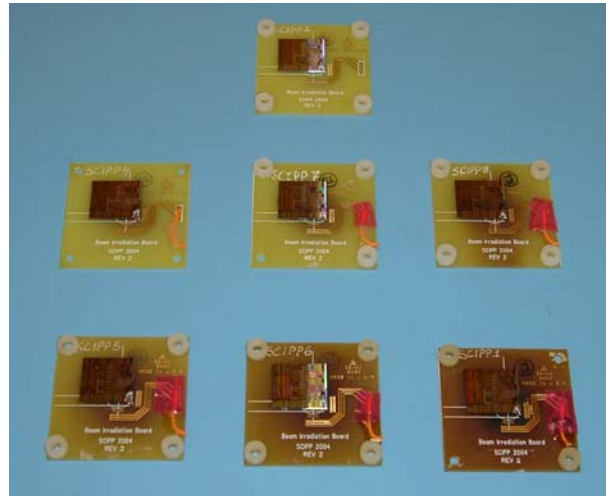


Figure 6: Test Structure Arrays on PCBs after Irradiations to Fluences of 0, 4×10^{13} , 1×10^{14} , 3.5×10^{14} , 1×10^{15} , 3.6×10^{15} and 1×10^{16} .

2.2.2. Irradiation Test Results

Figure 7 shows a typical Gummel plot of the performance of one transistor after it was irradiated to 1.3×10^{15} p/cm². As expected the radiation damage manifests itself as an increase in the base leakage current which effectively decreases the DC current gain β , which is the ratio of collector current to base current. When the bias current is scaled by the transistor size we see in Figure 8 that β as a function of fluence is independent of transistor size. This figure also shows that the transistors are still operational after being irradiated to 1×10^{16} p/cm² although the performance at the highest fluence is marginal.

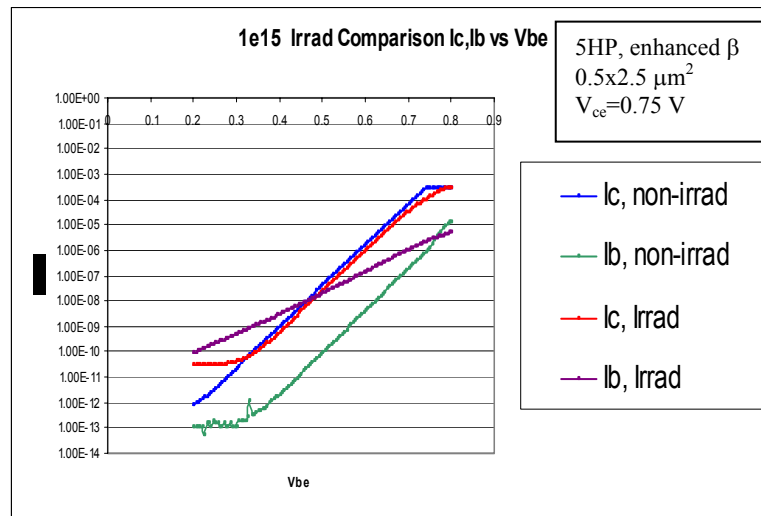


Figure 7: Gummel Plot for $0.5 \times 2.5 \text{ mm}^2$ transistor irradiated to 1.3×10^{15} p/cm².

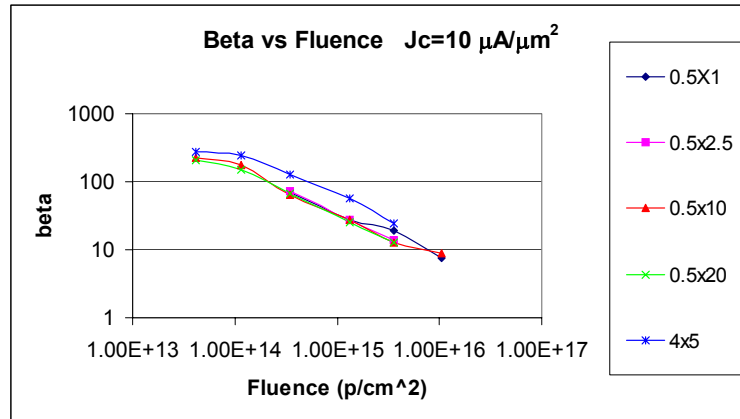


Figure 8: DC current gain β vs. fluence at fixed collector current density $J_c = 10 \mu\text{A}/\mu\text{m}^2$.

After the post-irradiation testing was completed, annealing tests were performed to determine to what extent the damage can be repaired. Annealing at elevated temperature accelerates the repair thus emulating the effects of a longer time at normal operating temperatures. Figure 9 shows the resulting improvement of β for one transistor, which had been irradiated to $1 \times 10^{15} \text{ p/cm}^2$. One can see from the plot a very marked improvement (e.g. β increases from 15 to 51 at $10 \mu\text{A}$ of bias current) after full annealing. Part of our ongoing work is to determine how much of this annealing is to be expected during normal operation of the transistors over an extended period of time.

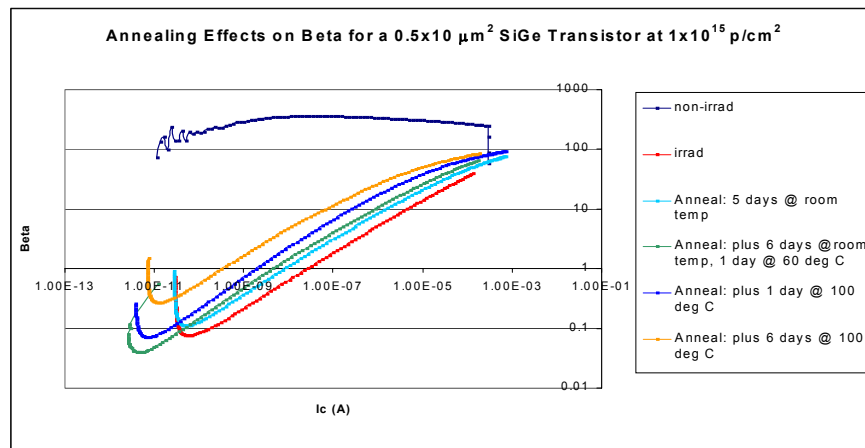


Figure 9: Annealing of radiation damage after $3 \times 10^{15} \text{ p/cm}^2$: part of the β loss is restored.

The results up to a fluence of $3 \times 10^{15} \text{ p/cm}^2$ look quite encouraging. The data point at $1 \times 10^{16} \text{ p/cm}^2$ was taken as an exploratory measure just to see how rad-hard this technology is. The range of interest for mid and outer radii of the upgraded ATLAS Inner Tracker does not exceed $3 \times 10^{15} \text{ p/cm}^2$ and is probably closer to $1 \times 10^{15} \text{ p/cm}^2$ for the inner most radius of interest for non-pixel silicon detectors. It is envisioned that pixel detectors with solely CMOS, not biCMOS, electronic readout will occupy the inner most

radii where the fluences exceed 3×10^{15} p/cm². The fact that these SiGe devices are still operational at 1×10^{16} p/cm² shows that there is some margin above the desired fluence.

Table 1: Bias Currents required to achieve β of 50 at fluence of 1.3×10^{15} p/cm²

Fluence: 1.34E15		
$\beta=50$		
Transistor Size μm^2	Required Current	
	I_c irradi	I_c anneal
0.5x1	3.E-05	1.E-07
0.5x2.5	7.E-05	4.E-06
0.5x10	4.E-04	1.E-05
0.5x20		6.E-05
4x5	1.E-04	1.E-05

If one chooses a β of 50 as the minimum acceptable value for post-rad operation, one can estimate at what minimum bias current each different size transistor can operate and whether this will represent a significant power savings over CMOS. Table 1 shows that all of the various transistor sizes will operate at a fluence of 1×10^{15} p/cm² with very modest bias currents, less than 100 μA for the large transistor to be used as the first stage amplifier and a fraction of a micro-Amp for the smallest transistors to be used in the other shaping and comparator stages. Using more conservative estimates of currents of 50-150 μA for the large front-end transistor and 5 μA for the small transistors, a crude estimate for power consumption is 0.25 to 0.50 mW/channel which would be a factor of 3 to 4 lower than that achieved by a comparable CMOS circuit [5]. If this can be realized, it would represent a considerable power savings for the ATLAS Tracker and help the problem of providing services.

3. R&D Plan for Year 2

3.1. SSD

In the second year, we will produce short-strip silicon strip detectors in the geometry appropriate for the intermediate region of the ATLAS upgrade ID, and construct single detector modules with fast low-noise readout. This will require new hybrids, which will be based on the successful ATLAS SCT hybrid design. The modules will also be a test bed for the ASICs based on SiGe technology.

We are planning to collaborate with US groups (BNL, Hawaii) and international partners mainly within RD50 on developing, irradiating and characterizing test structures and prototype detectors, and the design and fabrication of hybrids and readout DAQ. If the CERN testbeam will be available, we will irradiate the detectors with fluences up to 3×10^{15} p/cm².

3.2. Front-end ASIC

We have determined that there are at least 25 fabrication facilities that make similar SiGe biCMOS integrated circuits [6]. Some have more than one generation. Since each of these processes differs in the details of the collector-base-emitter structure and in

particular differs in the structure of the oxide isolation, it is possible that they have different levels of radiation tolerance. We believe that it is important to understand these differences and to judge a few of the available processes in order to best choose the appropriate process for a future upgrade. We have made arrangements to sample test structures from three vendors, IBM, IHP and STm. We plan to do similar radiation studies with samples from all three vendors, in some cases with more than one of their generations. This will give us a better understanding of the sensitivities of radiation tolerance to device structure and process. We have also made arrangements to irradiate samples with neutrons and gammas as well as protons. This will be accomplished in this second year.

Given the number of potential fabrication processes and the work involved in updating technology files to reflect post-rad parameters, we have postponed the completion of this one milestone until we have sampled more technologies. We will then update at least one, which appears to be a potential technology for a future upgraded tracker.

In order to advance our understanding of the true power savings beyond the level of calculated estimates, we will also design and fabricate a chip with a few channels of a front-end readout using one of the available processes that we are studying. Technology files from IHP have been obtained and design work has started. This may not be our final choice for optimum process but should be representative of the potential power savings. A full readout chip with a fully qualified SiGe biCMOS process will await future work after year 2 is completed.

Year 2 Milestones

Layout of short SSD hybrid	3/1/2006
Short strip SSD fab'd	6/1/2006
Short SSD hybrid fab'd	6/1/2006
Efficiency measurements on short strip SSD	10/1/2006
Layout of SiGe proof-of-principle IC	12/1/2005
Layout of test board for SiGe proof-of-principle IC	2/1/2006
SiGe test structures characterized from multiple vendors	3/1/2006
SiGe proof-of-principle IC fabricated	4/1/2006
SiGe test board fab'd	4/1/2006
SiGe test structures irradiated from multiple vendors	7/1/2006
SiGe proof-of-principle IC characterized	10/1/2006
SiGe technology files updated for at least one process	10/1/2006

4. References

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- [2] E. Barberis et al., *IEEE TNS* 41. 785, 1994
- [3] E. Barberis et al., *Nucl. Inst and Meth. A* 342. 90, 1994
- [4] 6th RD50 Workshop, Helsinki June 2-4 2005
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- [5] J. Kaplon et al., "Fast CMOS Binary Front-End for Silicon Strip Detectors at

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6. Manpower

David Dorfan	Physicist	ASIC technology and design
Alex Grillo	Physicist	ASIC coordination & evaluation, system
Hartmut Sadrozinski	Physicist	SSD coordination & evaluation
Abraham Seiden	Physicist	Physics, layout, rates, system
Ned Spencer	EE Eng.	ASIC design and layout, system aspects
Sergei Kashiguine	EE Eng.	Hybrid layout, electrical measurements
Max Wilder	EE Tech.	Interfaces, hybrids, characterization
David Larson	Tech.	DAQ
Jessica Metcalfe	grad. stud.	Irradiations, ASIC characterizations
Ken Fowler	grad. stud.	Efficiency meas., SSD characterizations
John Gerling	student	Efficiency meas., SSD characterizations
Kunal Arya	student	DAQ
Nate Blumenkrantz	student	SSD characterizations
Ashley Jones	student	ASIC characterizations
Dominic Lucia	student	ASIC characterizations
Matthew Mendoza	student	ASIC characterizations