Signal-to-Noise with SiGe

7th RD50 Workshop
CERN

Hartmut F.-W. Sadrozinski
SCIPP – UC Santa Cruz
Technical (Practical) Issues

The ATLAS-ID upgrade will put large constraints on power. Can we meet power and shaping time requirements with deep sub-micron CMOS?

- Achieving sufficient transconductance of the frontend transistor typically requires large bias currents.

The changes that make SiGe Bipolar technology operate at 100 GHz for the wireless industry coincide with the features that enhance performance for our application.

- Small feature size increases radiation tolerance
- Extremely small base resistance (of order 10-100 Ω) affords low noise designs at very low bias currents.

Can these features help us save power?

Will the SiGe technologies meet rad-hard requirements?
Evaluation of SiGe Radiation Hardness

The Team


SCIPP-UC Sanat Cruz

Collaborators:
A. Sutton, J.D. Cressler
Georgia Tech, Atlanta, GA 30332-0250, USA
M. Ullan, M. Lozano
CNM, Barcelona
S. Rescia et al.
BNL
Irradiated Samples

Thanks, Michael & Maurice!

Pre-rad

4.15 x 10^{13}  
1.15 x 10^{14}  
3.50 x 10^{14}  
1.34 x 10^{15}  
3.58 x 10^{15}  
1.05 x 10^{16}

ATLAS Upgrade
Outer Radius

Mid Radius

Inner Radius
Radiation Damage Mechanism

Ionization Damage (in the spacer oxide layers)

- The charged nature of the particle creates oxide trapped charges and interface states in the emitter-base spacer increasing the base current.

Displacement Damage (in the oxide and bulk)

- The incident mass of the particle knocks out atoms in the lattice structure shortening hole lifetime, which is inversely proportional to the base current.

Radiation damage increases base current causing the gain of the device to degrade.

Gain = \( \frac{I_c}{I_b} \) (collector current/base current)

Forward Gummel Plot for 0.5x2.5 \( \mu \text{m}^2 \)

\( I_c, I_b \) vs. \( V_{\text{be}} \) Pre-rad and After 1x10\(^{15} \) p/cm\(^2\) & Anneal Steps

Collector current remains the same

Base current increases after irradiation

\( \text{IC (pre-rad)} \)
\( \text{IB (pre-rad)} \)
\( \text{IC (1e15, anneal)} \)
\( \text{IB (1e15, anneal)} \)
We studied the effects of annealing. The performance improves appreciably. In the case above, the gain is now over 50 at 10\( \mu \)A entering into the region where an efficient chip design may be implemented with this technology. The annealing effects are expected to be sensitive to the biasing conditions. We plan to study this in the future.
Initial Results

Current Gain beta vs. Ic for 0.5 um x 10um
pre-rad and for all Fluences including full annealing

After irradiation, the gain decreases as the fluence level increases. Performance is still very good at a fluence level of 1x10^{15} p/cm². A typical Ic for transistor operation might be around 10 µA where a β of around 50 is required for a chip design. At 3x10^{15}, operation is still acceptable for certain applications.
Feasibility for ATLAS ID Upgrade

Qualifications for a good transistor:

A gain of 50 is a good figure of merit for a transistor to use in a front-end circuit design.

Low currents translate into increased power savings.

<table>
<thead>
<tr>
<th>Fluence: 3.50E14 p/cm² (2.17x10¹⁴ neq/cm²)</th>
<th>Fluence: 1.34E15 p/cm² (8.32x10¹⁴ neq/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor Size μm²</td>
<td>I_c irrad</td>
</tr>
<tr>
<td>---------------------</td>
<td>-----------</td>
</tr>
<tr>
<td>0.5x1</td>
<td>2.E-06</td>
</tr>
<tr>
<td>0.5x2.5</td>
<td>4.E-06</td>
</tr>
<tr>
<td>0.5x10</td>
<td>3.E-05</td>
</tr>
<tr>
<td>0.5x20</td>
<td>5.E-05</td>
</tr>
<tr>
<td>4x5</td>
<td>9.E-06</td>
</tr>
</tbody>
</table>

At 3.5x10¹⁴ in the outer region (60 cm), where long (10 cm) silicon strip detectors with capacitances around 15pF will be used, the collector current I_c is low enough for substantial power savings over CMOS.

At 1.34x10¹⁵ closer to the mid radius (20 cm), where short (3 cm) silicon strip detectors with capacitance around 6pF will be used, the required collector current I_c is still only 5 – 10 μA. We expect even better results from 3rd generation IBM SiGe HBTs.
Frontend Simulation Results

IHP ELDO SIMULATION STUDY RESULTS

Front Bipolar Bias: 150 uA
Bias: +2 Volts

Preamp
Gain
Shaper
Comparator

Stage Bias Currents
1.4 uA 5.8 uA 5 uA 9 uA

Back Currents Total: 21.2 uA or 43 uW @ 2 V
Using simulation of first SiGe frontend, an estimate for power can be obtained. Compare to 0.25 µm CMOS design of J. Kaplon et al., 2004 IEEE.

<table>
<thead>
<tr>
<th>CHIP TECHNOLOGY FEATURE</th>
<th>0.25 µm CMOS ABCDS/FE J. Kaplon et al., (IEEE Rome Oct 2004)</th>
<th>IHP SG25H1 SCT-FE Preliminary design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power: Bias for all but front transistor</td>
<td>330 µA</td>
<td>0.8 mW</td>
</tr>
<tr>
<td></td>
<td>$= 30 \mu A$ (conservative)</td>
<td>0.06 mW</td>
</tr>
<tr>
<td>Power: Front bias for 25 pF load</td>
<td>300 µA</td>
<td>0.75 mW</td>
</tr>
<tr>
<td></td>
<td>150 µA</td>
<td>0.30 mW</td>
</tr>
<tr>
<td>Power: Front bias for 7 pF load</td>
<td>120 µA</td>
<td>0.3 mW</td>
</tr>
<tr>
<td></td>
<td>50 µA</td>
<td>0.10 mW</td>
</tr>
<tr>
<td>Total Power (7 pF)</td>
<td>$1\times10^{15}$</td>
<td>1.1 mW</td>
</tr>
<tr>
<td>Total Power (25 pF)</td>
<td>$2\times10^{14}$</td>
<td>1.5 mW</td>
</tr>
</tbody>
</table>
Noise in Bipolar Transistors (H. G. Spieler):

\[ Q_n^2 = i_n^2 F_i T_s + e_n^2 C_{tot}^2 \frac{F_v}{T_s} \]

\[ C_{tot} = C_{det} + C_{in} \]

\[ i_n^2 = 2q_e \left( \frac{I_c}{\beta} + I_{bias} \right) \]

\[ e_n^2 = \frac{2 \left( k_B T \right)^2}{q_e I_e} + 4kT r_{bb} \]

Temperature dependence of bias current ties the noise to the temperature management of the sLHC tracker, which is already complicated by annealing of leakage current and depletion voltage.

Noise depends on product of leakage current \( I_{bias} \) and shaping time \( T_s \)

(applies to CMOS as well)
Short Strips Signal-to-Noise using SiGe Frontend

Electronic noise small, leakage current important →
Trade shaping time against operating temperature

Fixed Fluence:
2.2 \times 10^{15} \text{ neq/cm}^2 (\text{short strips})
The maximum bias voltage is 600 V

Noise(20 \text{ ns} & -20 \text{ °C}) = \text{Noise}(15 \text{ ns} & -10 \text{ °C})!

No advantage to very low temps!
Electronic noise dominant, leakage current not so important

Expect no sensitivity to shaping time or operating temperature

Temperature: -10 °C

Fixed Fluence: $2.2 \times 10^{14}$ neq/cm$^2$ (long strips)
The maximum bias voltage is 600 V

Noise at -10 °C and 20 ns acceptable!

No advantage to very low temps!
Inter-strip Capacitance

One of the most important sensor parameters contributing to the S/N ratio

Depends on the width/pitch ratio of the strips and on the isolation technique (p-stops, p-spray).

SMART reported large bias dependence on p-type detectors, due to accumulation layer.

Irradiation with $^{60}$Co (250 krad) reduces the bias dependence, as expected (c.f. talk by C. Piemonte)

SMART 14-5
p-type FZ
low-dose spray
w/p = 15/50
$V_{dep} = 85$ V
(I. Henderson, J. Wray, D. Larson, SCIPP)
Expected Performance for p-type SSD

Details in: “Operation of Short-Strip Silicon Detectors based on p-type Wafers in the ATLAS Upgrade ID M. Bruzzi, H.F.-W. Sadrozinski, A. Seiden, SCIPP 05/09

Conservative Assumptions:
\[ \alpha_p = 2.5 \cdot 10^{-17} \text{ A/cm (only partial anneal)} \]
\[ C_{\text{total}} = 2 \text{ pF/cm} \]
\[ V_{\text{dep}} = 160V + \beta \cdot \Phi \quad (\text{with } 2.7 \cdot 10^{-13} \text{ V/cm}^2) \text{ (no anneal)} \]
\[ (= 600V \text{ @ } \Phi = 10^{16} \text{ neq/cm}^2) \]
\[ \sigma^2_{\text{Noise}} = (A + B \cdot C)^2 + (2 \cdot I \cdot \tau_s)/q \quad A = 500, \ B = 60 \]

S/N for short strips vs. fluence for different bias voltages:

- 300 µm, -20deg, 400V
- 300 µm, -20deg, 600V
- 300 µm, -20deg, 800V

- 200 µm, -20deg, 400V
- 200 µm, -20deg, 600V
- 200 µm, -20deg, 800V

no need for thin detectors, unless n-type: depletion vs. trapping
600V seems to be sufficient

do need
update on fluences