Signal-to-Noise with SiGe

7th RD50 Workshop

CERN

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Technical (Practical) Issues

The ATLAS-ID upgrade will put large constraints on power.

Can we meet power and shaping time requirements with deep sub-micron CMOS?

- Achieving sufficient transconductance of the frontend transistor typically requires large bias currents.

The changes that make SiGe Bipolar technology operate at 100 GHz for the wireless industry coincide with the features that enhance performance for our application.

- Small feature size increases radiation tolerance
- Extremely small base resistance (of order 10-100 Ω) affords low noise designs at very low bias currents.

Can these features help us save power?

Will the SiGe technologies meet rad-hard requirements?

Evaluation of SiGe Radiation Hardness

The Team

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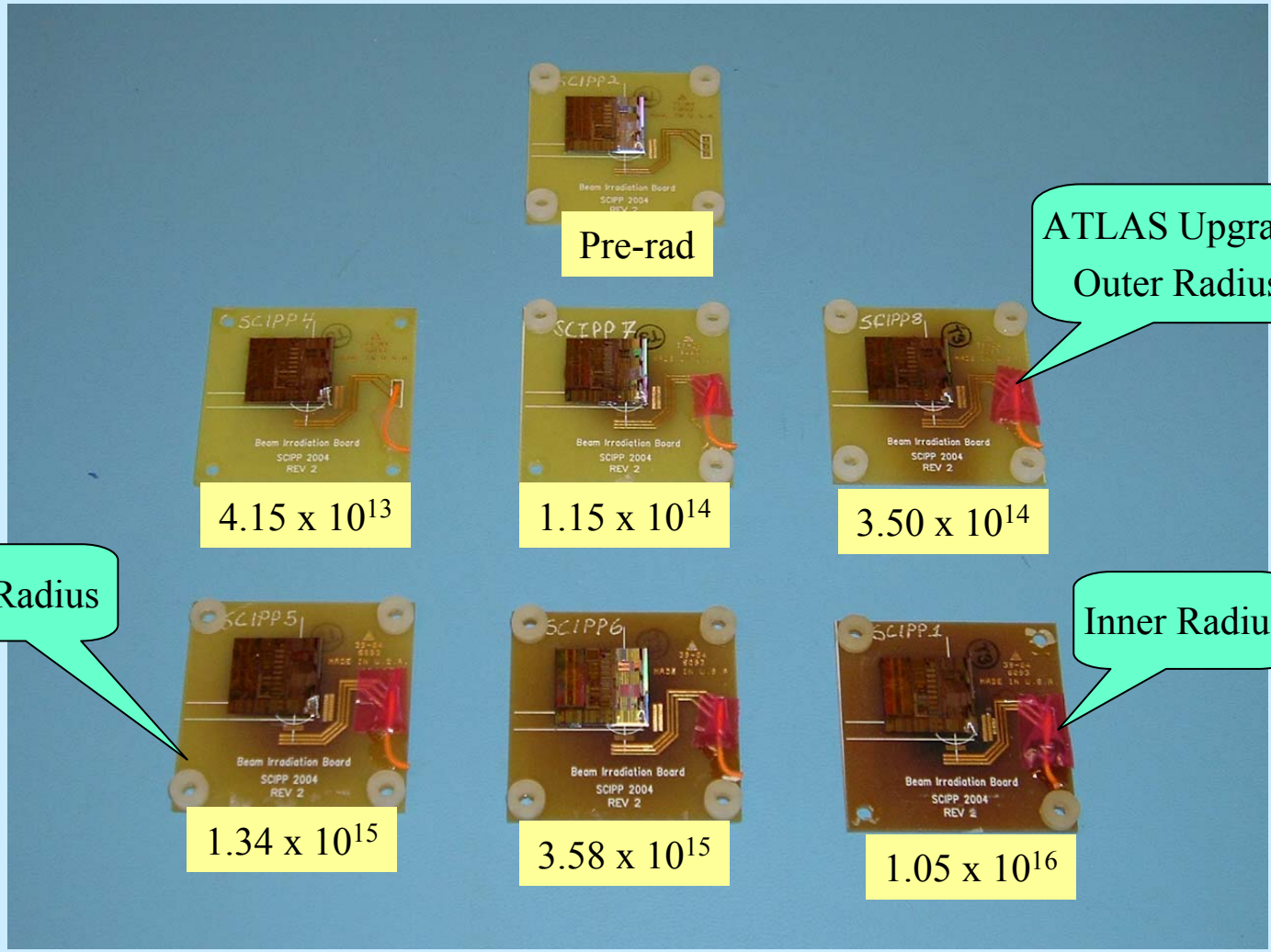
BNL

Irradiated Samples

Thanks, Michael & Maurice!



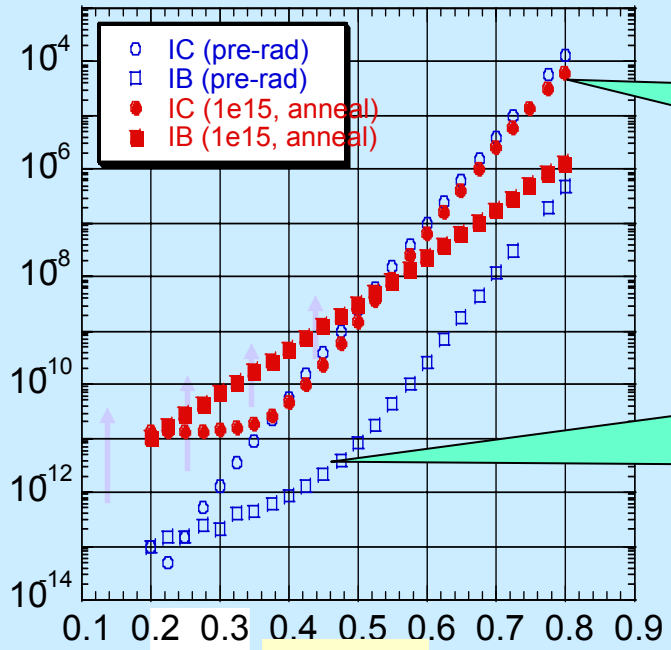
Radiation Damage Mechanism

Forward Gummel Plot for 0.5x2.5 μm²

I_c,I_b vs. V_{be} Pre-rad and After $1x10^{15}$ p/cm² & Anneal Steps

Radiation damage increases base current causing the gain of the device to degrade.

Gain=I_c/I_b (collector current/base current)



Collector current remains the same

Base current increases after irradiation

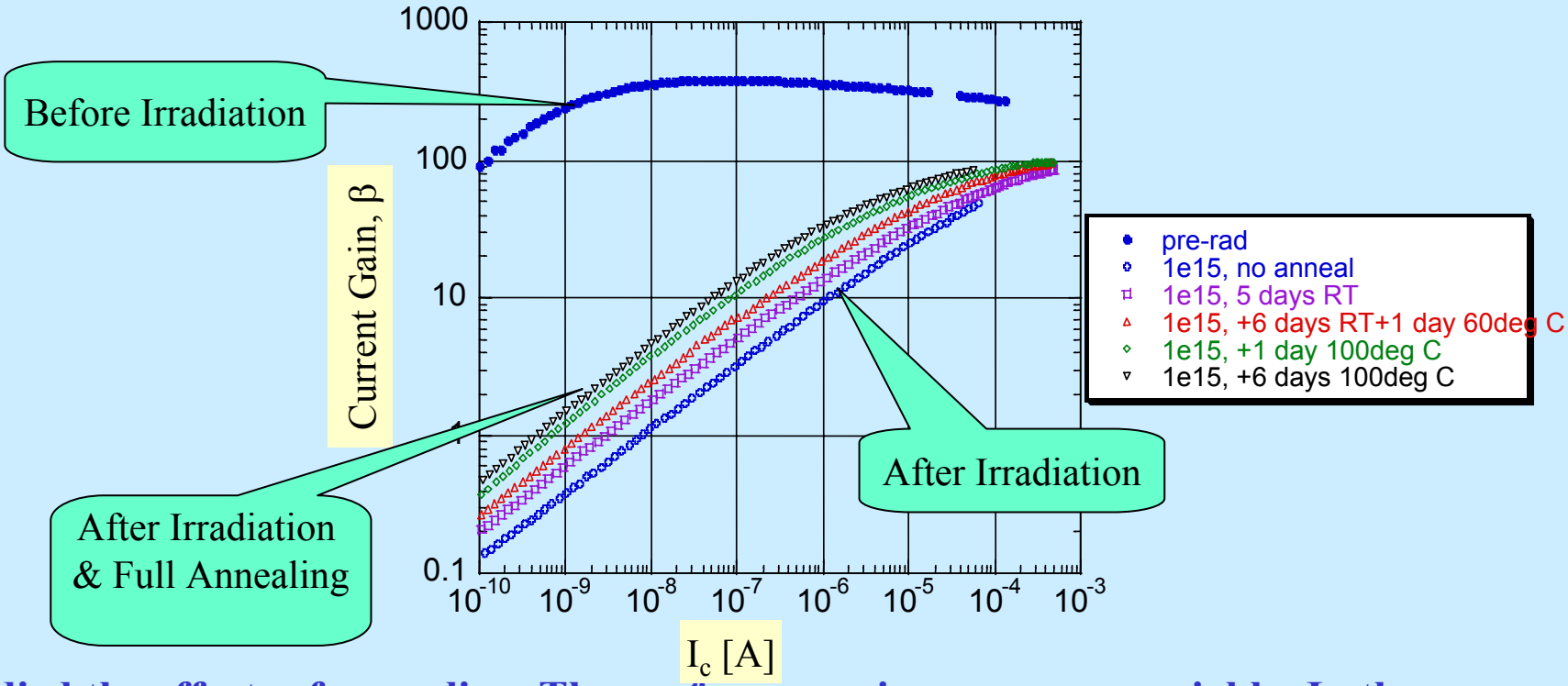
Ionization Damage (in the spacer oxide layer)

- **The charged nature of the particle creates oxide trapped charges and interface states in the emitter-base spacer increasing the base current.**

Displacement Damage (in the oxide and bulk)

- **The incident mass of the particle knocks out atoms in the lattice structure shortening hole lifetime, which is inversely proportional to the base current.**

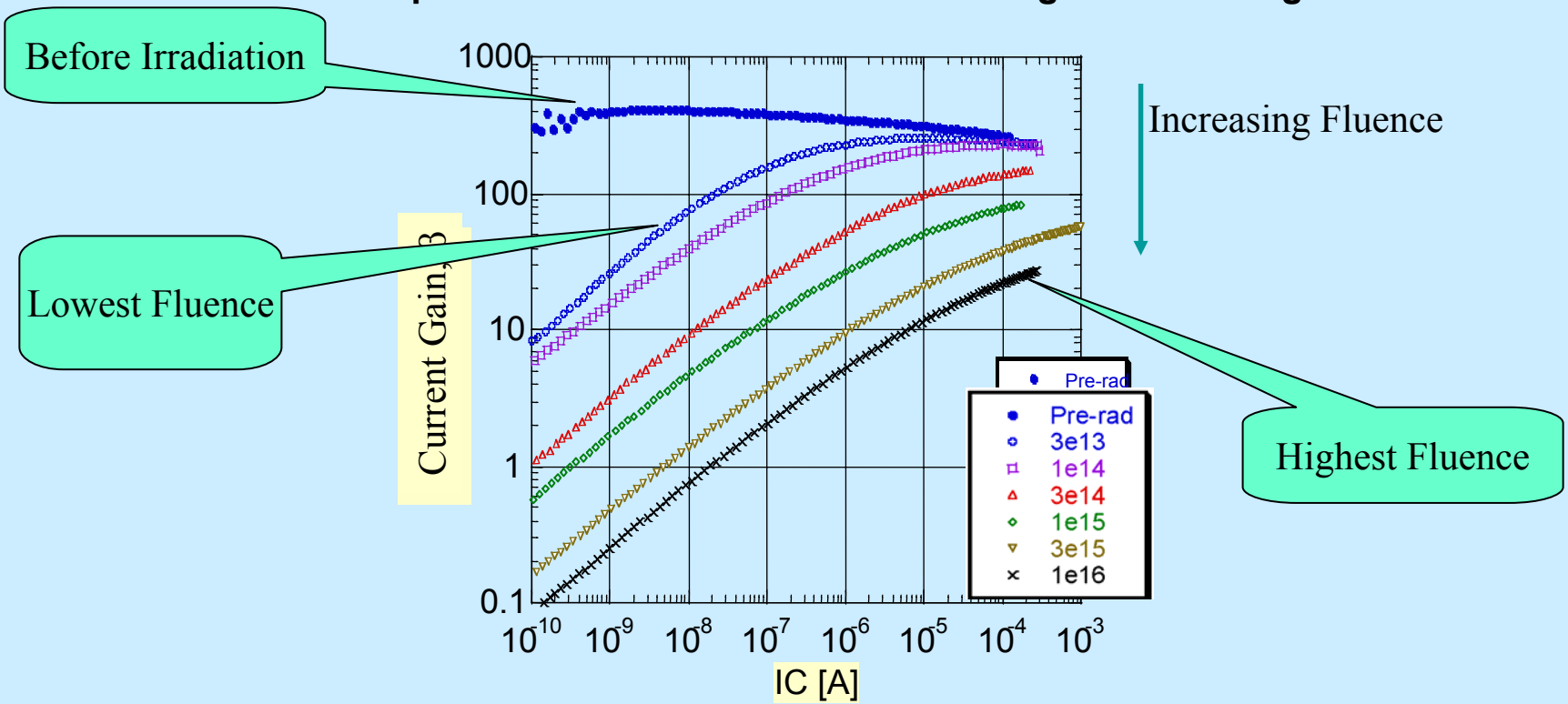
Annealing Effects



We studied the effects of annealing. The performance improves appreciably. In the case above, the gain is now over 50 at 10μA entering into the region where an efficient chip design may be implemented with this technology. The annealing effects are expected to be sensitive to the biasing conditions. We plan to study this in the future.

Initial Results

Current Gain beta vs. Ic for 0.5 um x 10um
pre-rad and for all Fluences including full annealing



After irradiation, the gain decreases as the fluence level increases. Performance is still very good at a fluence level of $1x10^{15}$ p/cm^2. A typical I_c for transistor operation might be around 10 μA where a β of around 50 is required for a chip design. At $3x10^{15}$, operation is still acceptable for certain applications.

Feasibility for ATLAS ID Upgrade

Qualifications for a good transistor:

A gain of 50 is a good figure of merit for a transistor to use in a front-end circuit design.

Low currents translate into increased power savings.

Fluence: 3.50E14 p/cm^2 (2.17x10^{14} n_{eq}/cm^2)
β=50

Transistor Size μm^2	I_c irrad	I_c anneal
0.5x1	2.E-06	
0.5x2.5	4.E-06	5.E-08
0.5x10	3.E-05	8.E-07
0.5x20	5.E-05	2.E-06
4x5	9.E-06	5.E-07

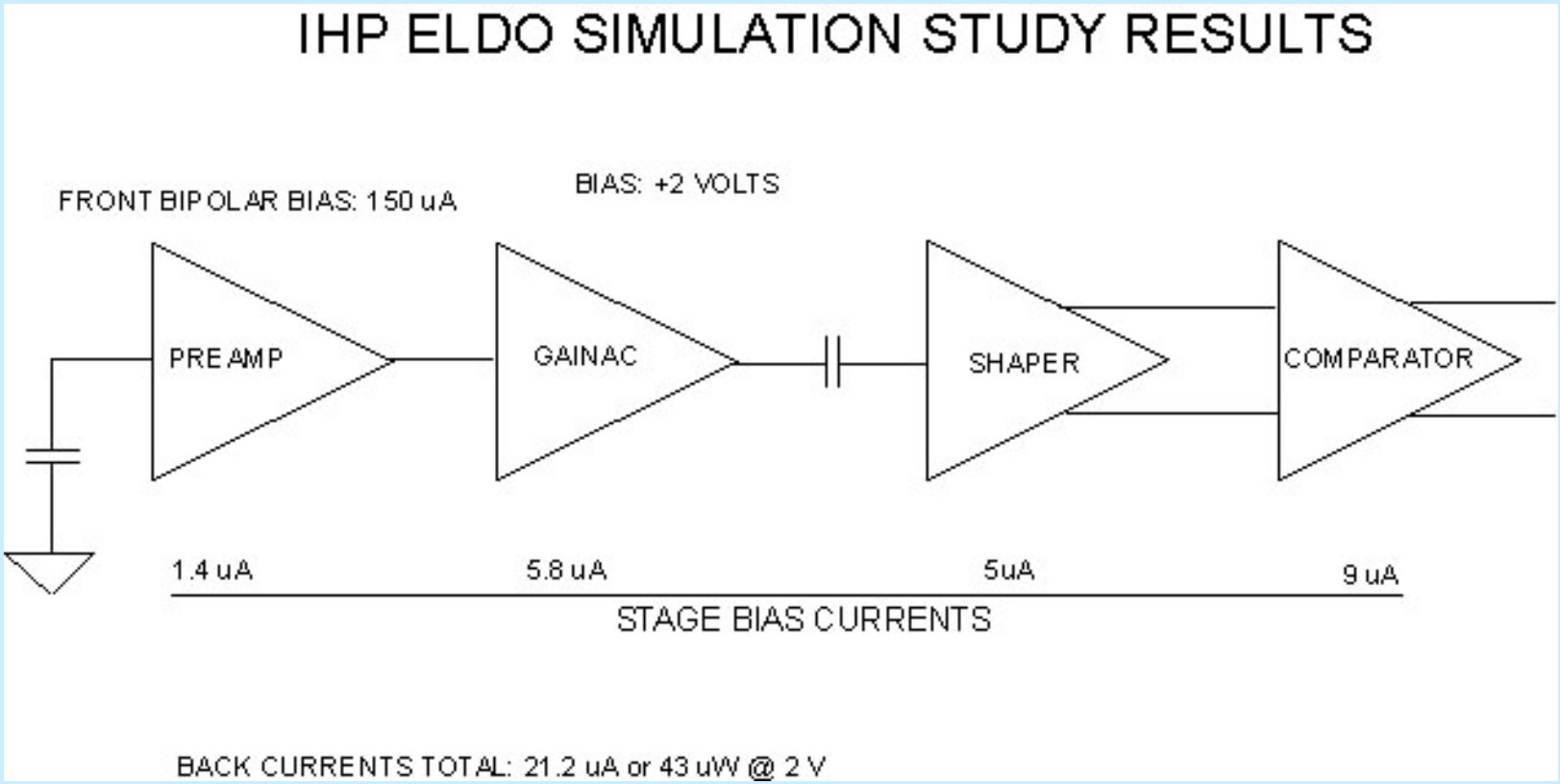
Fluence: 1.34E15 p/cm^2 (8.32x10^{14} n_{eq}/cm^2)
β=50

Transistor Size μm^2	I_c irrad	I_c anneal
0.5x1	3.E-05	1.E-07
0.5x2.5	7.E-05	4.E-06
0.5x10	4.E-04	9.E-06
0.5x20		6.E-05
4x5	1.E-04	1.E-05

At 3.5x10^{14} in the outer region (60 cm), where long (10 cm) silicon strip detectors with capacitances around 15pF will be used, the collector current I_c is low enough for substantial power savings over CMOS.

At 1.34x10^{15} closer to the mid radius (20 cm), where short (3 cm) silicon strip detectors with capacitance around 6pF will be used, the required collector current I_c is still only 5 – 10 μA. We expect even better results from 3rd generation IBM SiGe HBTs.

Frontend Simulation Results



First Guess at Potential Power Savings

Using simulation of first SiGe frontend, an estimate for power can be obtained. Compare to 0.25 μm CMOS design of J. Kaplon et al., 2004 IEEE.

CHIP TECHNOLOGY FEATURE	0.25 μm CMOS ABCDS/FE J. Kaplon et al., (IEEE Rome Oct 2004)		IHP SG25H1 SCT-FE Preliminary design	
Power: Bias for all but front transistor	330 μA	0.8 mW	= 30 μA (conservative)	.06 mW
Power: Front bias for 25 pF load	300 μA	0.75 mW	150 μA	0.30 mW
Power: Front bias for 7 pF load	120 μA	0.3 mW	50 μA	0.10 mW
Total Power (7 pF) $1x10^{15}$	1.1 mW		0.16mW	
Total Power (25 pF) $2x10^{14}$	1.5 mW		0.34mW	

Noise in Bipolar Transistors (H. G. Spieler):

$$Q_n^2 = i_n^2 F_i T_s + e_n^2 C_{tot}^2 \frac{F_v}{T_s}$$

$$C_{tot} = C_{det} + C_{in}$$

$$i_n^2 = 2q_e\left(\frac{I_c}{\beta} + I_{bias}\right)$$

$$e_n^2 = \frac{2(k_B T)^2}{q_e I_e} + 4kTr_{bb}$$

Temperature dependence of bias current ties the noise to the temperature management of the sLHC tracker, which is already complicated by annealing of leakage current and depletion voltage.

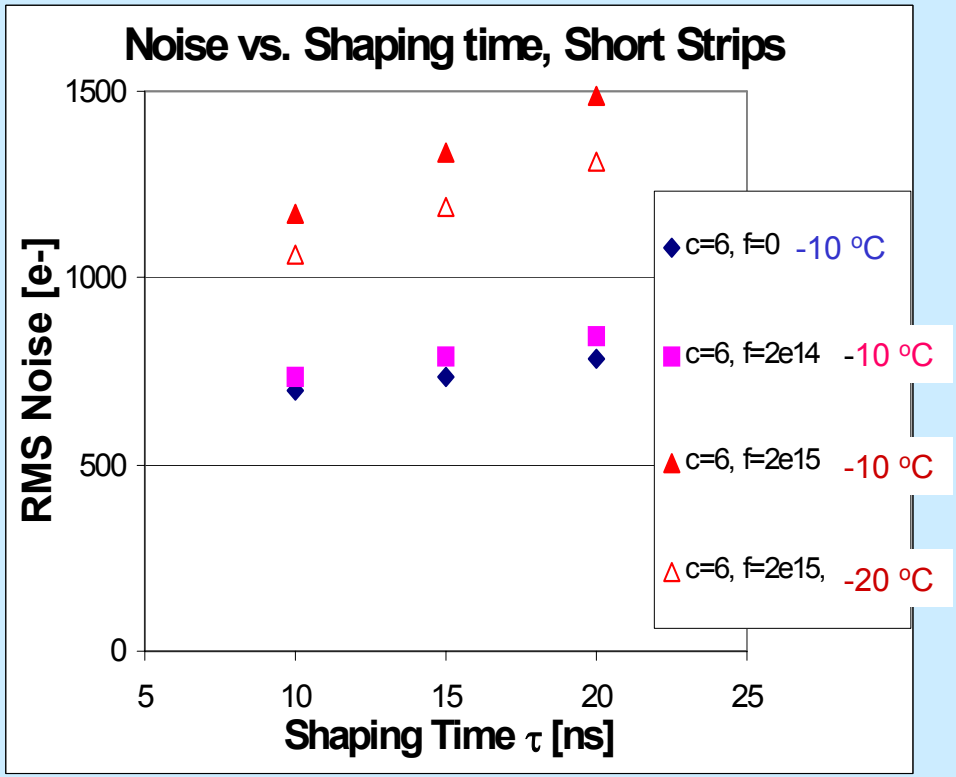
Noise depends on product of leakage current I_{Bias} and shaping time T_s

(applies to CMOS as well)

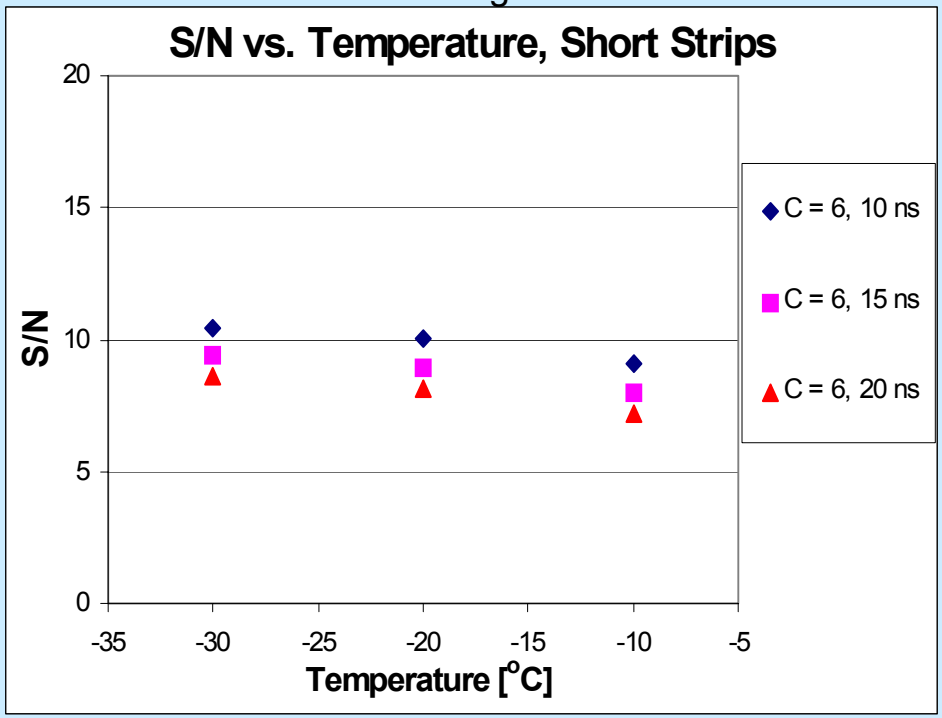
Short Strips Signal-to-Noise using SiGe Frontend

Electronic noise small, leakage current important →
Trade shaping time against operating temperature

Temperature: -10 °C vs.- 20 °C



Fixed Fluence:
$2.2 \cdot 10^{15}$ neq/cm^2 (short strips)
The maximum bias voltage is 600 V



Noise(20 ns & -20 °C) = Noise(15 ns & -10 °C)!

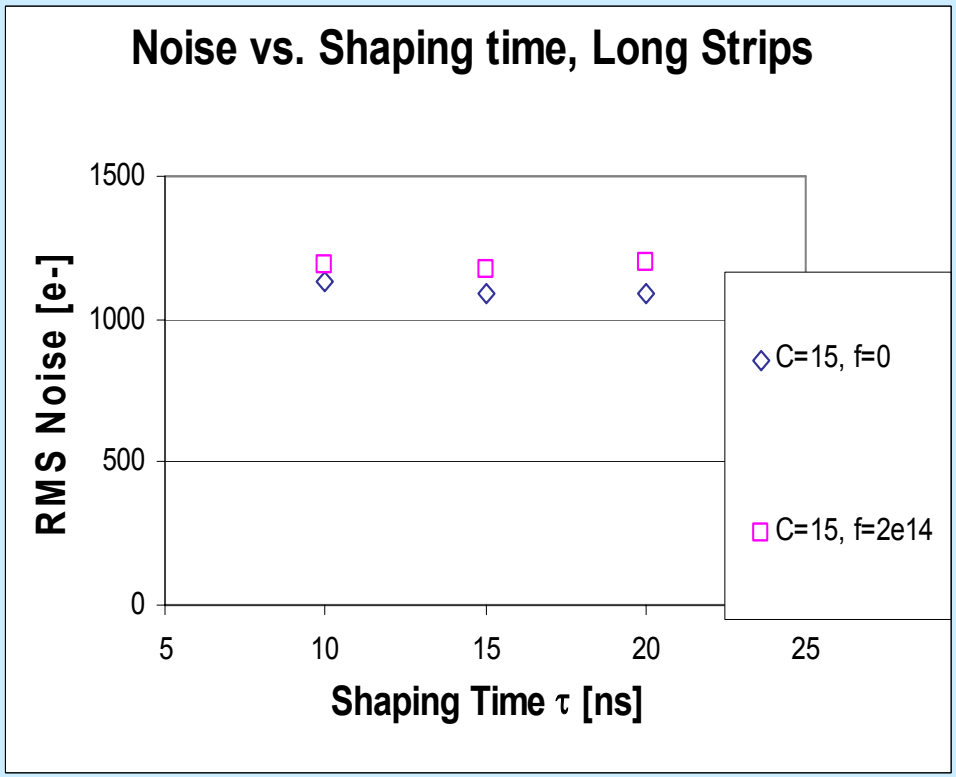
No advantage to very low temps!

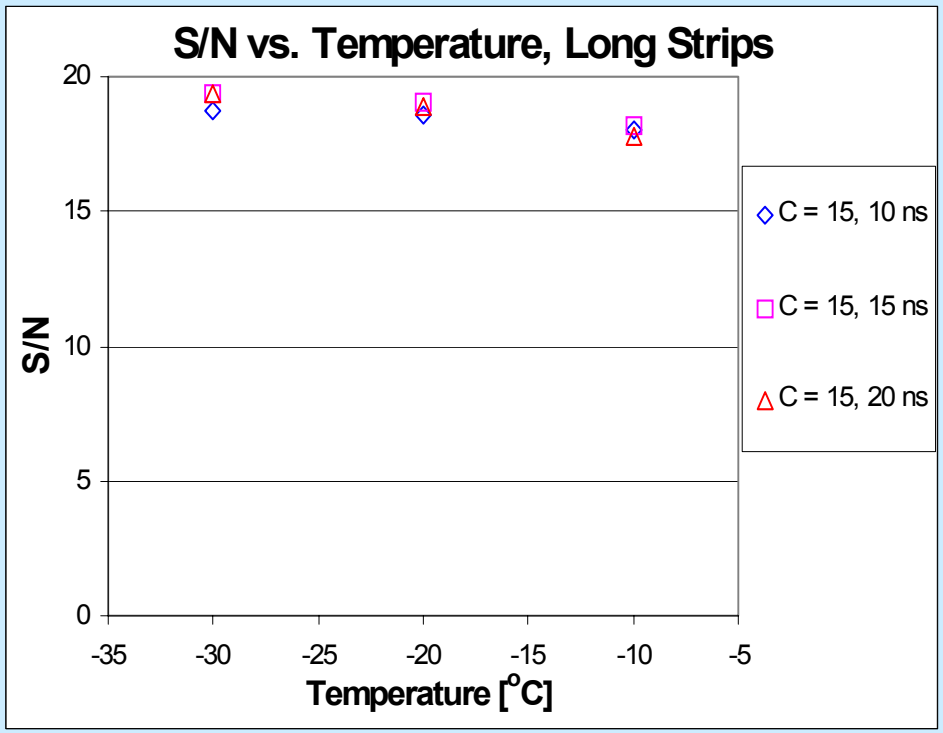
Long Strips Signal-to-Noise using SiGe Frontend

Electronic noise dominant, leakage current not so important →
Expect no sensitivity to shaping time or operating temperature

Temperature: -10 °C

Fixed Fluence:
$2.2 \cdot 10^{14}$ neq/cm^2 (long strips)
The maximum bias voltage is 600 V





Noise at -10 °C and 20 ns acceptable!

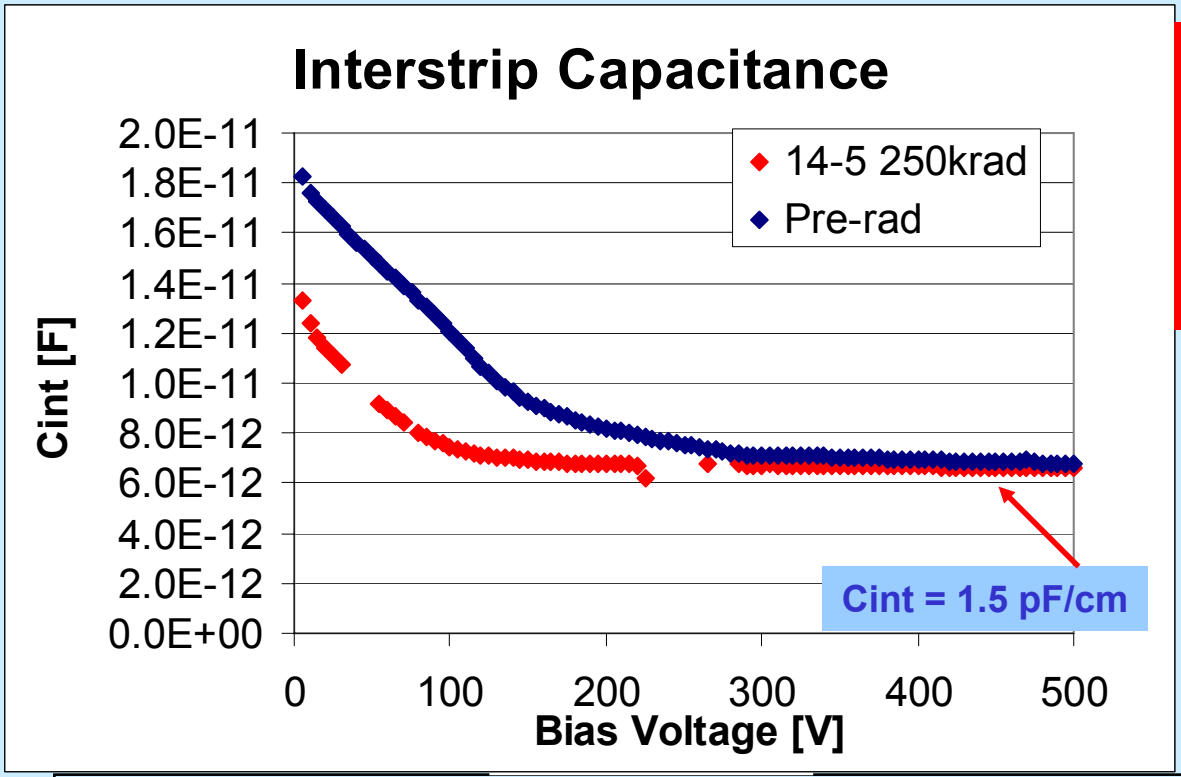
No advantage to very low temps!

Inter-strip Capacitance

One of the most important sensor parameters contributing to the S/N ratio

Depends on the width/pitch ratio of the strips and on the isolation technique (p-stops, p-spray).

SMART reported large bias dependence on p-type detectors, due to accumulation layer.



Irradiation with ^{60}Co (250 krad) reduces the bias dependence, as expected (c.f. talk by C. Piemonte)

SMART 14-5
p-type FZ
low-dose spray
w/p = 15/50
V_{dep} = 85 V
(I. Henderson, J. Wray, D. Larson, SCIPP)

Expected Performance for p-type SSD

Details in : "Operation of Short-Strip Silicon Detectors based on p-type Wafers in the ATLAS Upgrade ID
M. Bruzzi, H.F.-W. Sadrozinski, A. Seiden, SCIPP 05/09

Conservative Assumptions:

$\alpha_p = 2.5 \cdot 10^{-17}$ A/cm (only partial anneal)

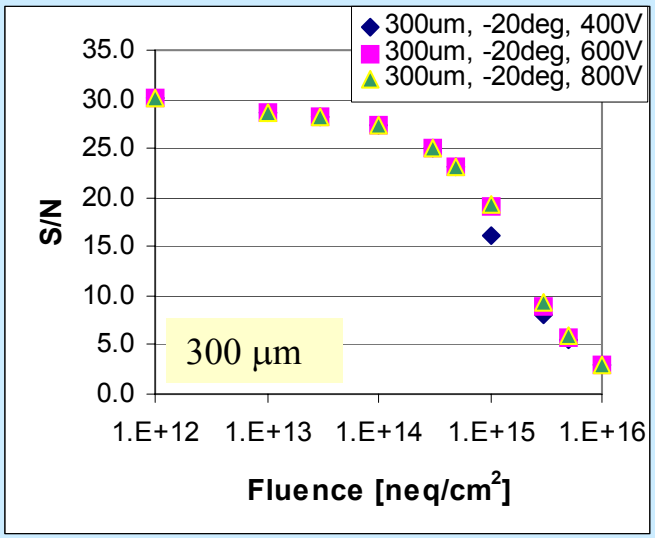
$C_{total} = 2$ pF/cm

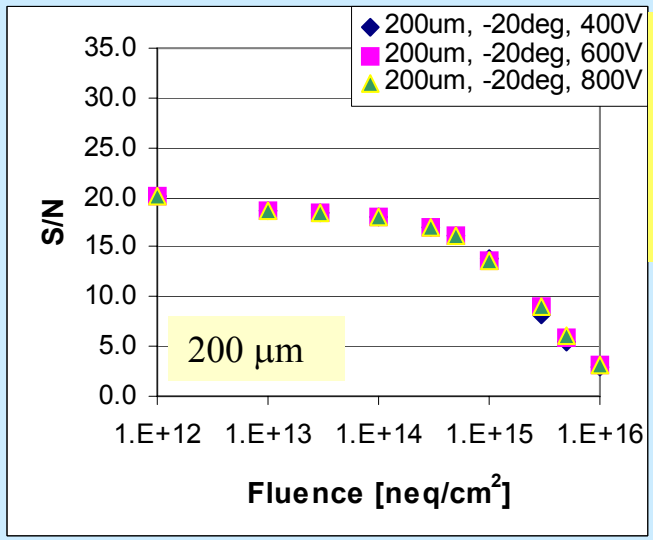
$V_{dep} = 160V + \beta * \Phi$ (with $2.7 * 10^{-13}$ V/cm^2) (no anneal)

$(= 600V \ @ \ \Phi = 10^{16}$ neq/ cm^2)

$\sigma^2_{Noise} = (A + B \cdot C)^2 + (2 \cdot I \cdot \tau_s)/q \quad A = 500, B = 60$

S/N for short strips vs. fluence for different bias voltages:





no need for thin detectors, unless n-type: depletion vs. trapping 600V seems to be sufficient

do need

update on fluences