Available online at www.sciencedirect.com
SCIENCE DIRECT®
ELSEVIER
Nuclear Instruments and Methods in Physics Research A 541 (2005) 29–39
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

Design and properties of the GLAST flight silicon micro-strip sensors

T. Ohsugi[a,*], S. Yoshida[a], Y. Fukazawa[a], K. Yamamura[b], K. Sato[b], K. Yamamoto[b], Hartmut F.-W. Sadrozinski[c], the GLAST-LAT collaboration

[a]*Department of Physics, Hiroshima University, Higashi-Hiroshima 739-8526, Japan*
[b]*Hamamatsu Photonics (HPK), Hamamatsu 435, Japan*
[c]*SCIPP, University of California Santa Cruz, CA 95064, USA*

Available online 11 March 2005

Abstract

We have designed and developed the flight model silicon micro-strip detector (FM-SSD) for Large Area Space Telescope (GLAST). The concepts and details of the sensor design are described and the results of production testing of the SSDs are reported. A total of 11,500 FM-SSDs were produced in the 2-yr time span from the start of 2001 to the end of 2003. The fabrication was done on the 6-in process line at Hamamatsu Photonics Company. The properties of each SSD were determined by measuring a set of specific parameters. The leakage current and dead channel rate establish a new performance standard for SSD mass production, indicating that the SSD design and fabrication technologies have been well optimized and are well matured.

1. Introduction

The next generation gamma-ray space telescope following the successful CGRO mission [1] will be the Large Area Space Telescope (GLAST). The GLAST mission will consist of the Large Area Telescope (LAT) and GLAST Burst Monitor (GBM). The LAT [2] is designed to detect cosmic gamma-rays in the energy range of 30 MeV to over 300 GeV. Like EGRET [3] on CGRO, the LAT will detect gamma-rays by converting them into electron–positron pairs and tracking the trajectories of the charged particles to determine the direction of the gamma-ray, employing an electromagnetic calorimeter to measure their energies. In order to determine the conversion point and evaluate the incident direction of gamma-rays impinging on the LAT, the trajectories of the electron and positron produced by the gamma conversion and the position of the ensuing shower have to be measured with high precision. Silicon strip detectors (SSDs) have been selected as the tracking medium of the precision tracker because of their excellent position resolution, high

*Corresponding author.
E-mail address: ohsugi@hirax7.hepl.hiroshima-u.ac.jp (T. Ohsugi).

0168-9002/$ - see front matter © 2005 Elsevier B.V. All rights reserved.
doi:10.1016/j.nima.2005.01.035

detection efficiency, high-speed signal response, wide angular sensitivity and their high and sustainable reliability of operation, making them ideally suited for space application.

The GLAST flight model silicon micro-strip detector (FM-SSD) is a single-sided silicon micro-strip sensor. Two-dimensional information is gained by rotating alternate layers by 90°. The GLAST silicon tracker pioneered the use of 6″ high-resistivity wafers instead of the previous 4″ technology, which reduces the amount of assembly needed to construct the LAT tracker consisting of close to $80\,m^2$ of FM-SSD. In addition, using fewer and larger sensors results in increased reliability and reduced cost when fabrication is done in a modern and reliable processing line. The GLAST sensors were developed in collaboration with Hamamatsu Photonics Company (HPK) for a newly installed 6″ line. In order to guarantee reliable operation in space, the layout has been optimized to reduce high field regions, which could lead to micro-discharge [4] and/or high leakage current. Since the LAT tracker [5] combines four sensors to "ladders" close to 36 cm long strips, the strip capacitance and the resistance of the metal readout strips had to be minimized, and the coupling capacitance and bias resistance maximized.

Below, we will report in detail the design concepts of the GLAST-FM-SSD, including the "per lot" fabrication monitoring data of the circuit parts on test structures. Then our method of tracking the quality of fabrication with gamma-ray irradiation will be discussed. Finally, we report the data from measurements of SSD characteristics important for space applications. The data cover the entire run of 11,500 GLAST-FM-SSD, and results for the leakage current (which is considered the most important indicator of process quality), depletion voltage, and the dead channel rate are shown.

2. Design concept of the silicon micro-strip sensors

The SSD for the GLAST-LAT is a single-sided, AC-coupled sensor with P-strip on an $<100>$ N-type substrate [6]. Specifications for selected parameters of the GLAST-FM-SSD are listed in Table 1. The picture of the processed wafer is shown in Fig. 1, with the approximately 9 cm × 9 cm flight SSD in the center, surrounded by many test structures.

Table 1
Specifications of the GLAST-Flight-Model SSD

Items	Specifications (units)
Outer dimensions	$89{,}500 \pm 20 \times 89{,}500 \pm 20$ (μm^2)
Active area	$87{,}552 \times 87{,}552$ (μm^2)
Substrate thickness	410 ± 10 (μm)
Strip pitch	228 (μm)
Number of strips	384
Width of implant-strip	56 (μm)
Width of Al readout electrode	64 (μm)
Resistance of implant-strip	<30 (kΩ/cm)
Resistance of Al readout electrode	<50 (Ω/strip)
Full depletion voltage	<120 (V)
Resistance of isolation resistor (variation within a chip)	50 ± 30 (MΩ)
	± 10 (MΩ)
Capacitance of coupling capacitor (at 10 kHz)	>500 (pF)
Leakage current	
(at $V_b = 150$ V)	<500 (nA)
(at $V_b = 200$ V)	<600 (nA)
Bad channel rate (average)	<0.2 (%)
Bad channels allowed in a chip	$\leqslant 3$ (number of strips)

2.1. Strip design

The strip pitch of the GLAST-FM-SSD is constrained by a compromise between the physics requirements and the maximum number of allowed readout channels derived from the power load limitation of the GLAST satellite. The required low readout capacitance for the planned long strip assembly of ganged SSDs can only be satisfied by a narrow strip width [7], but this is limited by the desire to keep the electric field low at the implants to avoid micro-discharge. A strip pitch of 228 μm with a strip implant width of 56 μm was chosen. High electric fields can occur on the two ends of the strips. Hence, we have taken further steps to reduce the risks of having micro-discharge and at the same time achieve a low

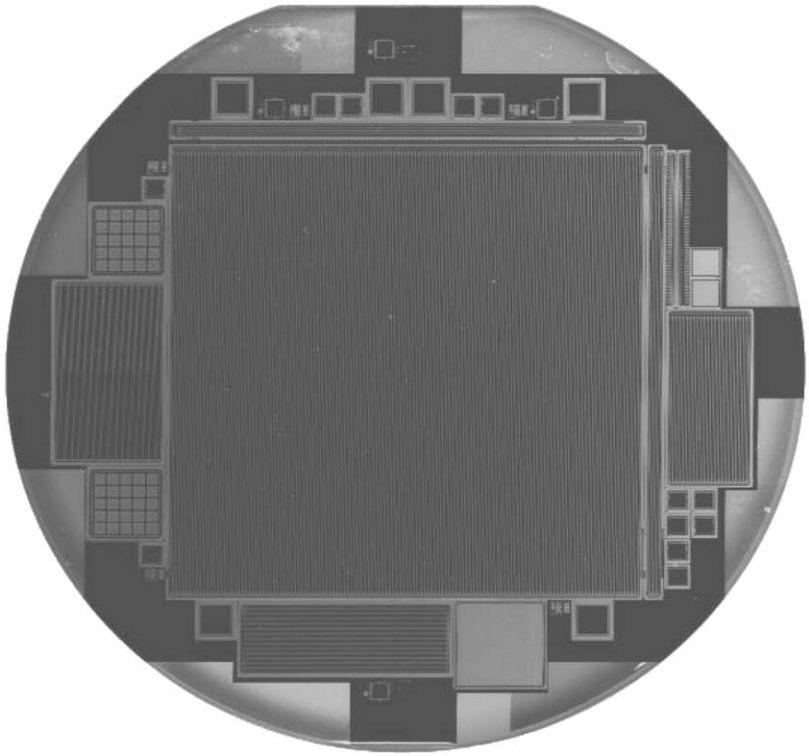

Fig. 1. Picture of the 6″ wafer processed by HPK for GLAST. The central square shape part is the GLAST-FM-SSD. Among the various test structures are (on the right-hand side) the full length "skinny" and large area "baby" test SSDs, which are used in the process monitoring.

readout capacitance. We have calculated the field at the strip edge as a function of the implant-strip width and the bias potential. We have confirmed that the field strength is safely below the breakdown field of silicon if the strip has a deep implant of more than 1 μm. To make the safety margin larger, the Al readout electrode is chosen to be 64 μm wide, covering the strip edges with a 4 μm overhang. The Al overhang structure is effective in preventing the micro-discharge at the edges when Al readout electrode and implant-strip have the same potential [8]. In addition, the strip ends have been contoured with a "hammer-head-like" shape as shown in Fig. 2. They have been designed this way in order to make the minimum curvature sufficiently large and to make the maximum field as low as possible at the strip ends. This shape could also improve the definition of the sensitive boundary between the strips and the bias ring.

2.2. Biasing resistor

The design and structure of the silicon strip sensor are based on an R&D program done in collaboration with the HPK [9]. A poly-silicon resistor is selected as the most reliable method of biasing and isolating each strip. A doped poly-silicon meandering "zigzag" line with 5 μm width (line itself is not visible in the Fig. 2) gives the desired resistance value of 50 MΩ. Since the bias resistors are implemented inside the bias ring, the sensitive area has been maximized while the insensitive edge zone has been minimized by extending the implant-strip toward the bias ring underneath the poly-silicon bias resistor as shown in Fig. 2. This part of the strip (length < 1 mm) is not covered by the Al readout electrode but the generated signals can propagate along the sufficiently short strip implant to the region covered by

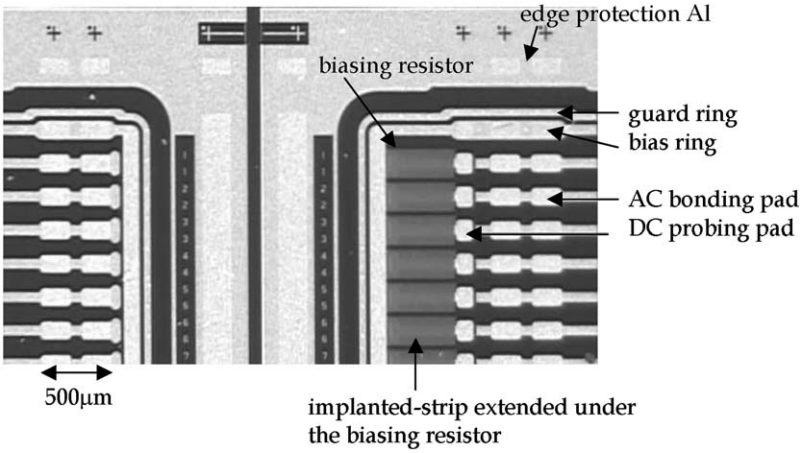

Fig. 2. Picture of corners of two SSDs aligned for wire bonding. Various alignment fiducials are seen, as well as the aluminized edge protection (''rim structure'') including the substrate contact strip, the guard and bias rings and the double row of AC bonding pads. Important features of the SSD include ''hammer-head'' end of strips (left and right), implants extended underneath the resistors (right) and DC probe pads (right).

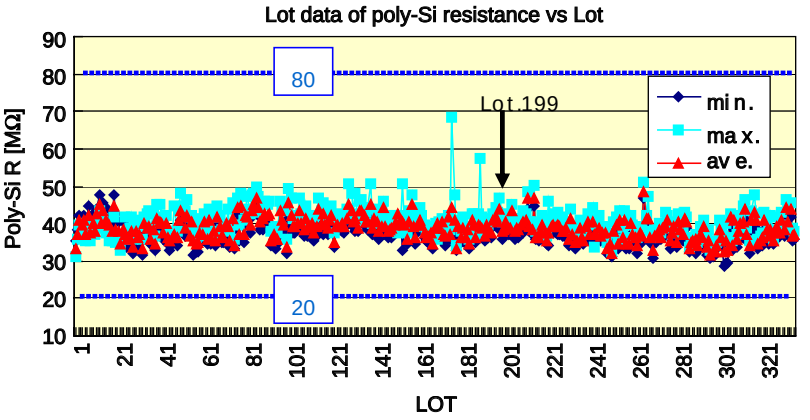

Fig. 3. Distribution of resistance values of the biasing resistors vs. lot number. The maximum, minimum and average resistor values are shown, as well as the specified upper and lower limits.

the Al electrode. Since the resistance of implant-strip is controlled to be less than 30 kΩ/cm, the signal attenuation in this part is negligibly small.

Fig. 3 shows the lot-by-lot variation of the bias resistance from a sample of 88 resistors from four wafers per lot. The means cluster around the value of 40 MΩ with very good uniformity of between 1 and 3 MΩ within one lot. The distribution fits very well within the specified band between 20 and 80 MΩ indicated in Fig. 3.

2.3. AC coupling capacitor

The AC coupling capacitor is integrated on top of each strip. The thin dielectric layer of the AC coupling capacitor has been made as a double-layer structure of SiO_2 and Si_3N_4 to achieve good production yields [10]. The thickness of each layer has been chosen as a compromise between large coupling capacitance and good yield with sufficiently high breakdown voltage of the capacitor.

A thinner insulating layer gives a larger coupling capacitance with associated improved signal strength, but has a higher risk of punch through and breakdown. The breakdown voltage of the coupling capacitor is designed to be more than 200 V, although we plan to bias the implant-strips at ground and to apply a smaller potential of about 120 V to the back plane. Fig. 4 shows the lot-by-lot distribution of the coupling capacitance, where the two outside and one center strips in a full-length "skinny" test detector are measured on two wafers per lot. The achieved average value of 580 pF is comfortably above the specified minimum value of 500 pF.

2.4. Pure Al readout electrode

A thick pure aluminum electrode has been developed to achieve a low readout resistance in the long configuration of narrow strips. For long-term operation in space, a pure aluminum electrode on SiO_2 dielectric could have a migration problem which could cause the coupling capacitor to break down. In our design, the Si_3N_4 layer prevents migration of Al into the SiO_2 coupling layer. This thick pure aluminum is also essential for the reliability and ease of wire-bonding which will be discussed in the next section. The lot-by-lot variation of the resistance of the Al electrode is shown in Fig. 5, using the same sample as for the coupling capacitance.

2.5. Bonding pads

The bonding pads need special attention because ultrasonic wire bonding, the most popular method in connecting the readout electronics and biasing connections, can exert mechanical stresses on the SSD. There are many bond pads on the micro-electronics chip, but they tend to be in inactive areas, in distinction to the SSD, where, to use the detector area effectively, an equally large number of bond pads need to be within the active area, and are actually on top of the implants and the thin dielectric of the coupling capacitors. In order to make such a thin structure robust against bonding shocks, we have developed a multi-layer structure underneath the pure Al bonding pad. The soft and thick ($>1\,\mu m$) Al layer has an important role to absorb bonding shocks. It also guarantees good bonding properties. We have implemented a pair of bonding pads on each strip which provides flexibility in separating the location of probing and bonding, and low-risk re-bonding.

2.6. Probing pads

A DC probing pad of sufficiently large size for automated probing is implemented on each strip implant for wafer testing of the coupling capacitors and integrity of the biasing connection. No current measurement was performed on individual strips because of the tight specifications on the

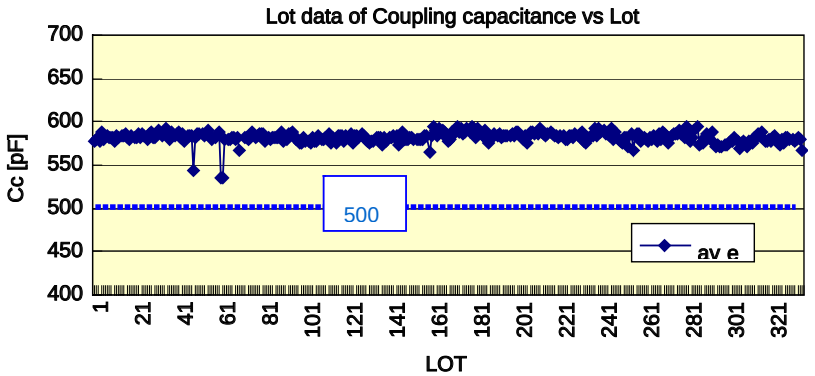

Fig. 4. Distribution of coupling capacitance values vs. lot number with the lower allowed limit indicated. A total of 2010 are displayed (3 strips/SSD × 2 SSD/lot × 325 lots).

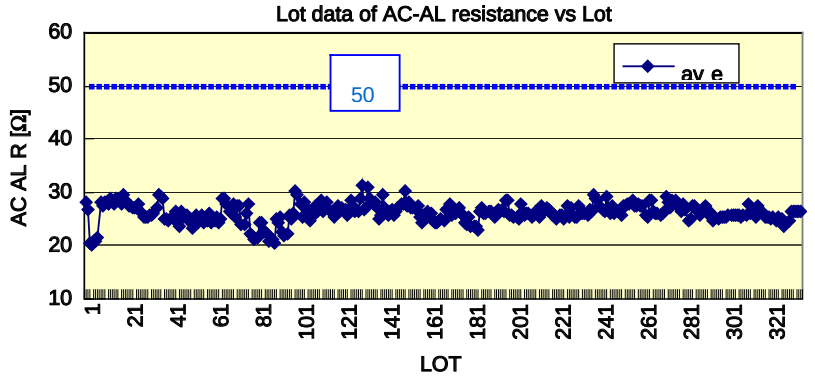

Fig. 5. Distribution of resistance values of the Al readout trace vs. lot number, with a maximum allowed value indicated. A total of 2010 are displayed (3 strips/SSD × 2 SSD/lot × 325 lots).

total SSD current. In addition, a substrate contact strip is implemented across the detector close to the edge for easy automated probing. Each coupling capacitor has been tested by supplying 100 V potential between this substrate contact strip and the AC pad.

2.7. Bias ring and guard ring

A biasing ring has the double function to supply the bias potential to the strip and to absorb the leakage current outside the bias ring. In addition, we have implemented a single floating-guard-ring to relax the edge field strength of the bias ring [10]. In order to minimize the insensitive area at the detector edge, we choose a single guard-ring structure. The potential of the floating electrode will automatically be adjusted by the leakage current and prevent breakdown and micro-discharge. Both rings have a DC-coupled Al electrode, which overhangs the implants by 10 μm to prevent micro-discharge at the strip edge [4].

2.8. Rim structure

The rim area is defined as the area outside the guard ring. Since the rim area is insensitive to the detection of particles, we should minimize the rim area. In cutting the SSD rim from wafer, we have used the most popular cutting device which is the diamond saw. The diamond-saw cutting introduces many micro-cracks along the cutting edge. Thus, the edge is sensitive to high leakage currents and breakdown if the field is applied. Newly developed laser cutting has much better accuracy and leaves the edge in much better physical and electrical condition, but it is still in the development stage.

The surface of the rim insensitive area is covered with n^+ implant and thin Al deposited over the n^+ implant. This structure is introduced primarily for minimizing surface leakage current as well as the leakage current at the cutting edge. The Al cover also suppresses the chipping off along the cutting edges. One may be concerned about the distance between the p^+ guard ring and the n^+ edge implant, which may be sensitive to breakdown at the guard-ring edge. The required distance is a function of the operating bias voltage and the thickness of the substrate. In this case we choose a distance of 150 μm, which is safe against micro-discharge up to several hundred volts. The Al covering the n^+ rim area contains many alignment marks and fiducials as mentioned below.

2.9. Distance from the sensitive edge to the sensor rim

There is no definite procedure to evaluate the safe distance between the cutting line to the bias ring, depending on the operation bias voltage, the substrate thickness, the guard-ring structure, the

rim structure and the cutting technology for the sensor rim. The most sensitive item in designing the sensor rim is in confining the electric field generated by the bias voltage not to reach the micro-cracks introduced by dicing. Our guiding principle in defining the edge distance is such that the distance should be more than twice the substrate thickness. For the GLAST-FM-SSD, we have pushed more aggressively toward the edge and have set $710 \pm 20\,\mu m$ from the edge of the guard ring to the detector edge. A micro-crack-free dicing technology using laser cutter may reduce the distance to the substrate thickness if the cutting plane can be doped with n^+.

2.10. Pattern accuracy

The patterns implanted or deposited on the SSD produced by the HPK silicon processing unit have a typical error in size and location of less than $0.5\,\mu m$. This error is caused by both the accuracy of the mask pattern and the mask mis-alignment. Simulations of the electric field on the implants using differing pattern accuracy convinced us that even for the large-pitch SSD like GLAST this pattern accuracy is required to prevent excessive fields on the strip implants.

2.11. Dicing accuracy

The dicing accuracy plays an important role in planning the assembly method. Given the accuracy in placing the pattern on the wafer mentioned before, the position of the SSD structures relative to the edge is determined by the dicing accuracy. The dicing error will result from two sources: translation (i.e. the distance from the scribe line to the cut edge) and rotation (i.e. the angle between the scribe lines and the edges). Here, we define the dicing error as the largest distance of a corner from its scribe line. The measurements were done on a sample of 1685 SSD, i.e. on about $\frac{1}{10}$ of all SSD, with high sample rate for the initial lots. As seen in Fig. 6, the dicing accuracy is excellent, with a mean of about $4\,\mu m$ and with no SSD with more than $9\,\mu m$. This is an important result for GLAST, because it allows the use of completely mechanical assembly methods in the ladder production.

2.12. Surface passivation

A passivation layer for the protection of the SSD surface is extremely important for two principal reasons: one is to prevent a contamination of the structures from chemicals like sodium. Sodium ions are attracted by the electric field and build up around the strip edge, which lowers the breakdown voltage of micro-discharge, and can lead to increased sensitivity to radiation damage. The other obvious reason for having a hard passivation is to avoid mechanical scratches during the handling of the SSD. The material used for passivation of the GLAST-FM-SSD is silicon-oxide which is highly insulating and very hard.

2.13. Monitoring structures

Besides the FM-SSD, several monitoring structures have been implemented on each wafer, as indicated in Fig. 1. The "skinny" SSD has the same structure including full-length strips as the FM-SSD but has only eight instead of 384 channels. It has been used in the evaluation of process parameters as mentioned above, and in the gamma-ray irradiation test described in the following. The small "baby" sensor ($3.5\,cm \times 1.5\,cm$) has a structure identical to the FM-SSD and it has been included to perform charge collection testing. Other structures are a bonding pad array for bonding test, photo-diodes and poly-silicon resistors to monitor the resistance variation.

2.14. Fiducials and alignment marks

Various alignment marks and fiducials have been printed onto the Al surface of the rim area where n^+ has been implanted. These include the ID number and other marks for easy and automatic positioning and alignment of the SSD needed in ladder production where the strips of four SSD are aligned and bonded up. Some of these are visible in the detailed picture of the edge of the SSD in Fig. 2.

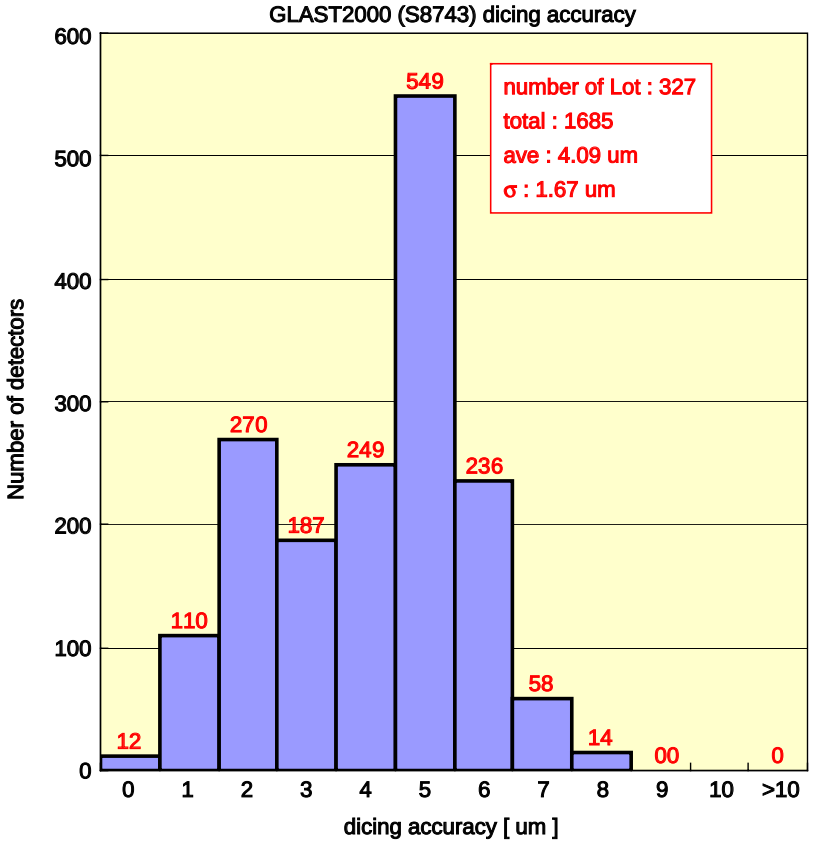

Fig. 6. Dicing accuracy showing a mean of 4 μm.

3. Production monitoring with irradiation

In each production lot (50 wafers), one skinny detector has been sampled and irradiated by ^{60}Co gamma-rays to a total ionizing dose (TID) of 10 krad. The idea behind this test is the observation that damage by gamma-ray irradiation is sensitive to the surface quality, i.e. the quality of processing and contaminations. The contamination tends to trap the holes generated by irradiation and these charge up the SiO_2. Then the high field due to the chargeup around the p^+ strip leads to increased leakage current. A typical current–dose relation measured up to a dose of 50 krad is depicted in Fig. 7. The current density as a function of dose is given by

$$i/A = 5.3 + 4.7D - 0.025D^2$$

(with the current density i/A in nA/cm^2 and the dose D in krad), indicating a linear behavior at a lower dose and a gradual saturation at a higher dose. The expectation is that if a contamination would have occurred, the irradiation sensitivity of the leakage current would be significantly larger. The acceptable limit for the radiation-induced leakage current is set at 150 nA/cm^2 for 10 krad. In Fig. 8, the leakage current after a TID of 10 krad has been plotted against the initial current. We do not see any strong correlation between these two quantities so that none of the processing lots have been rejected based on this test. In addition to TID testing, the sensors were subjected to heavy ion testing to investigate single-event effects (SEE). No SEE failures were observed [11].

4. Characteristic properties of the SSD

Initial results from SSD testing during fabrication have been published earlier [12]. Here,

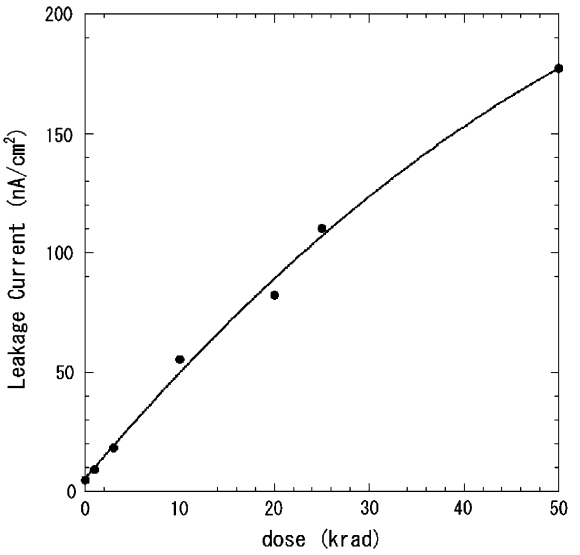

Fig. 7. Leakage current vs. total dose of the test chip irradiated by ^{60}Co gamma-rays.

we report the data from the complete testing of the entire fabrication run of 11,500 GLAST-FM-SSD.

4.1. Leakage current

The leakage current is customarily taken as a measure of the processing quality of the SSD. Most of the initial leakage current is generated at the deep energy levels located in the forbidden band, which could be introduced by surface damage during processing. The initial leakage current distribution after dicing is shown in Fig. 9. The current was measured by applying a positive bias voltage of 150 V to the back-plane, with the bias ring connected to the ground of the power supply and the single guard-ring floating. The achieved average leakage current of about 3 nA/cm^2 is comparable to the current levels for the best photo-diodes of about 1 nA/cm^2. Taking into account the long strip edges in SSDs, this is

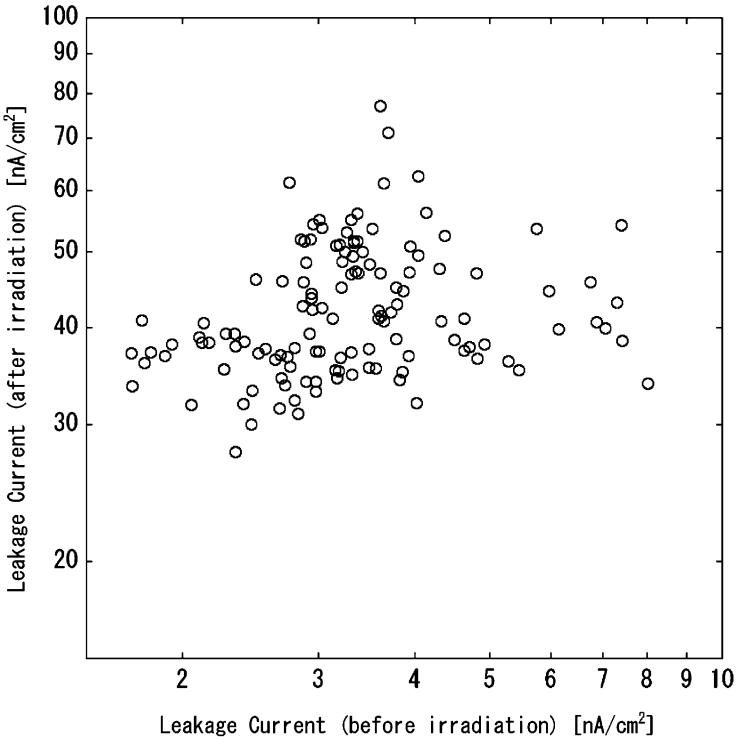

Fig. 8. Leakage current scatter plot: the current after irradiation with 10 krad ^{60}Co gamma-rays vs. the initial current.

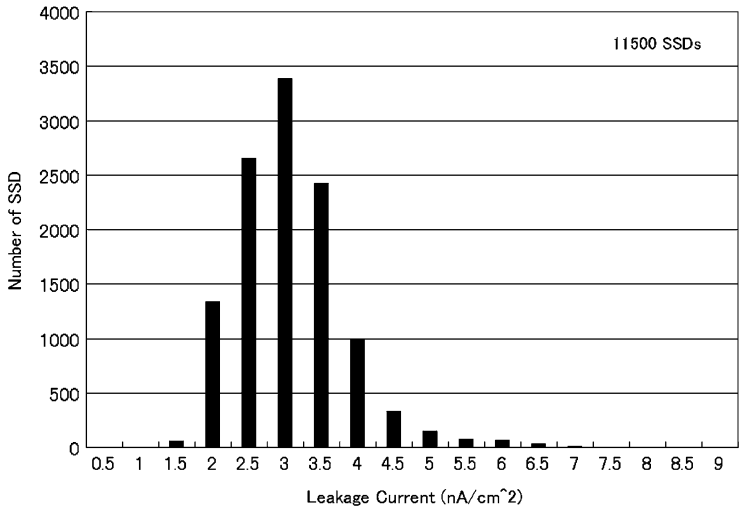

Fig. 9. Distribution of the initial leakage current per unit area.

close to ideal performance one could expect for micro-strip detectors.

4.2. Full depletion voltage and wafer resistivity

The full depletion voltage has been evaluated from the capacitance–bias voltage (C–V) curves taken in 5 V steps. The depletion voltage is the voltage where ($1/C^2$) saturates as a function of bias voltage (V_b). The capacitance is inversely proportional to depletion depth d and the depletion depth is proportional to the square root of V_b. At full depletion, the capacitance becomes constant because the depleted region is equal to the detector thickness. The distribution of full depletion voltages is shown in Fig. 10. The distribution peaks at about 65 V, and is cut off at 120 V, which is the specified maximum depletion voltage. Because the thickness of the wafer is well controlled, the width of the distribution reflects the spread in resistivity of presently available highly resistive 6″ wafers that are not yet well controlled at the crystal production stage.

4.3. Onset voltage of micro-discharge

We have specified the onset voltage of micro-discharge to be above 200 V. For every flight sensor, the leakage current was measured as a function of the bias voltage (I–V curve) up to 200 V and no indication of micro-discharge was observed.

4.4. Bad channel statistics

A total of 436 dead channels has been found, which is 0.01% of the total number of over 4.4 million channels and is about a factor of 20 lower than the specified value of 0.2%. These dead channels can be classified into the following three categories: bad implant-strip and/or bad bias resistor, short-circuited AC coupling capacitor and bad readout Al electrode. The first one consists of open (non-continuous) implant-strips, shorted out adjacent implant-strips and disconnected bias resistors. The third one includes both open (non-continuous) Al electrodes and shorted out adjacent Al electrodes. Our result indicates that the first category is 57.5%, the second is 32.5% and the third is 10%. It is interesting to note that most of the SSDs (~97.5%) delivered are perfect, having no dead channel at all.

5. Summary and conclusions

We have designed and produced a total number of 11,500 GLAST-FM-SSD for the GLAST LAT. The performance characteristics are setting a new

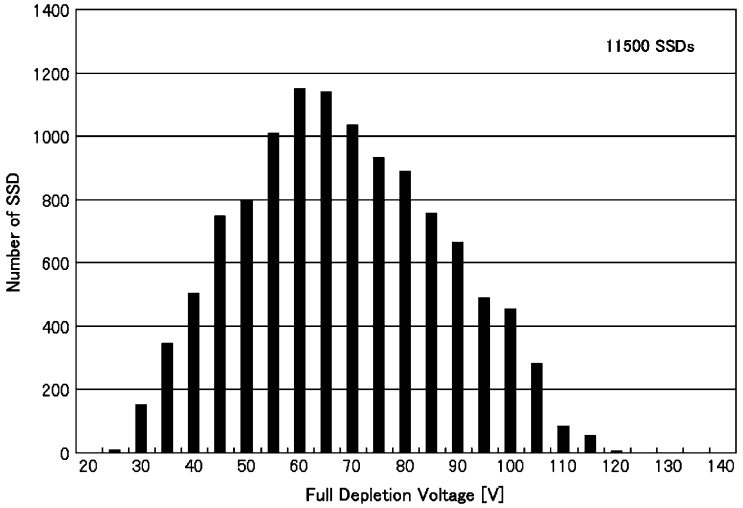

Fig. 10. Distribution of full depletion voltage for the 400 μm thick GLAST-Flight-Model SSDs.

standard for large-scale production of SSD: the typical leakage currents are 3 nA/cm^2, comparable to the best photo-diodes, and the dead channel rate is of the order of 0.01%, orders of magnitude lower than in previous projects. These results imply that the design of GLAST-FM-SSD and the silicon processing are well optimized and well tuned. In addition, they indicate that careful steps taken in the design to reduce the electric fields on implants are essential to reduce the leakage current and micro-discharge.

Acknowledgments

We would like to thank Mr. W. Althouse, Prof. R. Bellazzini, Prof. E. Bloom, Dr. T. Handa, Prof. R. Johnson, Prof. T. Kamae, Mr. T. Masuda, Dr. T. Mizuno, and Dr. C. Piemonte for their various contributions in the early stage of this work.

References

[1] The CGRO Mission, http://cossc.gsfc.nasa.gov/.
[2] P. Michelson, Proc. SPIE 4851 (2003) 1144.
[3] G. Kanbach, et al., Space Sci. Rev. 49 (1–2) (1988) 69.
[4] T. Ohsugi, et al., Nucl. Instr. and Meth. A 342 (1994) 22.
[5] R.P. Johnson, Proc. SPIE 4784 (2003) 288.
[6] T. Akimoto, et al., Nucl. Instr. and Meth. A 466 (2001) 354.
[7] E. Barberis, et al., Nucl. Instr. and Meth. A 342 (1994) 90.
[8] T. Ohsugi, et al., Nucl. Instr. and Meth. A 383 (1996) 116.
[9] T. Ohsugi, et al., Nucl. Instr. and Meth. A 342 (1994) 16.
[10] T. Ohsugi, et al., Nucl. Instr. and Meth. A 383 (1996) 166.
[11] S. Yoshida, et al., IEEE Trans. Nucl. Sci. NS-49 (2002) 1756.
[12] S. Yoshida, et al., IEEE Trans. Nucl. Sci. NS-49 (2002) 1017.