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Nuclear Instruments and Methods in Physics Research A 552 (2005) 1-6

www.elsevier.com/locate/nima

Tracking detectors for the LHC upgrade

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Available online 21 June 2005

Abstract

The plans for an upgrade of the Large Hadron Collider LHC to the Super-LHC (sLHC) are reviewed with special consideration of the environment for the inner tracking system. A straw-man detector upgrade for ATLAS is presented, which is motivated by the varying radiation levels as a function of radius, and choices for detector geometries and technologies are discussed in the context of required signal-to-threshold ratios. © 2005 Elsevier B.V. All rights reserved.

PACS: 29.30.Ay; 29.40.Gx; 29.40.Wk

Keywords: Silicon tracker; Super LHC; Radiation damage

1. Introduction

With the assembly of the detectors for the Large Hadron Collider LHC in full swing, a program for a future upgrade of the LHC is taking shape [1]. Machine studies have shown that a 10-fold luminosity increase might be possible, extending the physics reach of the LHC significantly [2]. While the experiments could collect an integrated luminosity of 250 fb^{-1} in the initial 6 years of data taking at the LHC, an upgrade, the SuperLHC (sLHC) could increase this number to about 2500 fb^{-1} in 4 years.

Given that it will take close to 10 years to develop a new detector from concept to switch-on,

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the planning has started for an upgrade to be ready for data taking in the 2015 time scale. In preparation for this, the RD50 collaboration [3–5] at CERN was formed in 2002 and is providing guidelines to the detector technologies, which might be employed at the anticipated high radiation levels.

2. Discovery potential of the sLHC

A practical view of the LHC upgrade is that it will be a necessity if the LHC science potential is to be exploited to the fullest. By the year 2015, the inner parts of the LHC detectors will have seen 8 years of beams and need to be replaced mainly because of radiation damage. The LHC discovery potential has an even shorter time span. According

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^{0168-9002/\$ -} see front matter 2005 Elsevier B.V. All rights reserved. doi:10.1016/j.nima.2005.05.038

to reasonable scenarios for the turn-on of the LHC, the time needed to halve the statistical error of the data will be 8 years in 2012, after only 2 years at full luminosity [6]. Even if the sLHC turns on in 2015 with a slow ramp-up in luminosity, the time to halve the statistical error of 7 years might be reached only a few years after the collider reached the full luminosity! Thus, the time of largest discovery potential is the few years after the accelerator has reached full luminosity. It is important that until 50% of the final integrated luminosity is collected, the detector preserves its peak performance.

For the detector upgrades, an R&D program needs to start in 2004 and last until 2009; followed by construction in 2010 to 2013, and installation in 2014. This is already a very aggressive plan based on the LHC experience. The two large detector groups, ATLAS and CMS, have held workshops to review requirements for an upgrade R&D program [7–9]. The detector upgrades will have to be preceded by detailed simulations of the radiation environment; although for the present analysis, a simple scaling-up of the environment based on the LHC case provides a good first look at what to expect.

3. Beam time structure of the sLHC

The LHC detectors and electronics have been optimized for a luminosity of $10^{34} \text{ cm}^2 \text{s}^{-1}$ and attempting to extend the operation to $10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ will cause severe problems for all of the subsystems.

The structure of the physics events are determined by the center-of-mass energy and will not change from the LHC (although the rate will increase), while the background in these events from minimum bias events will increase by a factor 10. A potentially helpful feature might be a shortened bunch spacing in phase 1 of the upgrade; from 25 to 12.5 ns. If the tracking systems can exploit this by shortening the shaping times, then the occupancies will increase "only" by a factor of 5. Studies are under way to explore new bipolar technologies based on SiGe for use with shorter shaping times and large capacitances [10,11]. Recently there have been studies, which cast into doubt the possibility of the shortened bunch spacing, potentially making this a moot point [12]. On the other side of the parameter space, the machine designers are looking at superbunches of 1 μ s length [13], which would provide a 1000 times increased particle flux within 25 ns when compared with the LHC. Such a high particle flux would most likely preclude the exploitation of the luminosity increase of the sLHC.

4. The ATLAS ID upgrade

For ATLAS [14], an upgrade means replacing the entire Inner Detector (ID): the Transition Radiation Tracker (TRT) at large radius will have prohibitively large occupancy, and the Semiconductor Tracker (SCT) and Pixel System at smaller radii will have reduced performance because of radiation damage to the sensors and front-end electronics. Similar to the CMS inner detector [15], the upgraded ID tracker would have about 200 m^2 of semiconductor detectors. ATLAS will have to develop reliable assembly methods like CMS, which maintains identical production systems at seven sites to produce $\sim 20,000$ modules [16]. Because of increased particle fluence, the search for rad-hard sensors, an optimization of the detector layout with respect to the radius, and increased granularity, which might require increased multiplexing, will be of highest priority.

An ATLAS Upgrade Steering Group has been formed, and there is an US-ATLAS ID Upgrade Program [17], which emphasizes long-term R&D topics including development of pixel readout electronics (deep sub-micron CMOS), silicon strip front-end electronics (bipolar SiGe), radiationhard silicon strip detectors (p-type short strip and 2-D SSD), 3-D pixel detectors and module integration.

5. Tracker layout in the ATLAS upgrade

Due to the 10-fold increase in overlapping minimum bias events the tracker layout is governed

by two considerations: a high instantaneous rate causing pile-up of tracks, and the integrated particle flux leading to radiation damage and nuclear activation. The high instantaneous rate (particle flux) dictates the detector geometry, while the integrated fluence dictates the detector technology.

Fig. 1 shows the expected radial fluence distribution for a sLHC detector after an integrated luminosity of 2500 fb⁻¹ [18]. The scaling with radius is $R^{-1.6}$, but this underestimates the fluence at large radii, because of the neutron contribution from the calorimeter. At a radius R = 5 cm, the fluence is about 10^{16} cm^{-2} , at R = 20 cm, it decreases to about 10^{15} cm⁻², and at R = 50 cm it is about 2×10^{14} cm⁻². This suggests three different regions for a tracker with different technologies and layouts [1,19] as in-1: an outer region dicated in Fig. at $55 \text{ cm} \leq R \leq 1 \text{ m}$ where the present SCT technology can be used, a middle region using short strips between $20 \,\mathrm{cm} \leq R \leq 55 \,\mathrm{cm}$, where present pixel detector technology might work [20], and an inner region with pixels at $6 \text{ cm} \leq R \leq 12 \text{ cm}$ requiring new sensor technology.



Fig. 1. The fluence for an integrated luminosity of 2500 fb^{-1} as a function of radius *R* (left scale) is based on the data of Ref. [18] in open squares, with a fit of the form $1150/R^{1.6}$ superposed. The anticipated signal-to-threshold ratios (right scale) from Table 1 for silicon detectors are shown in the proposed tracker regions with the initial value (*x*) and the one after an integrated luminosity of 2500 fb^{-1} (\diamondsuit).

The outer region comprising the largest area in the sLHC tracker could be covered by four layers of "long" silicon strip detectors (SSD), and a single coordinate measurement might be adequate. No sensor problems are expected for the outer region—if the detectors work at the LHC. The limited space for services for the outer region will require careful tradeoffs between detector length, front-end electronics power/noise and amount of multiplexing and granularity. A new bipolar technology like SiGe [10,11] could give an advantage, specially for short shaping times.

The mid-radius region would be covered by four layers of short strips, providing space points. The options are short SSD of about 3 cm length [10,21], with either small-angle stereo arrangement, as in the present SCT, or 2-D Interleaved Stripixel Detectors (ISD) [22]. The latter have the advantage that two-dimensional information is received from a single detector layer requiring only singlesided processing. Their disadvantage is the fact that the collected charge is split between two readout directions. Moreover, the ISDs are expected to have larger capacitances and thus increased noise when compared to ordinary SSD. Because of the shortened strip length, the signalto-noise ratio S/N might be adequate, but further research is needed to evaluate this.

The innermost region at R < 20 cm will be covered with 3 layers with pixel style readout, which will provide adequate pattern recognition. A very detailed layout of the pixel region for the upgraded CMS, including power consumption and cost, is provided in Ref. [20].

6. Expected tracker performance

Based on recent results on radiation hardness of detectors and on extrapolation of present performance of readout electronics (i.e. without drastic improvement), one can make an initial assessment of the detector performance in the three regions. The efficiency of the tracking system is governed by the signal-to-threshold ratio S/T, i.e. it depends both on the signal extracted from the detector, which is mainly a function of the fluence, and the noise level in the electronics, which depends on the

size of the detector element, which has to be controlled by the threshold.

6.1. Radiation damage in sensors

The work of RD50 [23] permits a first assessment of the suitable sensor technology in the three tracker regions. Both in the outer and mid-radius region, for radii larger than 20 cm, silicon strip detectors will be a robust and suitable detector technology. New measurement of the charge collection efficiency in 280 µm thick p-type SSD report that after a fluence of high energy protons of $7.5 \times 10^{15} \,\text{p/cm}^2$ (corresponding to about $4 \times 10^{15} n_{eq}/cm^2$, expected for 8 cm at the sLHC), the collected charge is $> 6500 \text{ e}^{-}$ [24]. Moreover, no detrimental anti-annealing has been observed [21], making p-type the detector substrate of choice. Like the more expensive n-on-n detectors [25], n-on-p detectors would give head room in the required operating voltage. They have no type inversion and allow operation with partially depleted sensors. The higher electron drift velocity in saturation will also be advantageous at the end of the life time when trapping is the limiting factor. Magnetic Czochralski (MCz) material is a good candidate for the wafer material, because it has a high oxygen content and is available in large wafers [26].

The detector performance inside a 20 cm radius is governed by trapping. Previous trapping time measurements on silicon were done after fluences of up to $10^{15} n_{eq}/cm^2$ [27,28]. The recent measurements of Ref. [24], and recent analyses of charge collection measurements on pixels [29] and epitaxial silicon detectors [30] indicate that the charge collection at very high fluence is larger than a simple linear extrapolation of the measured trapping times would predict. This means that the charge collection in planar silicon detectors at fairly high bias voltages might be sufficient for all but the inner-most pixel layer. At a 20 cm radius, one can expect a collected charge of about 14,000 e⁻, and as mentioned above, at a radius of 8 cm, one can expect a collected charge of $> 6000 e^{-1}$ [24].

A large degradation is expected for all planar detectors, because charge trapping limits the

collection region. A different approach is provided by the 3-D detectors [31,32] where charge generation and collection are de-coupled by implanting vertical columns in the wafer. Placed at a radius of 5 cm, the predicted charge collected will be about 10,000 e⁻ after a fluence of $1 \times 10^{16} n_{eq}/cm^2$. One potential issue is the existence of low-field regions between the cells, which could lead to "blind spots" in the detector. A proposed solution would be to tilt the detectors. It should be pointed out that there are no measurements of the charge collection of 3-D detectors at these high fluences, and one has to rely on extrapolations. Other new geometries investigated within RD50 are thinned [33] and epitaxial Si detectors [30] to achieve constant and low depletion voltage, limited leakage currents and high inversion fluences. The latter effect is achieved by means of low resistivity bulk material (typically 50–100 Ω cm), as the high initial shallow doping will shift type inversion to very high fluences. This precludes making the epi detectors much thicker. The charge collected from thin detectors is small both initially because of the small charge generated and after irradiation because of trapping.

The quest for alternative affordable substrates to replace silicon has not been successful up to now. Detectors based on diamond [34] and SiC [35,36] have less collected charge pre-rad than silicon detectors, yet they appear to suffer from trapping at high fluences like silicon detectors. In addition, the very high wafer costs is an impediment for large-scale application.

6.2. Threshold settings

The performance of the tracking system like occupancy, position and time resolution depend on the signal-to-noise ratio S/N. A practical parameter influenced by the S/N is the threshold T, which must be low enough relative to the signal for efficient detection of particles, and high enough relative to the noise for low occupancy and stable operation. Although the noise is expected to increase slightly with radiation, we will assume that the threshold can be kept constant during the sLHC operation, either because of sufficient head

Radius	Detector	Threshold (e ⁻)	Signal/threshold			Comment
			Pre-rad	After 1250fb^{-1}	After 2500fb^{-1}	
> 55	Long strips	6250	3.7	3.6	3.5	SCT [37]
20-55	Short strips	4400	5.3	3.9	3.2	n-on-p [24]
8	Thick pixel	2000	11.5	5.5	3.0	n-on-p [24]
5	Thin pixel	2000	3.0	~1.5	~ 1.0	Epi75µ [30]
5	3-D	2000	~11.5	~ 7.5	~ 5.0	100 µm cells

Table 1 Projected signal-to-threshold ratio for silicon detectors in the upgrade ID

The numbers for 3-D are extrapolations using data from Ref. [24].

room in the initial threshold setting or control of the temperature.

The threshold for long strips in the SCT is $T = 1 \text{ fC} = 6250 \text{ e}^-$ [37], and one can expect that the upgrade tracker will be designed to operate with the same threshold. This is about 1/4 of the most probable signal, allowing for efficient track detection even if the signal is at the low end of the Landau distribution and the charge is shared between strips. Because of their reduced capacitance, short strips might be operated a with threshold of 70% of the canonical 1 fC number, i.e. 4400 e⁻.

For LHC pixel systems, the thresholds are tuned to $2500-3000 e^-$, at a noise level of $200-300 e^-$ [28,38–40]. This indicates that stability and matching (overcome with special threshold DACs) play a major role in the setting of the pixel thresholds, and one might count on only a small decrease of the pixel threshold to $2000 e^-$. Presently the threshold-to-noise ratio T/N is 4 for strips, and about 10 for pixels.

6.3. Efficiency vs. signal/threshold

As mentioned above, the threshold setting determines the tracking efficiency. In pixel systems in a strong magnetic field, large charge sharing occurs due to the Lorentz angle. Using the numbers of Ref. [38] as an indication, after radiation damage from a fluence of $6 \times 10^{14} n_{eq}/$ cm⁻², the signal-to-threshold ratio S/T = 6 results in an inefficiency of 1%; the S/T = 4 in an inefficiency of 2%; the S/T = 3 in an inefficiency of 3%; and the S/T = 2 in an inefficiency of 7%, respectively. Clearly a signal-to-threshold ratio S/T of above 3 and close to 4 is required.

Table 1 and Fig. 1 show the projected signal-tothreshold values for the upgraded tracking system, based on RD50 results. As expected, the strong radial fluence dependence shows up in the increased erosion of the S/T with decreasing radius. Using the criteria that a S/T of above 3 is required at the end of life, and close to 4 for the mid-point of sLHC running (when the discovery potential is high as explained in Section 2), the layout with all-silicon detectors would work, with planar n-on-p detectors at all radii from 8 cm out. The innermost pixel layers would be efficiently covered by 3-D detectors.

7. Summary

The LHC luminosity upgrade to 10^{35} cm⁻² s⁻¹ (sLHC) will be a challenge for the experiments: detector R&D needs to start now to upgrade the inner tracker, especially if one wants to be ready for data in 10 years time.

Based on measurements within the RD50 collaboration, the required tracking performance can be achieved with an inner detector using planar silicon detectors in all but the inner-most pixel layer, which will require 3-D detectors. Advances in electronics design would provide additional head room for the end of life performance.

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