UNIVERSITY of CALIFORNIA
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# CHARACTERIZATION OF THE IRST PROTOTYPE P-TYPE SILICON STRIP SENSOR

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# Abstract

A set of prototype P-Type Silicon Microstrip Sensors was characterized for bulk, surface and performance characteristics. The bias voltage dependence of the following parameters were measured; current, bulk capacitance, interstrip capacitance , interstrip resistance, and charge collection efficiency. Two new testing procedures were developed; one for measuring interstrip capacitance and the other interstrip resistance. The new interstrip capacitance measurements agreed exactly with previous studies using different measurement methods. The advantages of the new interstrip capacitance method include consistent setup through the use of bonding, and reliable shielding. The depletion voltage is found through the analysis of body capacitance, into a $\frac{1}{C^2}$ curve. The results from the interstrip resistance measurements have shown a saturation at high bias voltage similar to the interstrip capacitance. The interstrip capacitance is correlated with interstrip resistance in a linear relationship. The depletion voltage is bracketed using charge collection efficiency vs. bias voltage and the $\frac{1}{C^2}$ curve, and the analysis shows that the depletion characteristics are similar for both curves.

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# 1

# Introduction

## 1.1 Introduction to P-type Silicon Strip Detector

In this era of high-energy particle physics many experiments use head-on particle collisions to probe the structure of elementary particles[1]. To view the products of particle collisions several systems are employed. Currently the inner most particle detectors are made of silicon diodes in the form of strips or pixels. These diode detectors are subjected to extremely intense radiation. The electrical performance of detectors is known to deteriorate with exposure to radiation [2].

Currently the RD50 collaboration for the ATLAS project is looking for next generation detector devices to incorporate in the LHC upgrade [3]. The inner detector assembly of ATLAS LHC is made of three sections of detectors. The innermost detectors are of the pixel type, the second layer of detectors are made of short strips, and the last section are composed of longer strip detectors. This paper will characterize and performance test P-Type Silicon Strip Detectors (SSD) as a strong candidate to act as the two outer most detector systems.

### 1.1.1 N-type vs. P-type

Silicon Micro-strip detectors have been studied and characterized for the last two decades. During this time SCIPP has become a world leader in developing and understanding Silicon Strip Detectors. Several SSD systems have been researched and developed at UCSC for experiments including: ATLAS[4], PTSM[5], and GLAST[6].

The first SSDs were made out of N-Type Silicon bulk with P-Type diode implants. To date the N-Type detector is the most common type of SSD. The advantages of the N-Type detectors are:

- Well understood, as they were developed first
- Availability of high-purity N-type bulk Silicon wafers
- Small Lorentz angle

The advantages P-Type bulk Silicon has are:

- Electron mobility is better than the holes
- No Type inversion during high fluence application
- Extended Life time during high fluence application

To summarize the P-Type sensors are advantageous due to their lack of type inversion, which will allow prolonged system operation. There is also a small response time advantage to using the P-Type sensor over the N-Type.

## 1.2 The physics of SSDs

The P-Type SSD begins its life as any semiconductor device does, as bulk silicon. For the SSD the bulk silicon is doped with a charge carrying impurity. The silicon bulk is cut in to wafers of the order 200 $\mu$m for FZ or 300 $\mu$m for MCz. The wafers are then processed to implant surface structures to act as particle detection strips. The P-Type SSD is doped with N-Type Strips on one side, and P-Type impurities on the other. Once the impurities have been placed they are coated with a thin layer of Aluminum. The surface structures of the P-Type detectors are shown in Figure 1.1. The Figure 1.2 shows the location of the detector with a corresponding number. The structures that are built onto a detector are:

- Guard rings, to reduce the chance of surface electrical break-down
- Bias ring, Where the voltage is applied to the top of the sensor
- Bonding pads, the connection points for signal output
- A/C pads, used for A/C sensor biasing
- D/C pads, used for D/C sensor biasing

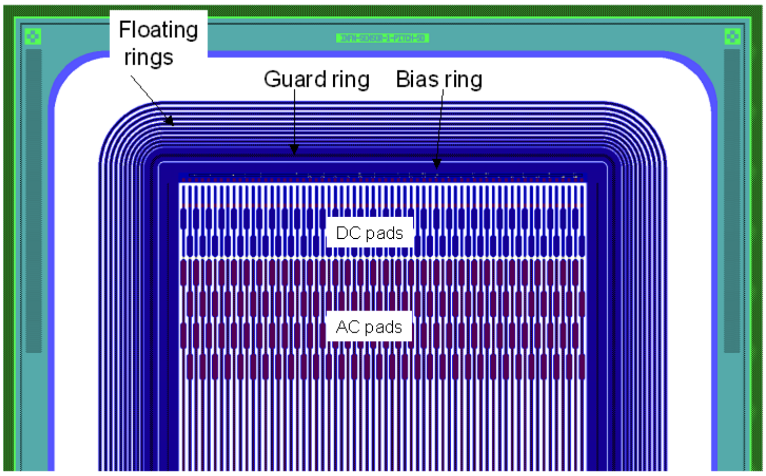

Figure 1.1: Detail of the P-Type SSD [7]

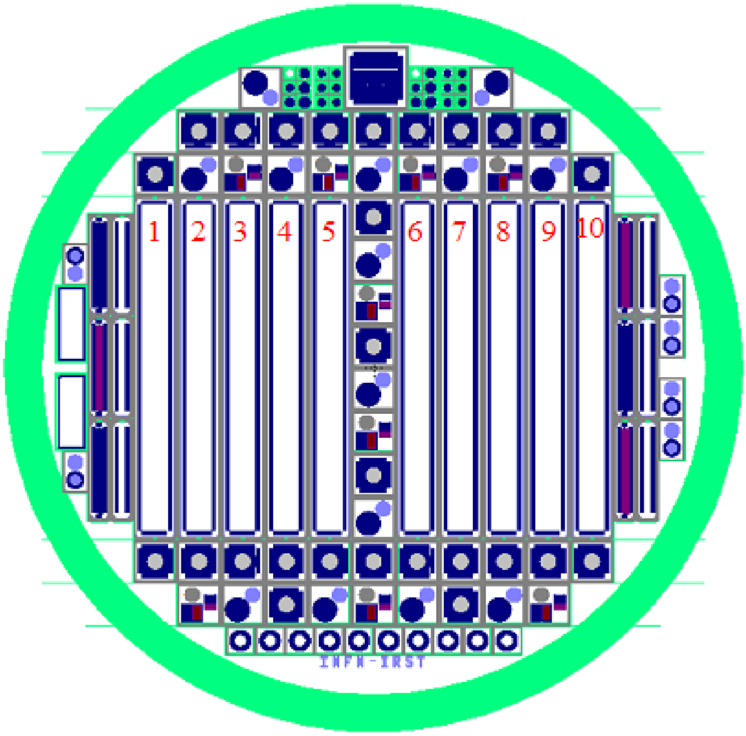

Figure 1.2: Detail of the P-Type wafer [7]

Table 1.1: Sensor Build Geometeries[8]

| Location | Pitch($\mu$m) | $N^+$ Implant($\mu$m) | Polysilicon($\mu$m) | Metal($\mu$m) |
|---|---|---|---|---|
| S1 | 50 | 15 | 10 | 23 |
| S2 | 50 | 20 | 15 | 28 |
| S3 | 50 | 25 | 20 | 33 |
| S4 | 50 | 15 | 10 | 19 |
| S5 | 50 | 15 | 10 | 27 |
| S6 | 100 | 15 | 10 | 23 |
| S7 | 100 | 25 | 20 | 33 |
| S8 | 100 | 35 | 30 | 43 |
| S9 | 100 | 25 | 20 | 37 |
| S10 | 100 | 25 | 20 | 41 |

The process where the particle detection takes place in the bulk of the silicon is diagramed in Figure 1.3. When a charged particles traverses the depleted region of the sensor ionization of the silicon atoms takes place. This ionization releases electron-hole pairs from the silicon atom. The electron-hole pairs them migrate by electro-static attraction generated by the biasing of the detector.

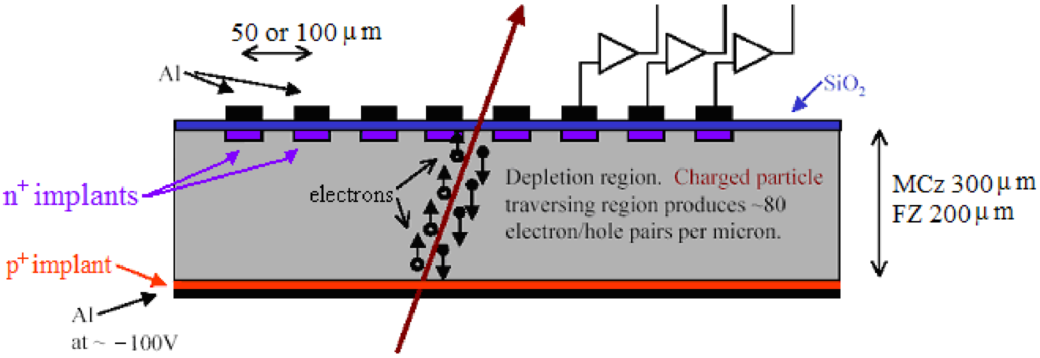

Figure 1.3: Ionization and particle detection diagram [1]

This bias voltage is increased to a point, full depletion, which is determined by characterization. Full depletion is defined by the absence of free electrons in the bulk of the

Silicon. Once full depletion is achieved the traversing particle produces the electron-hole pairs which register as a charge released in the surface diodes. The charge travels through the surface diodes to the read out electronics where the charge is read-out by the computer.

## 1.3 Motivation and Expectations

The goals of this research is to fully understand this prototype SSD for use on the sLHC's outer tracker detector. There are several signal and processing unknowns that have been discovered and dealt with so that detector can be used. The operating parameters of the P-Type SSD have been discovered through analyzing physical properties of the SSD through the following techniques:

- I-V Curves
- $\frac{1}{C^2}$-V Curves
- Interstrip Capacitance
- Interstrip Resistance
- Charge Collection Efficiency

These test will be described in the following sections and there results will be discussed. In many instances graphical analysis of the data is presented and will allow the formation of the characterization details. The data in the chapters extends to the voltage just before break down. This point of break down is different for each detector thus end-point voltage is different for each detector. The goal of pushing the voltage out to the break-down point was to provide data for comparison to a later study, which will characterize similar detectors that have been irradiated.

# 2

# P-Type Sensors Specifications

The detectors in this study were manufactured at ITC-irst, Trento, Italy. The INFN-SMART collaboration provided a sample of their latest P-Type sensor devices from the ITC SMART2 batch [8].

From wafers like the one shown in Figure 1.2, SCIPP received 16 full length sensors from different wafer types. In the following table the sensor geometries and process types are given for reference. The P-Type sensors are made of Boron doped bulk silicon with a concentration of 1.5-2.5 $x10^{-12}\frac{1}{cm^3}$ . In this study the only sensors used were ones with low dose P-Spray having a concentration of $3x10^{12}\frac{1}{cm^2}$. The concentration of the high dose P-Spray is $5x10^{12}\frac{1}{cm^2}$.

Table 2.1: Characterized Sensor Geometries

| Wafer I.D. | Location | Type | Pitch | $N^+$ | Polysilicon | Metal | Thickness |
|---|---|---|---|---|---|---|---|
| W014 | S5 | MCz | $50\mu m$ | $15\mu m$ | $10\mu m$ | $27\mu m$ | $300\mu m$ |
| W066 | S5 | FZ | $50\mu m$ | $15\mu m$ | $10\mu m$ | $27\mu m$ | $300\mu m$ |
| W014 | S8 | MCz | $100\mu m$ | $35\mu m$ | $30\mu m$ | $43\mu m$ | $200\mu m$ |
| W066 | S8 | FZ | $100\mu m$ | $35\mu m$ | $30\mu m$ | $43\mu m$ | $200\mu m$ |

# 3

# I-V Curves

The P-Type SSDs came I-V curves done at the wafer level. In these I-V curves there were several sensors that displayed break-down of the current carrying ability at approximately 60 volts. The behavior was unexplained by the ITC engineers and investigation was necessary.

The I-V curves done at SCIPP showed for some of the detectors the same break-down, although there were some sensors that displayed break-down at SCIPP that did not break-down at ITC.

This new break-down gave reason to believe that the break-down could be caused by some external factors. The outside of each detector was documented for surface scratches. The images showed that scratches were present on both top and bottom sides. It was discovered that the sensors that displayed break-down were not the only sensors that had surface scratches. Therefore break-down was attributed to the wafer processing.

A goal of this break-down investigation was to narrow down the field of candidate sensors, which would undergo full characterization. In this study two types of SSD processing are available, Magnetic-Czochralski(MCz) and Float Zone(FZ). Within these two types of detectors there are two geometries detailed in Table 2.1. The four sensors were chosen on the basis of no break-down in the I-V curves. The I-V curves done at SCIPP displayed a current reading different by at least 50% from the manufacturer. This difference can be attributed to several variables the most important being climate differences, which can give two times the current for a temperature change of seven degrees Celsius. Also, a difference in I-V curve apparatus setup, and if the sensor was measured as a part of a wafer or as a stand-alone could cause the decrease in current seen at SCIPP. The I-V curves done at SCIPP are shown in Figures 3.1 through 3.4.

Leakage current per $cm^2$ from ITC are quoted to be 140 $nA/cm^2$ for both FZ and MCz P-Type from Diodes [9]. The Calculations for the current consumption per $cm^2$ for the characterized sensors are calculated in Table 3.1 using Equation 3.1.

ITC-IRST's leakage current per $cm^2$ comes from a Diode [9]. The values for leakage current per $cm^2$ of the P-Type sensors received at SCIPP in some cases are three times as much as seen from diodes. Experience shows that the leakage current per $cm^2$ for GLAST N-Type sensors at SCIPP is considerately lower. The P-Type MCz sensors are displaying leakage currents a couple of order of magnitude higher than leakage currents for GLAST N-Type sensors which have leakage currents of a few of nA/$cm^2$ [6].

$$\frac{Leakage\ Current}{Sensor\ Area} = \frac{Leakage\ Current(100V)}{(Strip\ Length)(Strip\ Width)(No.\ of\ Strips)} \tag{3.1}$$

Table 3.1: Leakage currents of P-Type sensors

| Sensor I.D. | $\frac{nA}{cm^2}$ | Reference |
|---|---|---|
| MCz Diode | 140 | [9] |
| W066-S5 | 302 | This Paper |
| W066-S8 | 505 | This Paper |
| W014-S5 | 122 | This Paper |
| W014-S8 | 755 | This Paper |

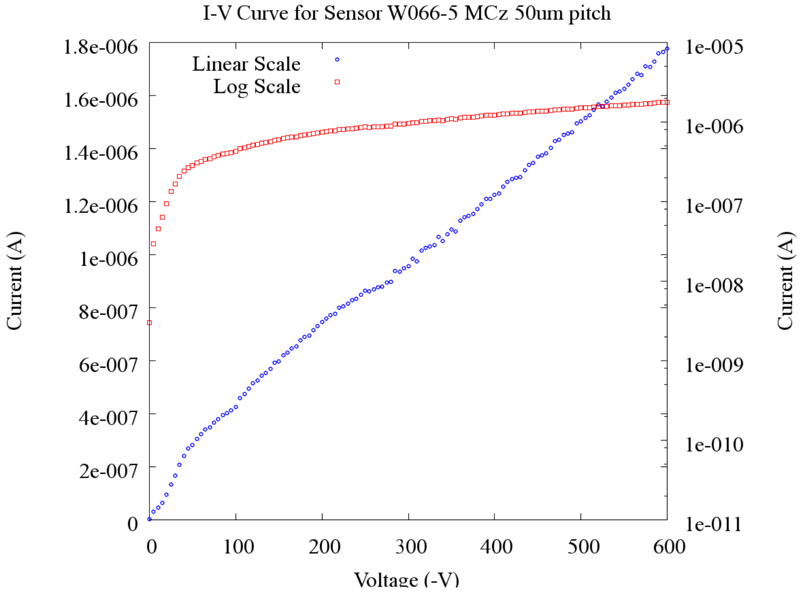

Figure 3.1: I-V curves for W066-S5 with linear and log scales

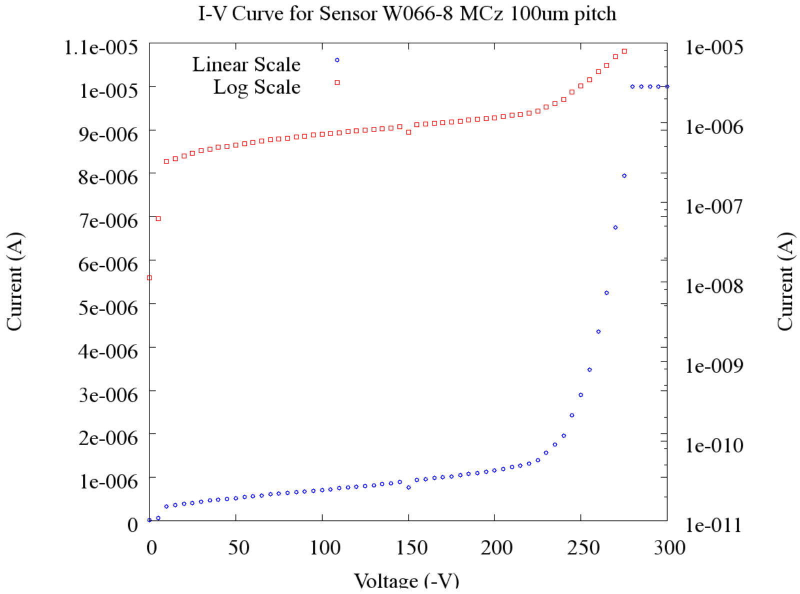

Figure 3.2: I-V curves for W066-S8 with linear and log scales

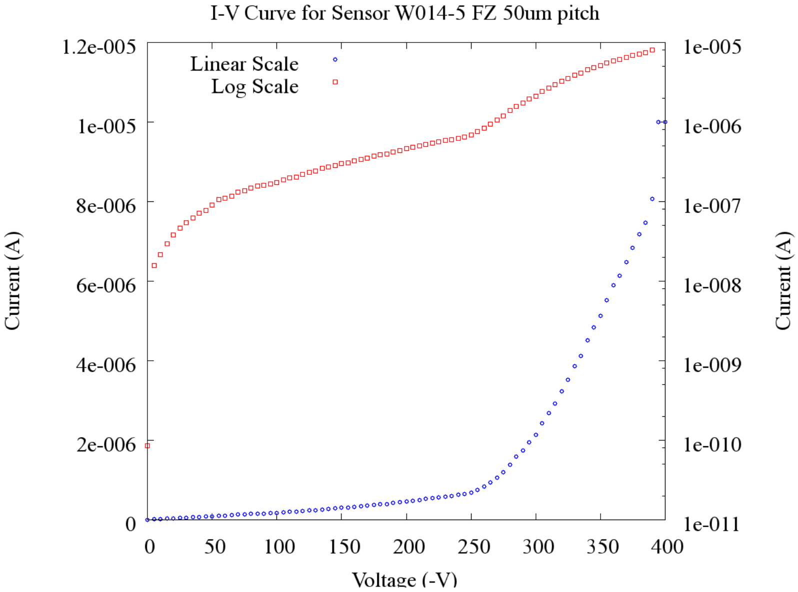

Figure 3.3: I-V curves for W014-S5 with linear and log scales

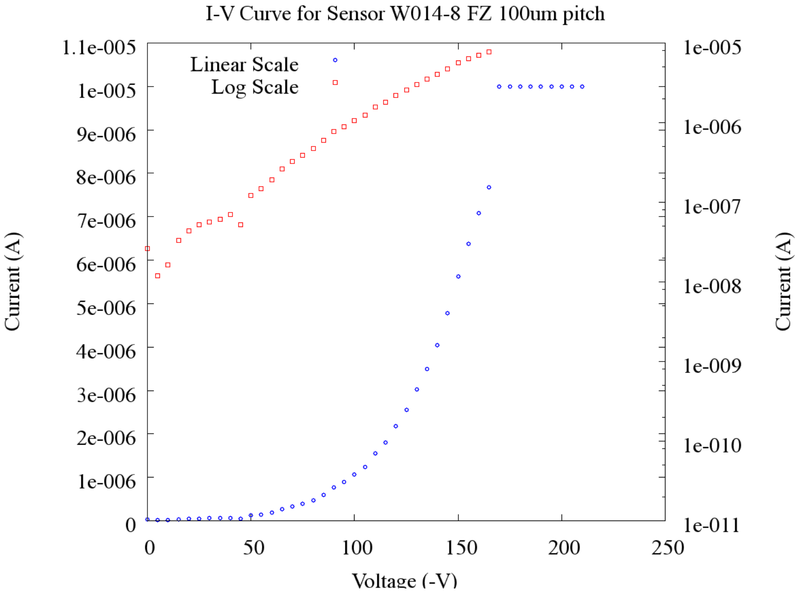

Figure 3.4: I-V curves for W014-S8 with linear and log scales

# 4

# $\frac{1}{C^2}$ Curves

Capacitance verses Voltage Curves were created using an HP 4284A Precision LCR meter. The LCR meter measures the complex impendence and is able to calculate the capacitance and resistance from this value. In the case of the P-Type Sensors the configuration is such that there is a resistor and capacitor in series. By connecting the bias ring to ground and applying a voltage to the backplane a current has to pass through the sensor bulk and then up through the strip to the DC bias resistor and out through the bias line to complete the circuit. In Figure 4.1 the bias ring, bias resistors, and DC pads are visible. This circuit is in reality a RC network with a frequency dependency that ends up being somewhat complicated. According to previous studies lower frequencies are able to see the whole length of the sensor[10]. In Figure 4.2 the capacitance verses the bias Voltage is plotted showing all of the different frequencies. The capacitance measured at 100kHz was used in the $\frac{1}{C^2}$ Curves.

The C-V curve is analyzed such that a $\frac{1}{C^2}$ curve is calculated, which in turn helps to magnify the depletion voltage. In the analysis of the C-V data is was found that at

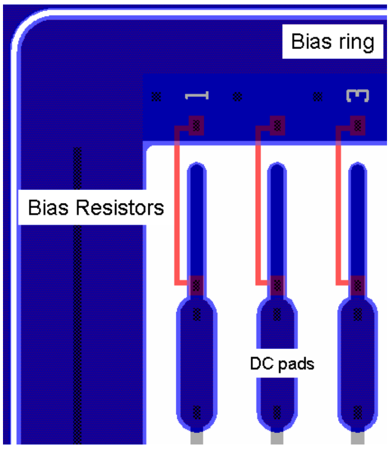

Figure 4.1: Top-down diagram of sensor circuit structure

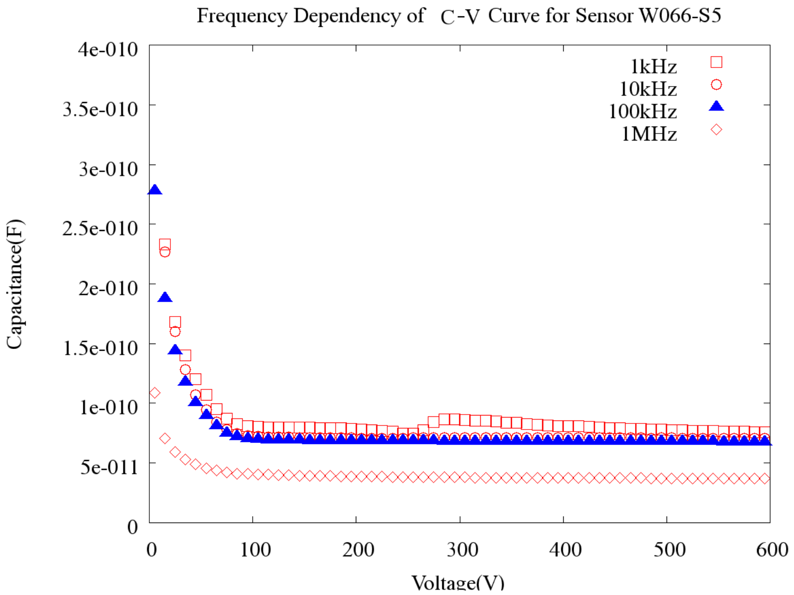

Figure 4.2: C-V curve with frequencies of 1kHz, 10kHz, 100kHz, and 1MHz

100kHz frequency the $\frac{1}{C^2}$ curve gave the most consistent results with the lowest frequency. In Figures 4.4 through 4.7 the plateau is clearly visible and the depletion voltage is marked by the intersection between the sloped region and the horizontal region. This intersection corresponds to a voltage where the detector is fully depleted.

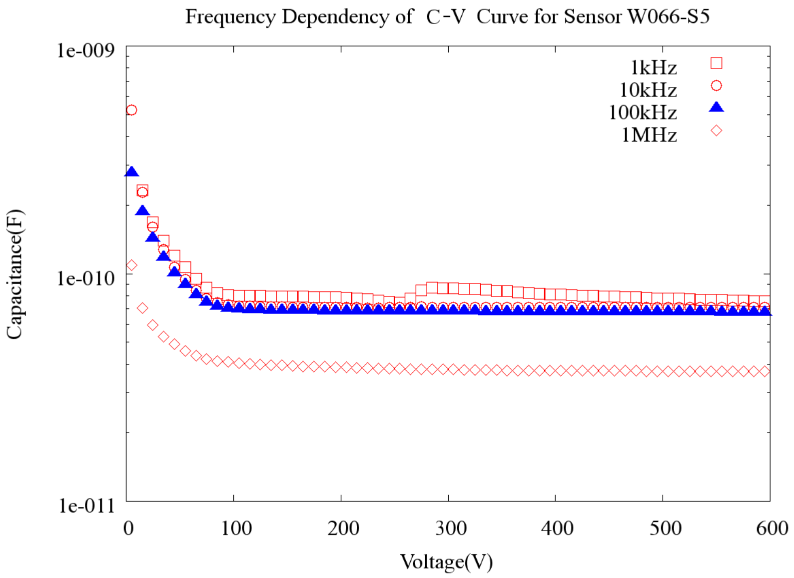

Figure 4.3: C-V curve with frequencies of 1kHz, 10kHz, 100kHz, and 1MHz using a log scale

## 4.1 Efficiency and Depletion voltage

Beyond depletion the sensor should be at its most efficiency at detecting high energy particles. In order to check this a sensor was mounted to a read-out system and the efficiency verse bias voltage was measured.

### 4.1.1 The Efficiency Test Structure

The basic idea behind the efficiency setup is to have a radiation source pass through the Silicon detector and then into a scintillation counter. The detector structure consists of the PTSM read-out board with a SSD mounted just in front of the PMFE [5].

The detector structure is mounted to a micro-position stage. Attached to the platform of the micro-position stage is a alignment bracket for the radiation source. The radiation source is collimated down to one millimeter by one millimeter square beam. Instead of mounting the read-out electronics directly to the FPGA board a cable is fabricated to run between the two.

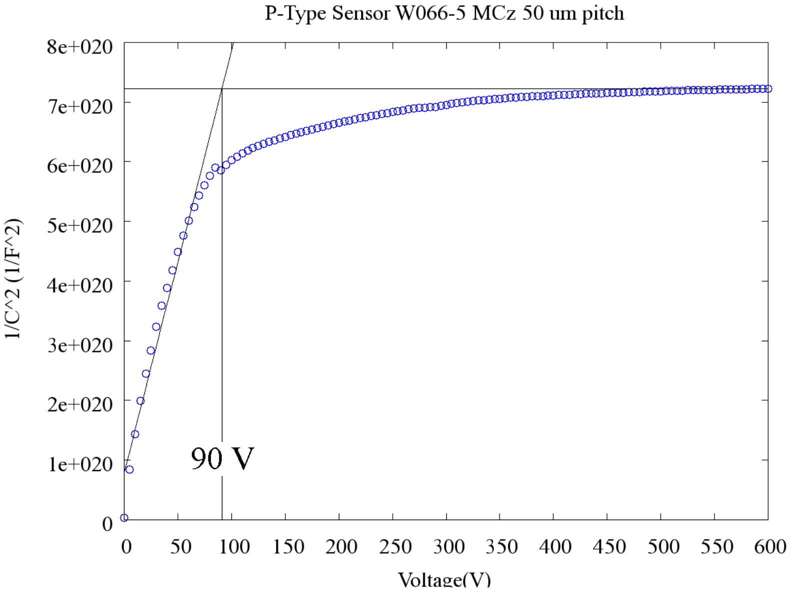

Figure 4.4: $\frac{1}{C^2}$ curve at 100kHz for W066-S5 50 $\mu$m pitch

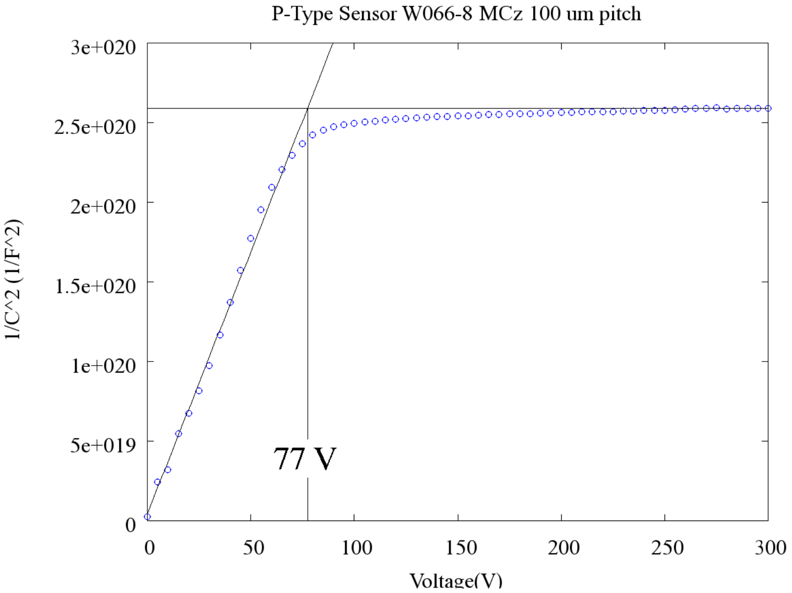

Figure 4.5: $\frac{1}{C^2}$ curve at 100kHz for W066-S8 100 $\mu$m pitch

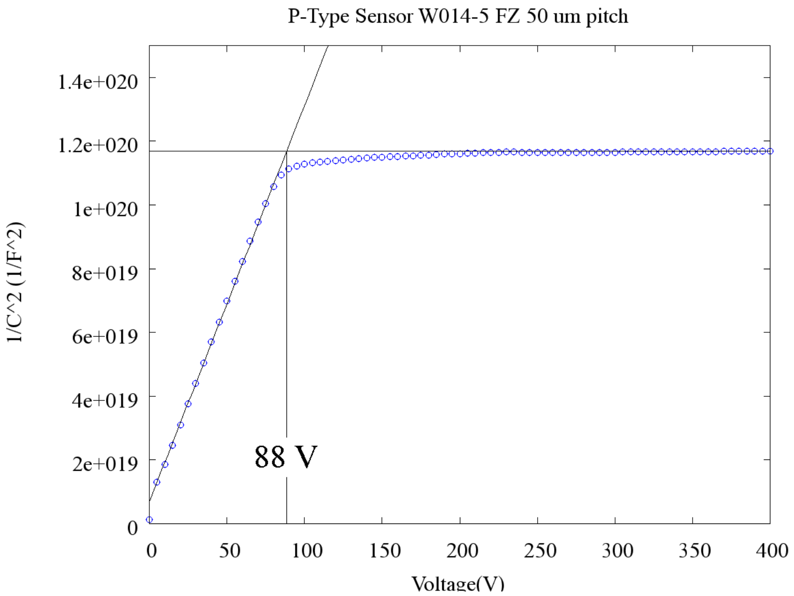

Figure 4.6: $\frac{1}{C^2}$ curve at 100kHz for W014-S5 50 $\mu$m pitch

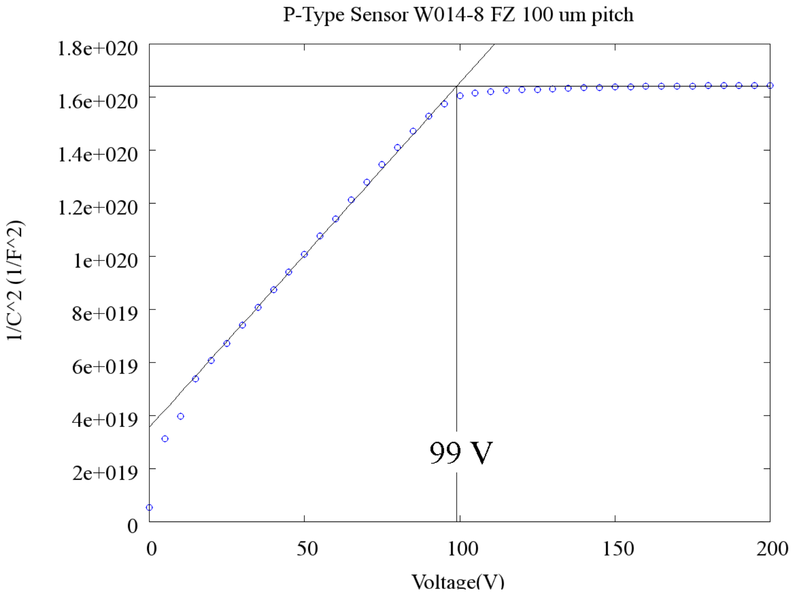

Figure 4.7: $\frac{1}{C^2}$-V curves at 100kHz for W014-S8 100 $\mu$m pitch

### 4.1.2 P-Type Efficiency Results

With efficiency data available for Sensor W066-S5 there is a second set of data to check the accuracy of the depletion voltage [12]. In Figure 4.8 data from the CCE vs. Bias Voltage and data from the $\frac{1}{C^2}$ curve were compared to see the difference in depletion voltage given by each. Figure 4.8 shows the depletion voltages agree with in 3 volts. Using the full $\frac{1}{C^2}$ curve in Figure 4.4 a depletion voltage of 90V is found, as compared with 87 volts from Figure 4.8. The depletion voltage from CCE in Figure 4.8 gives 84 volts. If the CCE curve was extended to higher voltages the agrement between the full $\frac{1}{C^2}$ curve and CCE curve would be better.

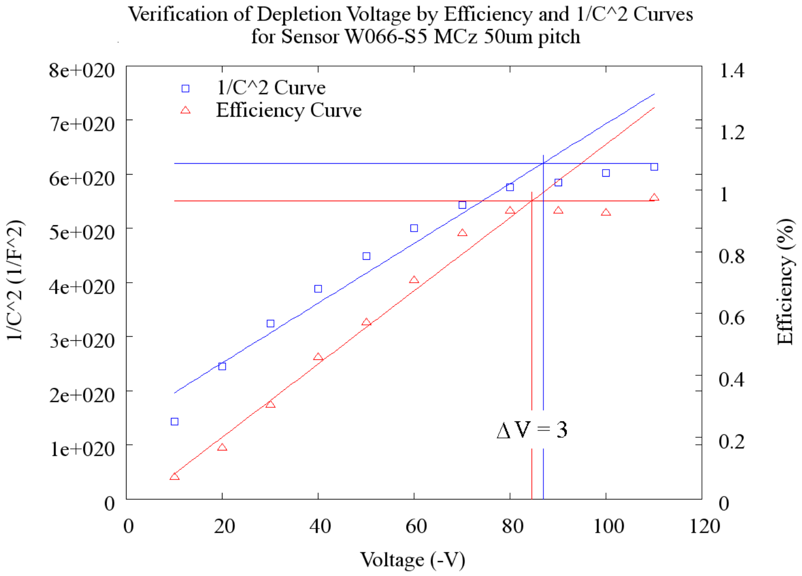

Figure 4.8: CCE [12] and $\frac{1}{C^2}$ curves are compared to bracketed depletion voltage

# 5

# Interstrip Capacitance

The interstrip capacitance measurement is used as an indicator of the surface characteristics of the sensor, is the main contributor to the total strip capacitance. The interstrip capacitance also tells of the noise from the detector. Originally the method of measuring the interstrip capacitance was to have a test strip, and then on either side of the test strip to bond together the next three neighbors. Then to each side shielding strips were bonded together and a probe was used to make the shielding connection. Shown in Figure 5.1 is the diagram from a study done at SCIPP in 1995 [10]. In this study is was discovered that bonding three neighbors to each side of the test strip will include 95% of the interstrip capacitance [10].

In measuring the interstrip capacitance for this study a different arrangement to measure the interstrip capacitance was devised. In order to validate the method data was collected using both arrangements. In figure 5.2 the agreement is nearly perfect for both methods. In Figure 5.3 a diagram of the new arrangement is shown.

In Figure 5.2 the percent difference is much less than 1% at high bias voltages.

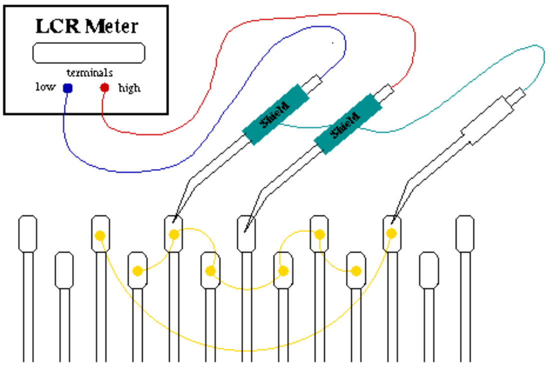

Figure 5.1: Interstrip capacitance diagram from a SCIPP 1995 study [10]

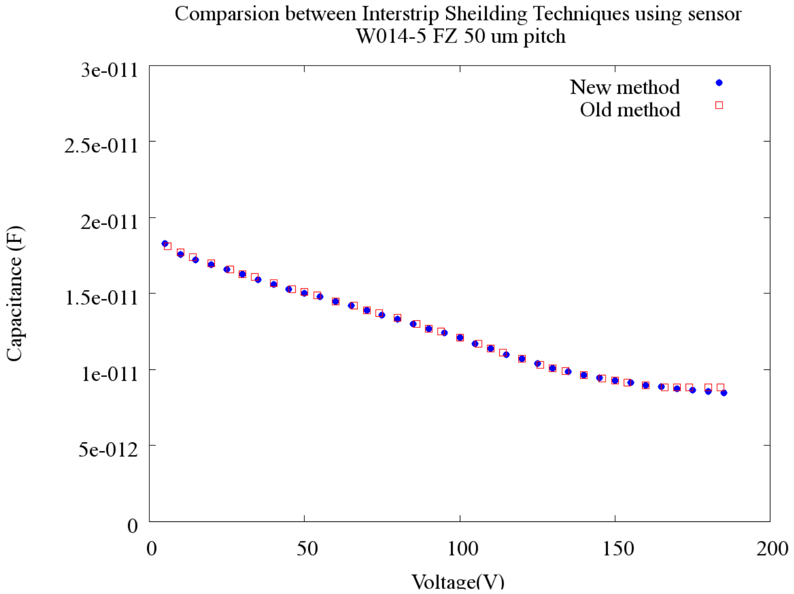

Figure 5.2: Interstrip Capacitance Curve for validation of new measurement technique

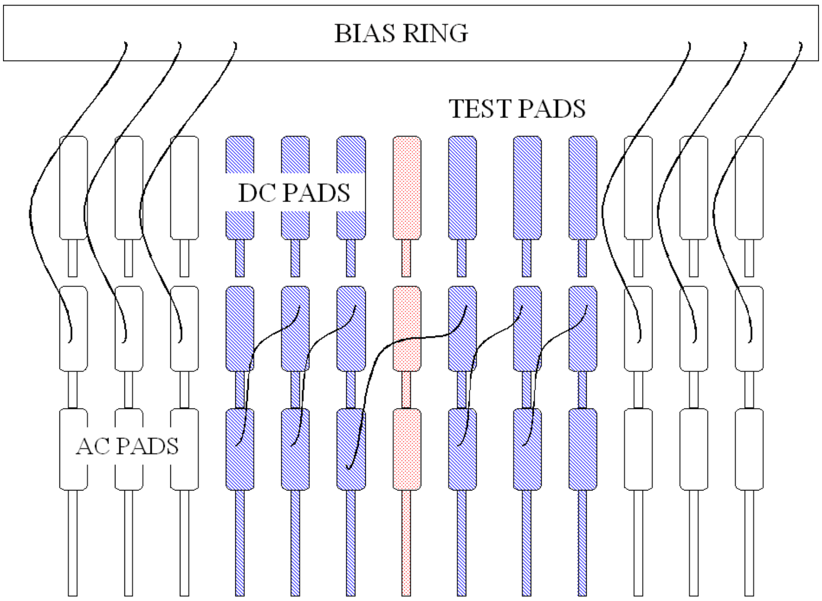

Figure 5.3: Diagram for new interstrip capacitance technique

The previous method of measuring the interstrip capacitance was difficult to connect up the shields. It was also was very difficult to produce a consistent setup that was reliable. As for the new arrangement a consistent setup was achieve each time.

In Figures 5.4 to 5.6 measurements were made with one pair of neighbors and three pairs of neighbors to check that the capacitance increased with the number of pairs to each side. It is clearly visible that the single neighbor measurement is missing some capacitance. Calculations give an increase of 10 to 15% of Interstrip Capacitance for three pairs of neighbors verses one pair of neighbors at high bias voltages.

The interstrip capacitance in Figures 5.7 through 5.10 show a correlation with the bias voltage. It seems that as long as the voltage is increased the interstrip capacitance will continue to go down to some minimum value where a leveling off is expected.

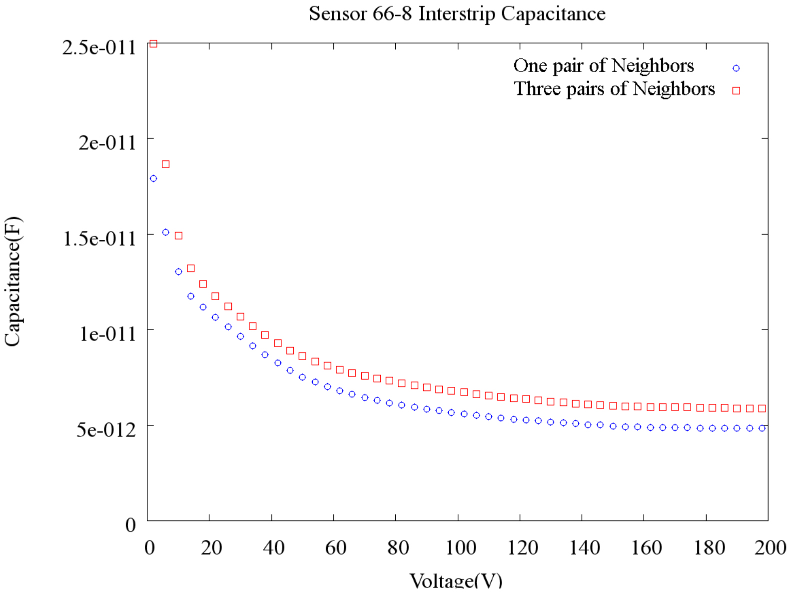

Figure 5.4: Comparing interstrip capacitance measurements for neighbors configuration for W066-S8 100 $\mu$m pitch

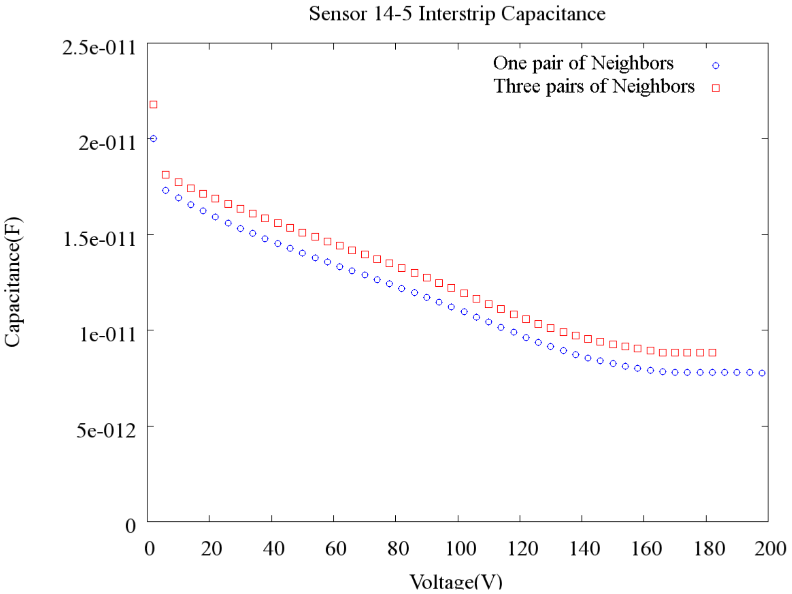

Figure 5.5: Comparing interstrip capacitance measurements for neighbors configuration for W014-S5 50 $\mu$m pitch

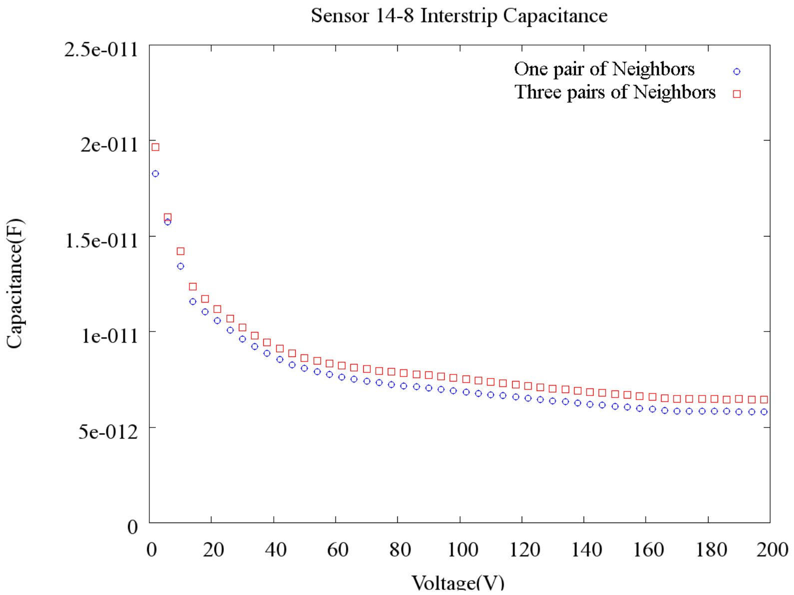

Figure 5.6: Comparing interstrip capacitance measurements for neighbors configuration for W014-S8 100 $\mu$m pitch

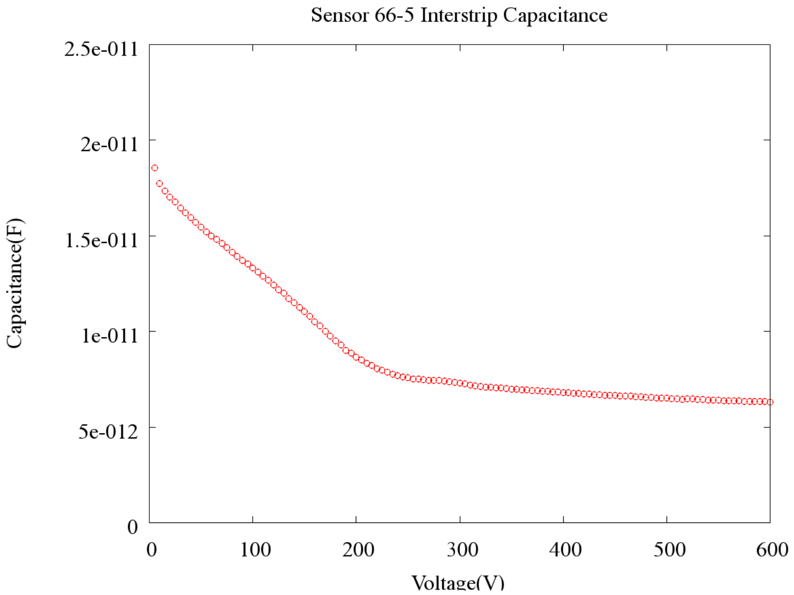

Figure 5.7: Interstrip capacitance curve for W066-S5 50 $\mu$m pitch

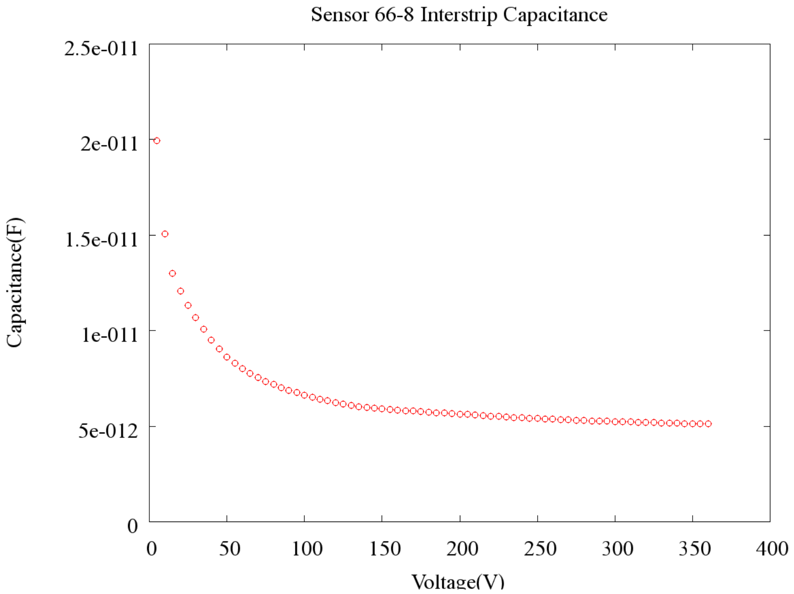

Figure 5.8: Interstrip capacitance curve for W066-S8 100 $\mu$m pitch

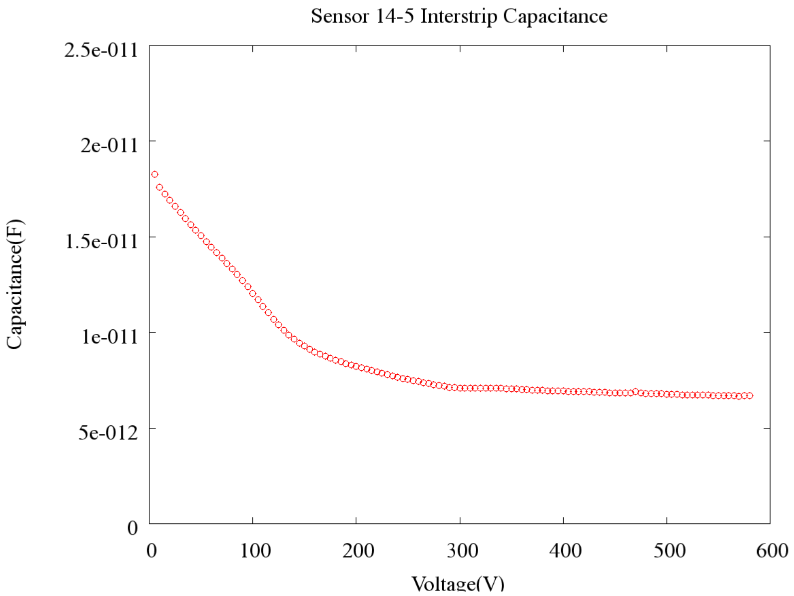

Figure 5.9: Interstrip capacitance curve for W014-S5 50 $\mu$m pitch

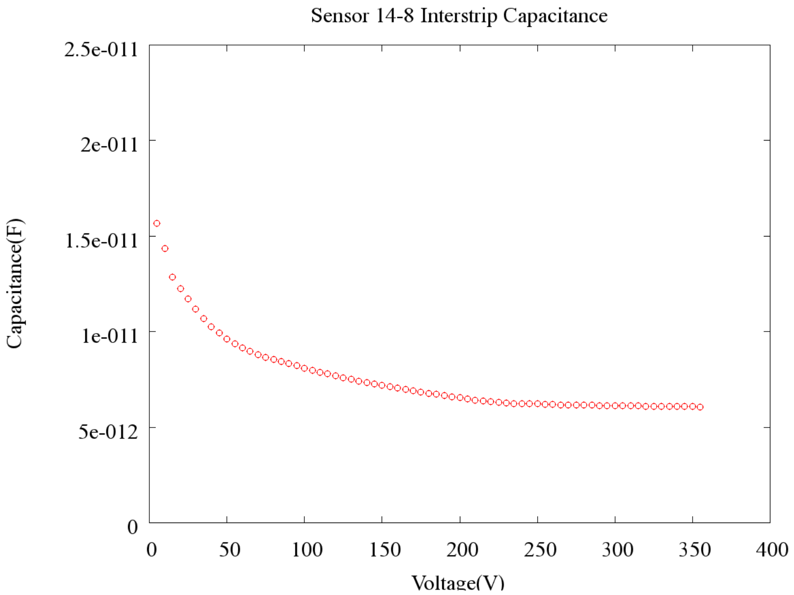

Figure 5.10: Interstrip capacitance curves for W014-S8 100 $\mu$m pitch

# 6

# Interstrip Resistance

The interstrip resistance measurement proved to be a very difficult. The set up was such that the sensor was biased, and three probes were used to make the measurement. On the outer two pads, probes were placed on the DC pads, a the same voltage was applied to both. The central strip, called the test strip, was kept at zero volts with the bias ring going to an external ground. The diagram in Figure 6.1 show how the probes were connected for the interstrip resistance measurement.

The interstrip resistance was determined through an I-V curve. The I-V curves was calculated from the difference between the test probe voltage (i.e. 0V) and voltage of the two probes (i.e. $+1V to - 1V$) versus the current of test probe. The data for the test probe is restricted to when the neighbor probes current is not at compliance. The test probe current is plotted against the voltage difference (restricted to ±.2V) the slope of this curve is one over the interstrip resistance, $1/R_{int}$. As shown in Figures 6.2, 6.3, and 6.4 the interstrip resistance IV curves are shown with there data fit equations from which the interstrip resistance is calculated. As for Sensor W066-S8 this sensor is still connected to the efficiency read-out system for further study, so a Interstrip Resistance measurement was not done on this sensor.

In Figure 6.2, the interstrip resistance IV measurement for W066-S5, the behavior of this detector was unexplainable. During the measurement for this detector all connections were triple checked. The measurement was second in the nights measurements with the measurements before and after giving normal curves. Interstrip resistance for sensor W014-S5 was also very strange. The interstrip resistance went from negative to very high positive values back to negative at the end. Again, this behavior is not understood. The interesting thing about the interstrip resistance measurements for W066-S5 and W014-S5, was that both displayed extremely strange behavior and both share the same surface geometry.

For Figures 6.6, and 6.5 the interstrip resistances for sensors W014-S5 and W014-S8 are plotted separately. The interstrip resistance was plotted versus the bias voltage of the sensor. In Figure 6.7 measurements for W066-S5 and W014-S5 were removed and including measurements for other sensors from another study were included. Figure 6.7 suggests that there is a saturation trend for the interstrip resistance notably W014-S8 follows this trend.

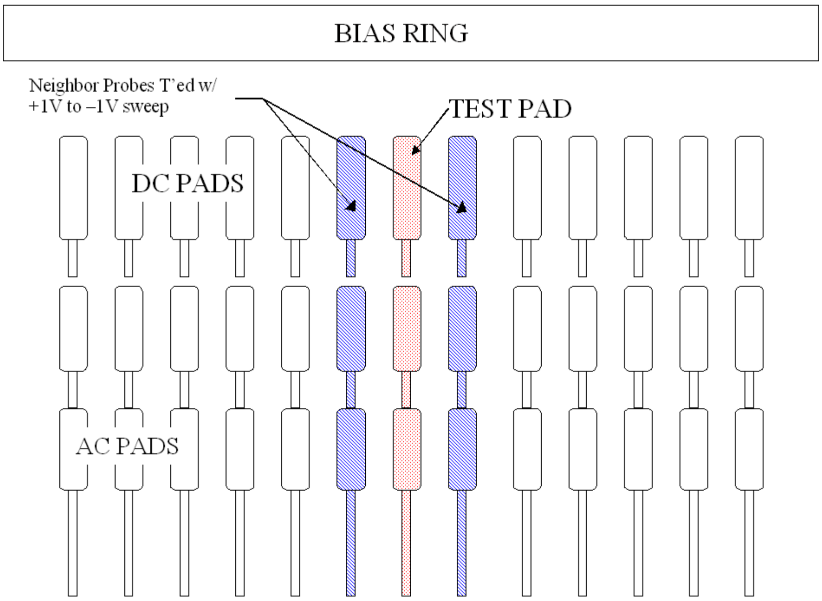

Figure 6.1: Diagram for interstrip resistance measurement

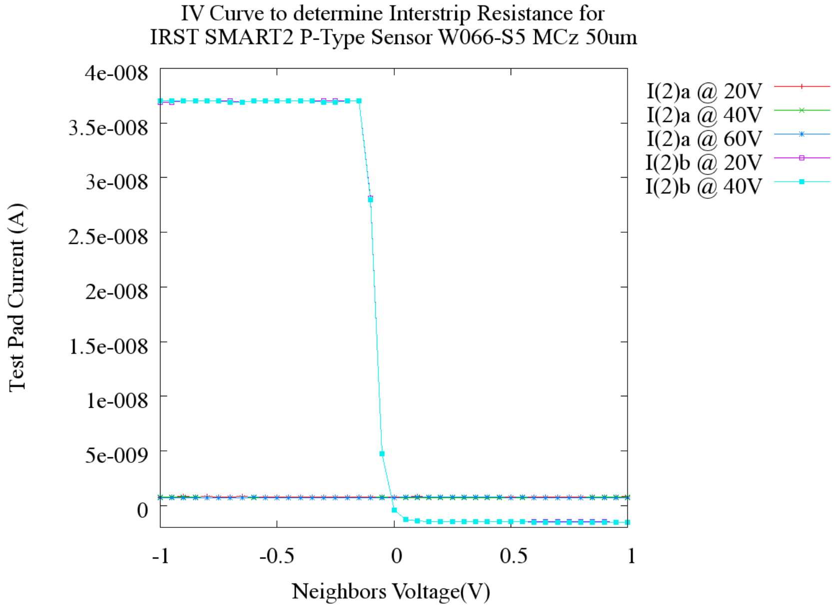

Figure 6.2: Interstrip resistance IV measurement for sensor W066-S5

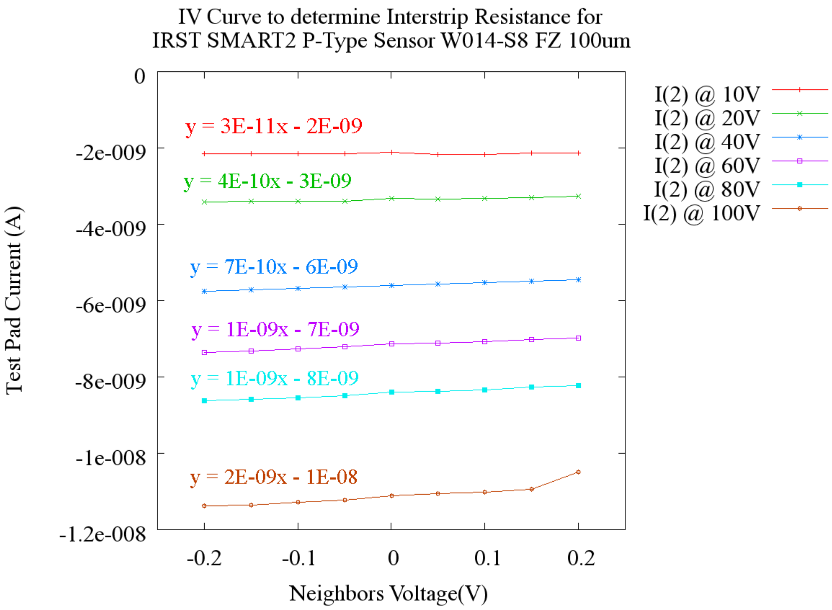

Figure 6.3: Interstrip resistance IV measurement for sensor W014-S8

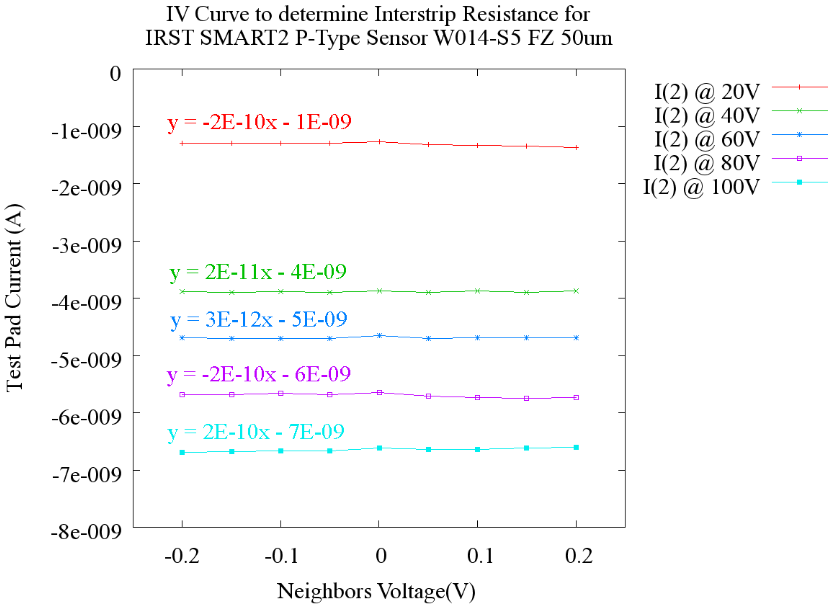

Figure 6.4: Interstrip resistance IV measurement for sensor W014-S5

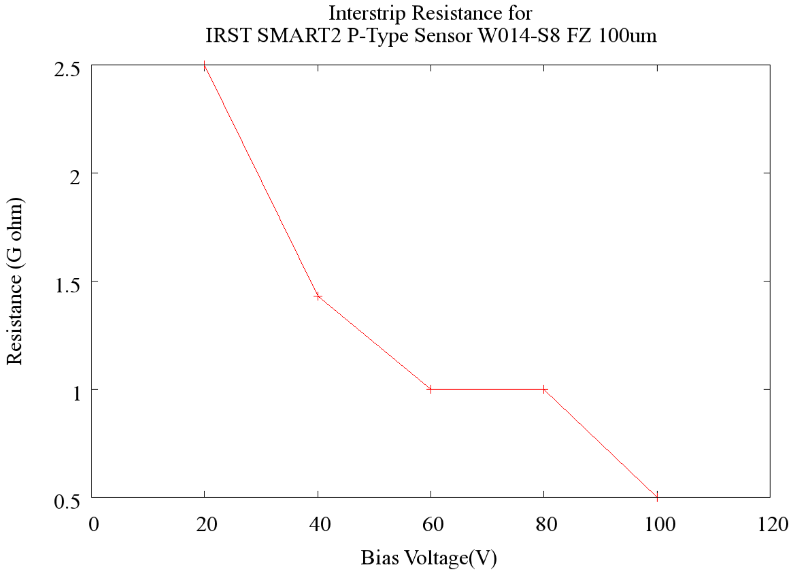

Figure 6.5: Interstrip resistance measurement for sensor W014-S8

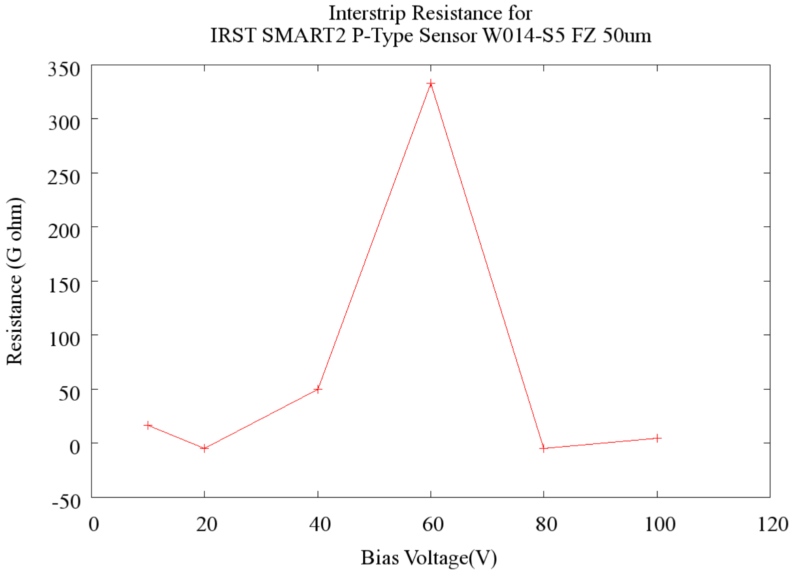

Figure 6.6: Interstrip Resistance measurement for sensor W014-S5

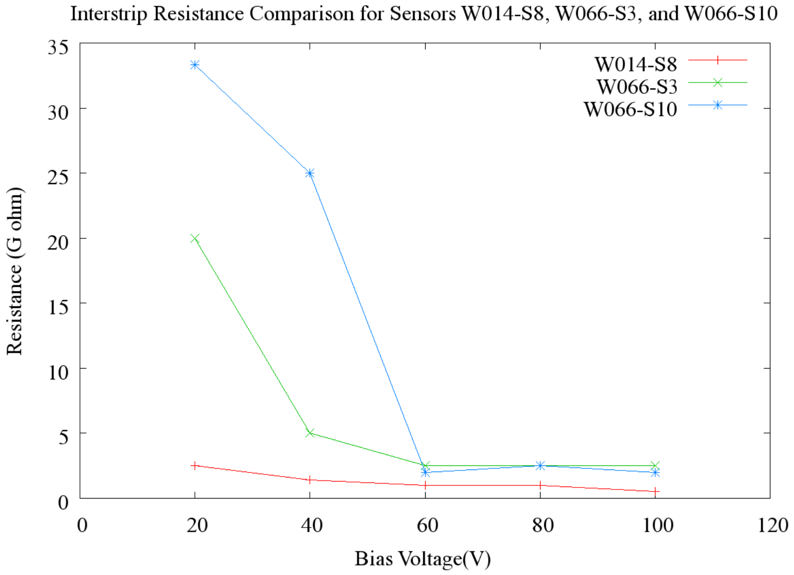

Figure 6.7: Interstrip Resistance Comparison of sensors W014-S8, W066-S3, and W066-S10

# 7

# Interstrip Capacitance vs. Interstrip Resistance

In an attempt to find a correlation between interstrip resistance and interstrip capacitance in a Interstrip Capacitance vs. Interstrip Resistance curves was created. For this correlation sensor W014-S8 was used. The graph showed linear correlation. With further agreement by other sensors this could be a way to find two useful surface characteristics by one measurement. Figure 7.1 shows this correlation along with the approximate equation fitting the data.

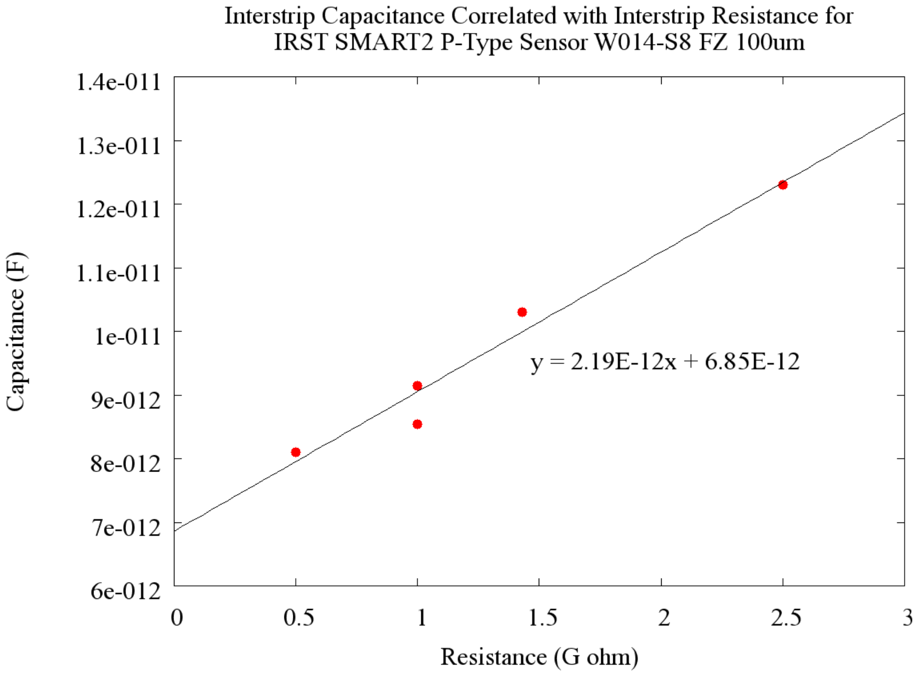

Figure 7.1: Correlation between interstrip capacitance and interstrip resistance for sensor W014-S8

# 8

# Conclusions

The characterization of the selected P-Type sensors went extremely well. There were several hurdles over come concerning measurement techniques. The extremely high leakage current was a characteristic noticed by ITC and confirmed at SCIPP. In looking for the reason of the high leakage current the surface degradation and damage was ruled out. The break-down was attributed to the wafer processing. The difference seen between the ITC-IRST's leakage current and SCIPP's values could be partially due to environmental conditions and measurement setup. Much of the data in this report will be compared to irradiation studies. These irradiation studies will be a very important step in gauging the success of the P-Type sensor.

The interstrip resistance measurements shielding and grounding issues were a major trouble spot. With these issues worked out there were still interstrip resistance behaviors that are strange. The correlation between interstrip capacitance and interstrip resistance is a major finding, and should soon be confirmed by simulation.

Overall the goals of this paper were accomplished. The P-Type sensors could prove

Table 8.1: Measurement Results

| Sensor | Type | Pitch $\frac{\mu}{m}$ | $N^+$ Implant $\frac{\mu}{m}$ | Leakage I $\frac{nA}{cm^2}$ | V dep -V | Backpl C $\frac{pF}{cm}$ | Cint $\frac{pF}{cm}$ | Rint $\frac{10^9\Omega}{cm}$ |
|---|---|---|---|---|---|---|---|---|
| W066-S5 | MCz | 50 | 15 | 140 | 90 | 0.15 | 1.5 | NA |
| W066-S8 | MCz | 100 | 35 | 302 | 77 | 0.28 | 1.2 | NA |
| W014-S5 | FZ | 50 | 15 | 122 | 88 | 0.21 | 1.6 | 1.1 |
| W014-S8 | FZ | 100 | 35 | 755 | 99 | 0.35 | 1.4 | 0.11 |

to be the next best technology for use in the ATLAS LHC upgrade. Plus, future studies will have plenty of data to compare their results.

In the Table 8.1 I have tabulated the results for this study. In all cases the P-Spray is low dose of $3x10^{-12}\frac{1}{cm^2}$. The width measurements for things such as implant width and pitch are in micrometers. For the back-plane capacitance (backpl C), and interstrip capacitance the values are at saturation. The back-plane capacitance per cm is calculated using Equation 8.1. For the interstrip resistance (Rint) the results are give at 100 volts. For values such as Cint, and Rint are divided by the strip length, 4.3 cm.

$$backpl\ C = \frac{Bulk\ capacitance}{Sensor\ area} \cdot (Pitch) \tag{8.1}$$

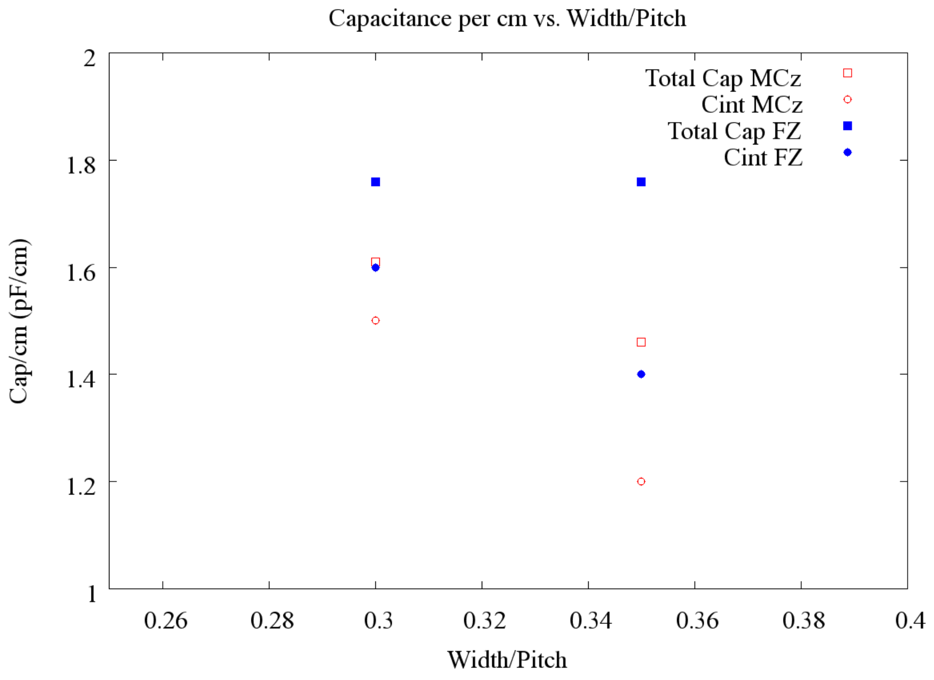

Figure 8.1: Total capacitance vs. width/pitch

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