Tracking Detectors for the LHC Upgrade

- **Layout**
- **Signal**
- **Noise**

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sLHC, the Machine
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Large Hadron Collider Project

LHC Project Report 626

LHC Luminosity and Energy Upgrade: A Feasibility Study

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Upgrade in 3 main Phases:

- Phase 0 – maximum performance without hardware changes

  Only IP1/IP5, N_b to beam beam limit → $L = 2.3 \bullet 10^{34}$ cm^{-2} s^{-1}
- Phase 1 – maximum performance while keeping LHC arcs unchanged

  Luminosity upgrade (β^*=0.25m, # bunches,..) → $L = 5 - 10 \bullet 10^{34}$ cm^{-2} s^{-1}
- Phase 2 – maximum performance with major hardware changes to the LHC

  Energy (luminosity) upgrade → E_{beam} = 12.5 TeV NOT cheap!

The sLHC as a necessity !

In 2015, the inner parts of the LHC detectors will have seen 8 years of beams and need to be replaced mainly because of radiation damage.

The LHC discovery potential has an even shorter time span:

The relative statistical errors on measurements are given by 1/√N, i.e 1/$\sqrt{\int Ldt}$

A good measure of the discovery potential is the time to half the statistical error

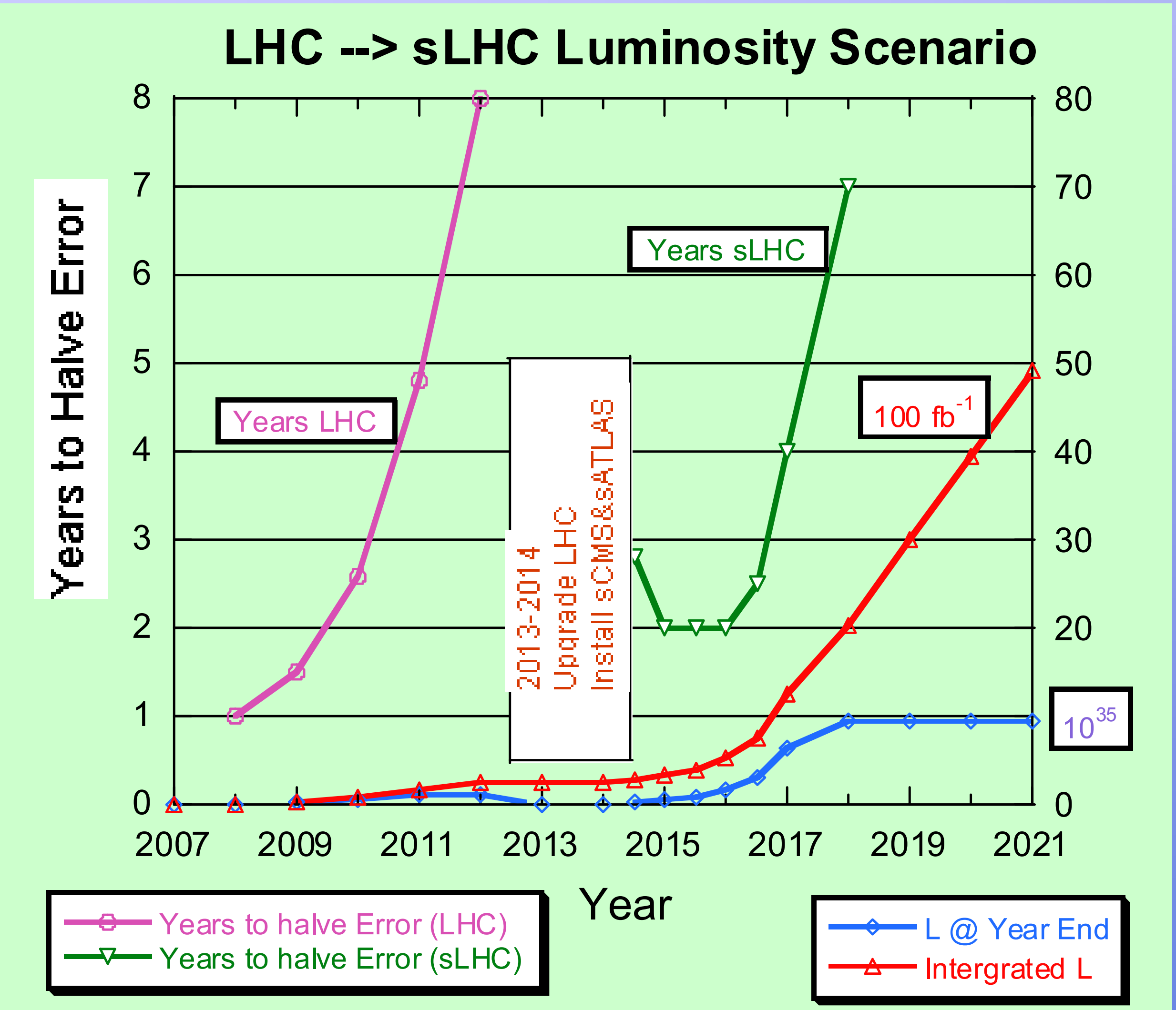
At the LHC in 2012, after two years at full luminosity, the time to halve the errors is 8 years ! Jim Strait (US LARP)

For the sLHC this might occur in 2018, when the collider just reached the full luminosity!

Thus, the time of largest discovery potential is the few years after the accelerator has reached full luminosity.

Until that time, at about 50% - 80% of the final integrated luminosity, the detector should have preserved its peak performance.

Discovery Potential of sLHC



Schedule of Upgrades

Machine:

Convert LHC	'13 – '14

Detectors:

Need to start	'04
R&D	'04 - '09
Construction	'10 -'13
Installation	'14

Are we too late already??

Expected Detector Environment

	LHC	sLHC
$\sqrt{s}$ [TeV]	14	14
Luminosity [$cm^{-2}s^{-1}$]	10^{34}	10^{35}
Bunch spacing Δt [ns]	25	12.5/25
σ_{pp} (inelastic) [mb]	~ 80	~ 80
# interactions/x-ing	~ 20	~ 100/200
$dN_{ch}/d\eta$ per x-ing	~ 150	~ 750/1500
$\langle E_T \rangle$ charg. Part. [MeV]	~ 450	~ 450
Tracker occupancy *	1	5/10
Dose central region *	1	10
LAr Pileup Noise [MeV]	300	950
μ Counting Rate [kHz]	1	10

* Normalized to LHC values: 10^4 Gy/year R=25 cm

Problems are daunting → Have a Workshop!

Jan 04 http://atlaspc3.physics.smu.edu/atlas/ US only

Feb 04 http://agenda.cern.ch/fullAgenda.php?ida=a036368

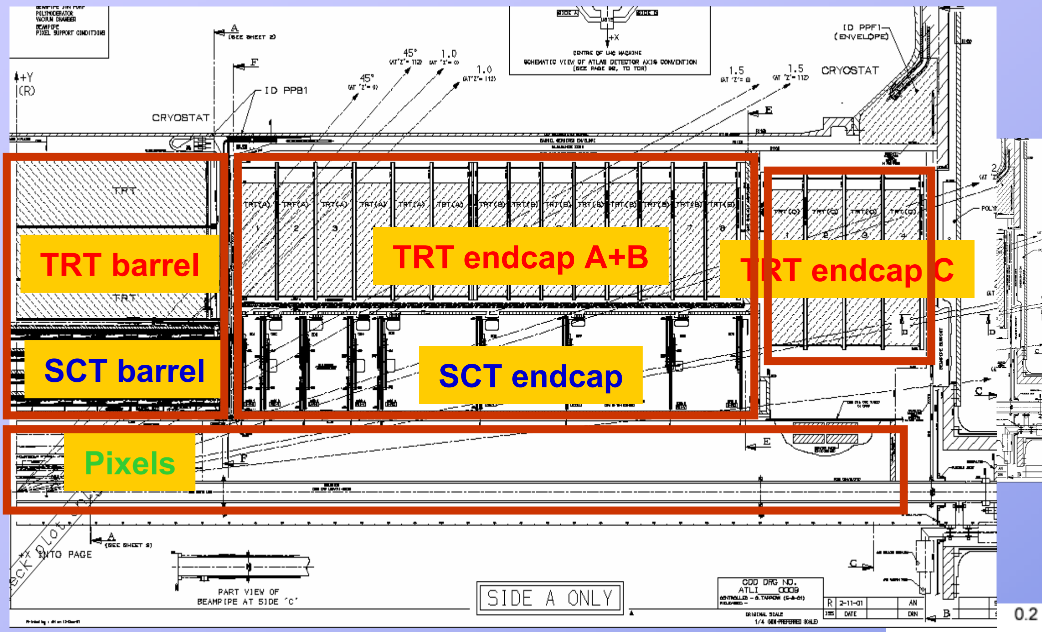
Jul 04 http://agenda.cern.ch/fullAgenda.php?ida= a041379

Goals for ATLAS (CMS) Upgrade @ 10^{35}

- **Detector Performance**
  - Strive to have same detector performance @ 10^{35} as will be achieved @ $10^{34,33}$
    - Energy stays the same
    - Needed for rare modes such as H -> $\mu\mu$, H-> Zγ, Z_L-Z_L
    - Physics emphasis may narrow to study of massive objects produced centrally decaying
    - Some compromises may be necessary, e.g. less coverage at high $|\eta|$
- **Detector Reliability**
  - Strive to have detector elements and electronics sufficiently rad-hard as to be able to run for long periods @ 10^{35} (~1,000 fb^{-1}/yr)
    - Assume that replacement of components on ~ one year time scale would be unacceptable
- **Upgrade R&D Program to be mindful of these goals**
  - Detailed simulation of radiation environment @ 10^{35} : scaling possible?
- **For ATLAS, upgrade of Inner Detector (Tracker) is highest priority**

No subsystem is entirely in the clear - extending operation to 10^{35} will pose problem

ATLAS ID Upgrade



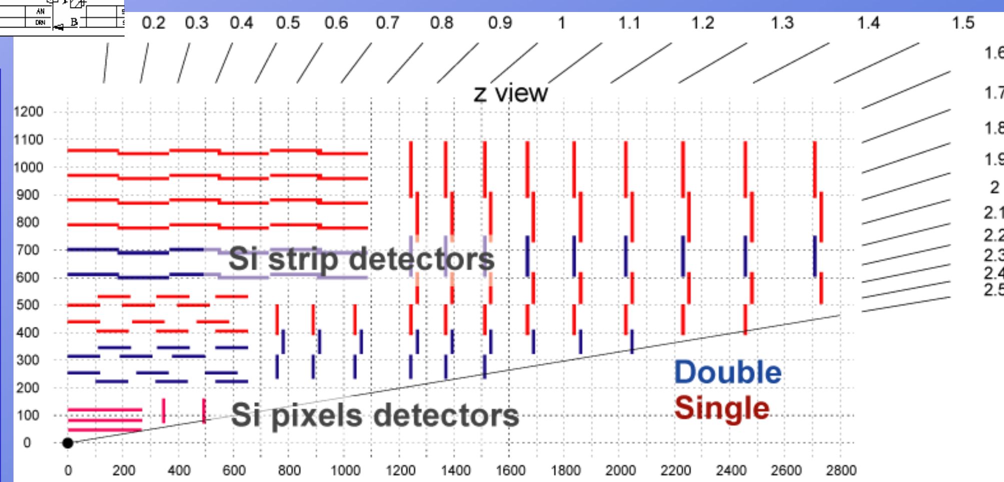
ATLAS Upgrade Steering Group

US-ATLAS Upgrade Program:

- Strip Electronics (SiGe)
- Module Integration
- Short strips (p-type and 2D)
- 3D detectors
- Pixel electronics

Replace entire ID (200m²)

Keep Modularity
-> (Pixels, Barrel, 2 endcaps)
Catch up with CMS:
-> replace gaseous TRT detectors
Find Rad-hard Sensors
Optimize Sensor Geometry
Increase Multiplexing



The layout of the CMS inner tracker

sATLAS Tracker Regions

Integrated Luminosity
(radiation damage) dictates the detector technology

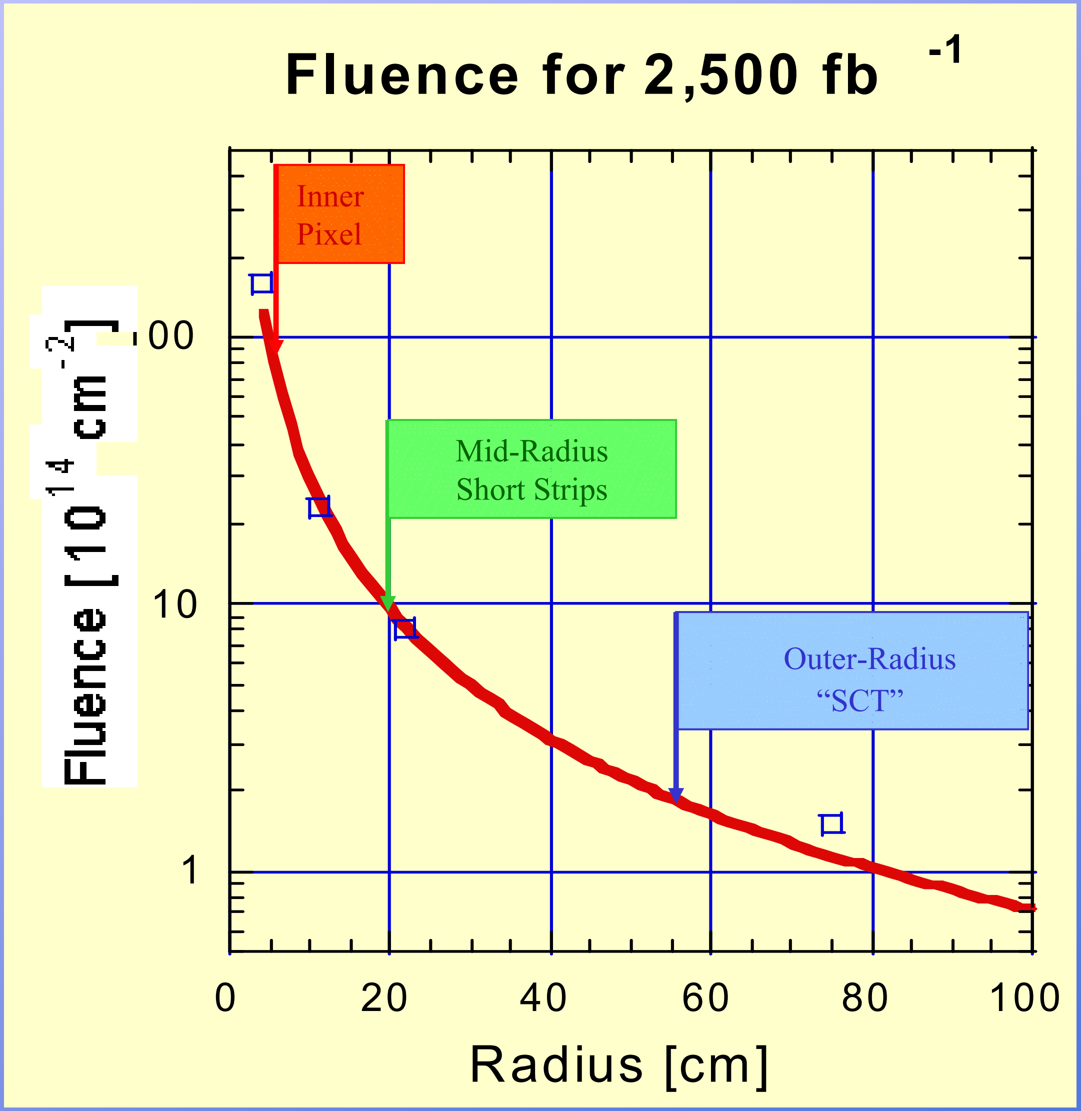
Instantaneous rate
(particle flux) dictates the detector geometry

Straw-man layout (Abe Seiden):

Inner: 6 cm ≤ r ≤ 12 cm
3 layers pixel
pixels style readout

Middle: 20 cm ≤ r ≤ 55 cm
4 layers short strips
space points

Outer: 55 cm ≤ r ≤ 1 m
4 layers "long strips"
single coordinate



Pile-up, Occupancy

The 10x higher luminosity increases the rate of min.bias events

For 10^{34}, occupancies and cluster merging are less severe (x2) in pile up events than in B jets from Higgs decay. At 10^{35} the situation is reversed by ~ x 5.

Solution:

Adjust geometry of detectors to radius, can scale from SCT :

Reduce detector length from 12 cm to 3cm, at twice the radius -> factor 16 less occupancy.

OR use 6 cm long detectors at twice the radius with 12.5 ns bucket timing.

A major constraint on the tracker is the existing ATLAS detector

- Implies a maximum radius of about 1m and a 2 Tesla magnetic field.
- Gap for services is a major constraint.
- Limited Granularity?

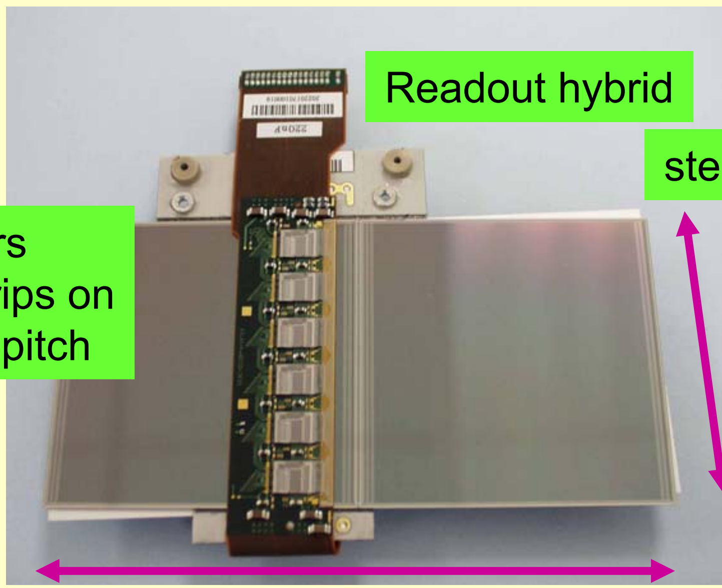
  (Outer silicon layers require more services than the TRT!)

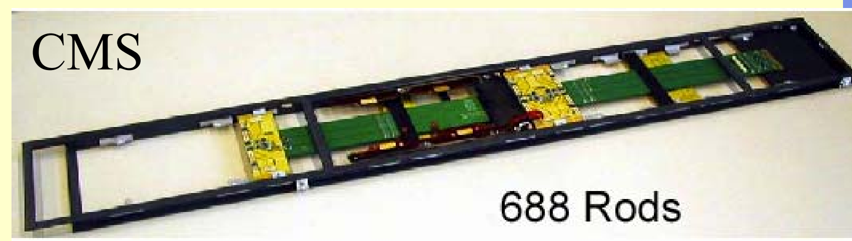
  Space available does not allow for the increase due to granularity.

Region of Outer-Radius r > 55 cm

No SSD problems are expected for the outer region – if the detectors work at the LHC!-

But the limited space in the outer region (r > 50 cm) will require careful tradeoffs between detector length, F.E. power, noise and amount of multiplexing and granularity.





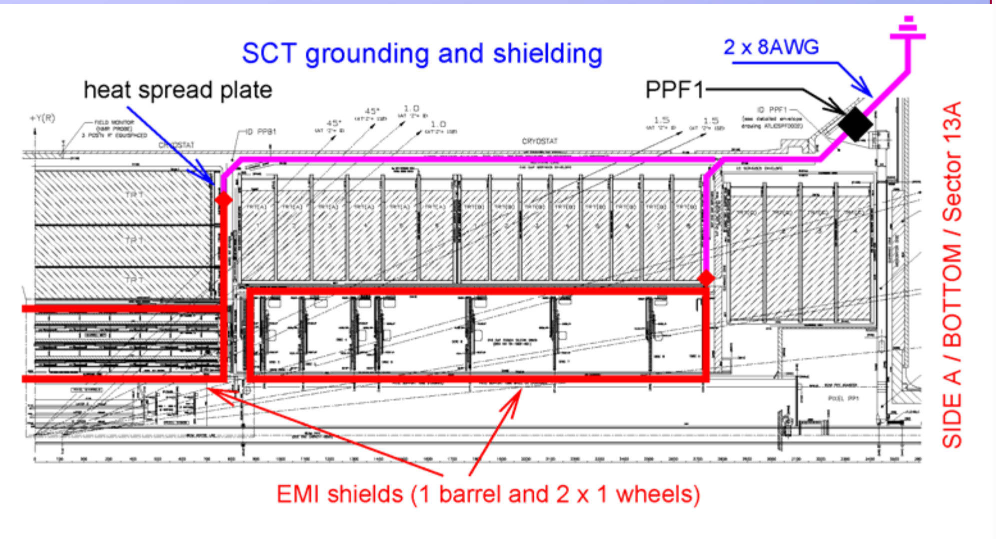
Future ATLAS sID “Stave” ?
(a la CMS and CDF)
between 20cm and 1m
Allows testing of
large Sub-Assemblies

Present SCT Module used between 30 and 57 cm

Material Reduction Challenge: FEE Problem!

ATLAS

Many Modules = Many Servives

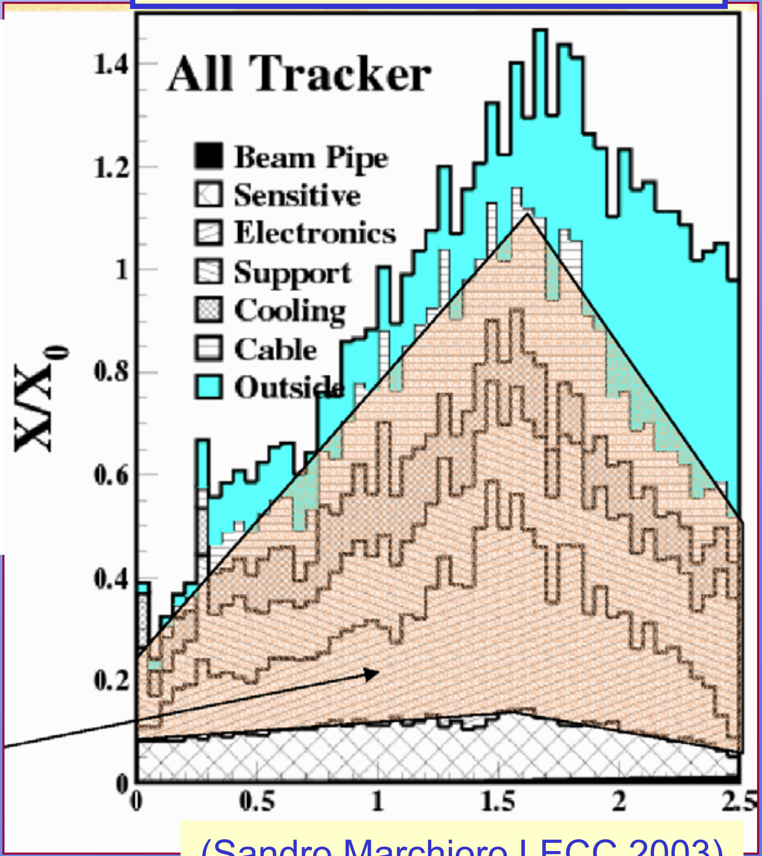


CMS ALL Si TKR:

10% Active detector

10% Support

80% “Electronics”



(Sandro Marchioro LECC 2003)

Increased Multiplexing required

Region of Mid-Radius 20 cm < r < 55 cm

Scaling of the SCT rates allow a readout region of about 80 μm x 1 cm

but this is too coarse a z – measurement.

Options:

(1) Short-strips (long-pixels) with dimension of order 80 μm x 2 mm.

Requires very many channels (power).

(2) Longer detector dimensions (3 cm length), coupled with faster electronics.

With improve rise-time by a factor two (assuming machine crossing frequency is doubled) get a factor of 4 due to detector length and a factor of 2 due to electronics wrt present SCT, compensating for higher luminosity.

Small-angle stereo arrangement similar to present SCT:

Confusion area in matching hits in the back-to-back stereo arranged detectors is proportional to the detector length squared.

Compared to the present SCT, confusion would be reduced by factor of 16 due to reduced length and factor of 2 due to faster electronics, I.e. improvement wrt present ATLAS.

Sensors for Mid-Radius Region 20 cm < r < 55 cm

Short Strips ~ 3 cm long

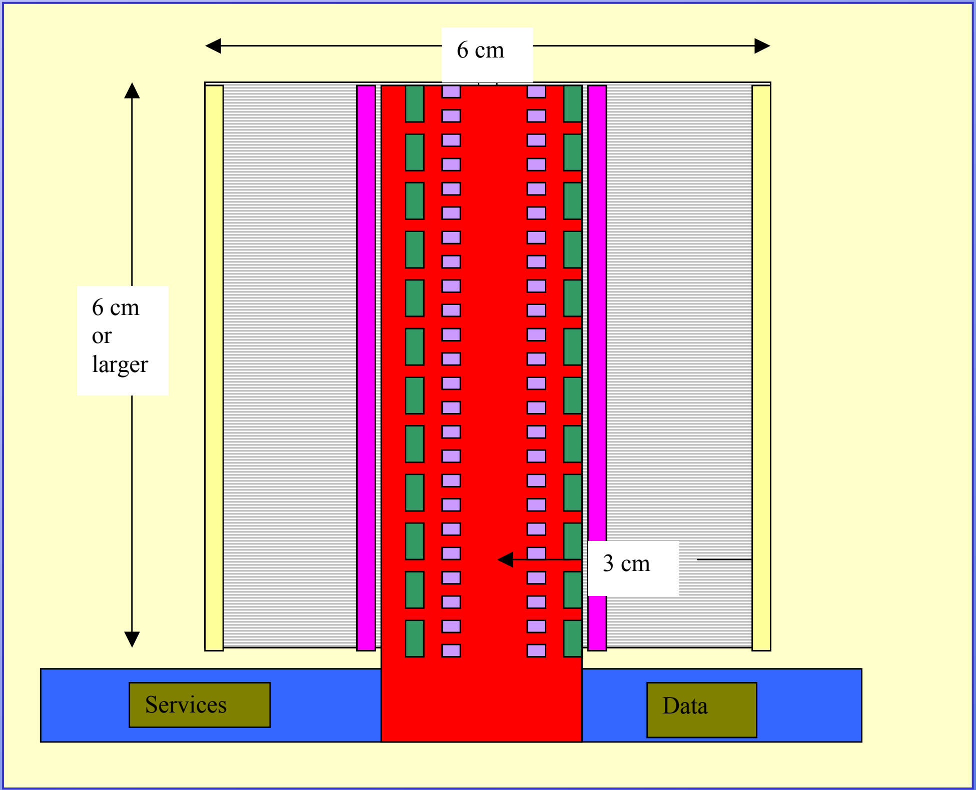
2 sets on one detector with hybrid straddling the center a la SCT

Single-sided

$\sigma_z \approx 1\text{cm}$

Back-to-back single-sided stereo

$\sigma_z \approx 1\text{mm}$



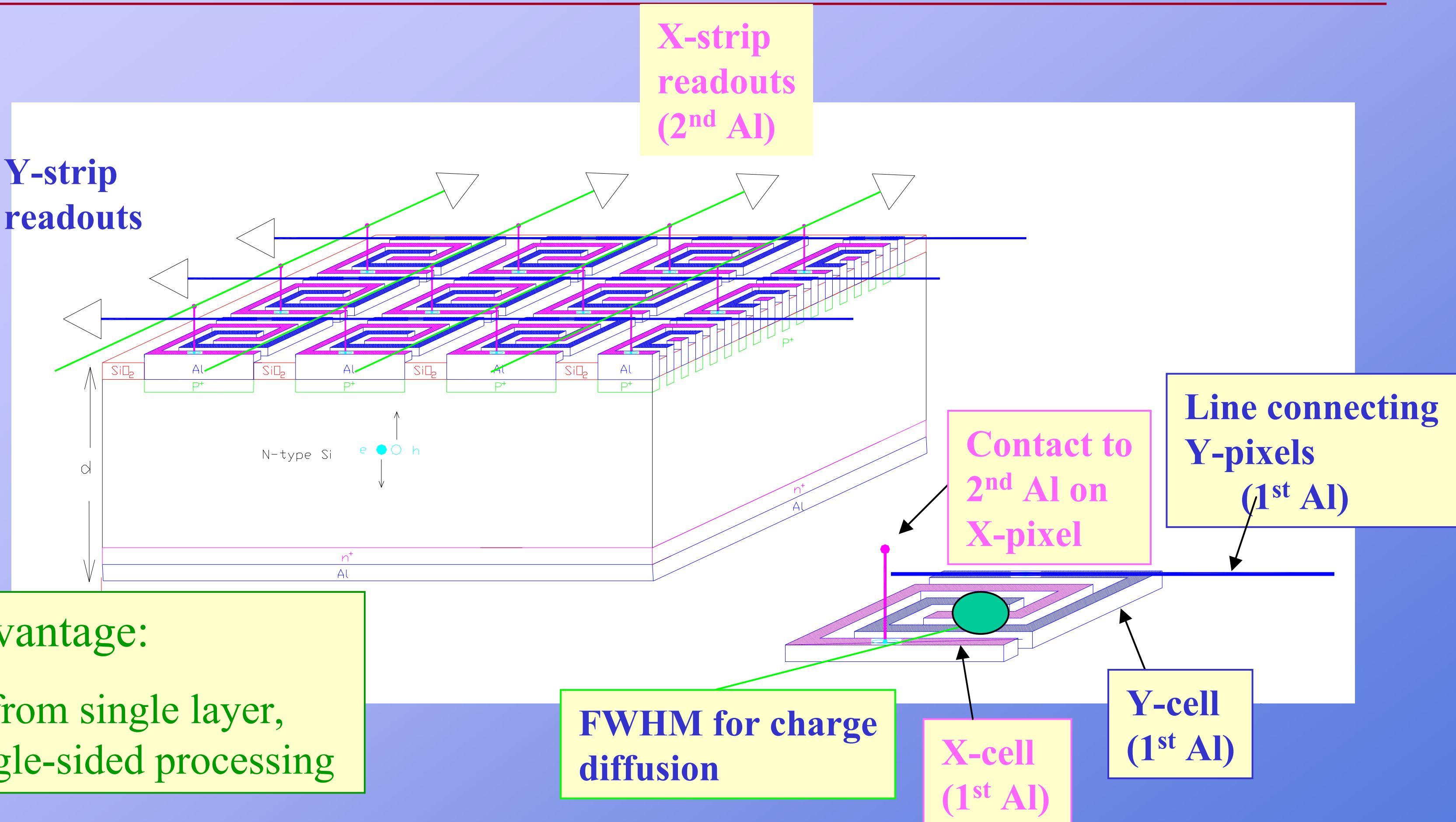
Explore availability of p-type substrates (RD50)

No type inversion

Collect electrons

Partial depletion operation (increased headroom)

2D Interleaved Stripixel Detector (ISD)



Advantage:

2d from single layer,
Single-sided processing

Disadvantage:

½ signal (charge sharing), 2-3 (?) times higher capacitance

BNL

Z. Li et al.

sCMS Pixels

Detailed Pixel System Layout

(including power & price tag)

Roland Horisberger

CMS: Inside out
“Fat” pixels, strips

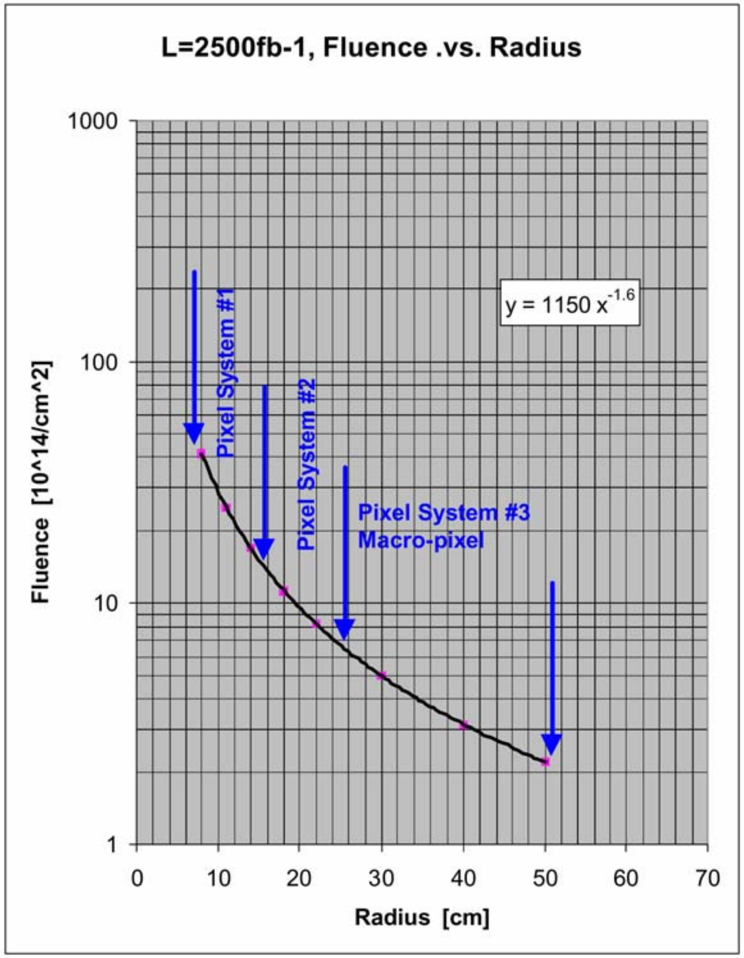
ATLAS Outside in
“Skinny” strips, pixels

Summary

- Propose 3 Pixel Systems that are adapted to fluence/rate and cost levels

- Pixel #1 max. fluence system ~400 SFr/cm²
- Pixel #2 large pixel system ~100 SFr/cm²
- Pixel #3 large area system Macro-pixel ~40 SFr/cm²

- 8 Layer pixel system can eventually deal with 1200 tracks per unit pseudo – rapidity
- Use cost control and cheap design considerations from very beginning.
- Can this be done for 2012/13 ????



Signal :Performance Targets

sLHC Tracker has 3 radial regions with 10x fluence increase

" move LHC systems outward"

Based on present performance, (i.e. without drastic improvement of electronics), guess at a specification of the collected charge needed in the 3 regions:

Radius [cm]	**Fluence [cm^{-2}]**	**Specification for Collected Signal (CCE in 300 um)**	**Limitation due to:**	**Detector Technology**
> 55	10^{14}	20 ke$^-$ (~100%)	Leakage Current	"present" LHC SCT Technology, Consider: n-on-p
20 - 55	10^{15}	10 ke$^-$ (~50%)	Depletion Voltage	"present" LHC Pixel Technology ? Consider: n-on-p
< 20	10^{16}	5 ke$^-$ (~20%)	Trapping Time	RD50 - RD39 - RD42 Technology 3-D!

Signal:Trapping

Charge trapping in Si SSD:

Collected Charge Q = Q_o*ε(depletion)* ε(trapping)
ε(depletion) depends on V_{bias} , V_{dep} -> effective detector thickness w

ε(trapping) = $\exp(-\tau_c / \tau_t)$,
τ_c : Collection time, τ_t : Trapping time

Trapping time is reduced with radiation damage:
(RD50, Krasel et al. for electrons/holes, measured up to 10^{15} cm^{-2} in n-type
$1/\tau_t = 5*(\Phi/10^{16})\ ns^{-1}$)

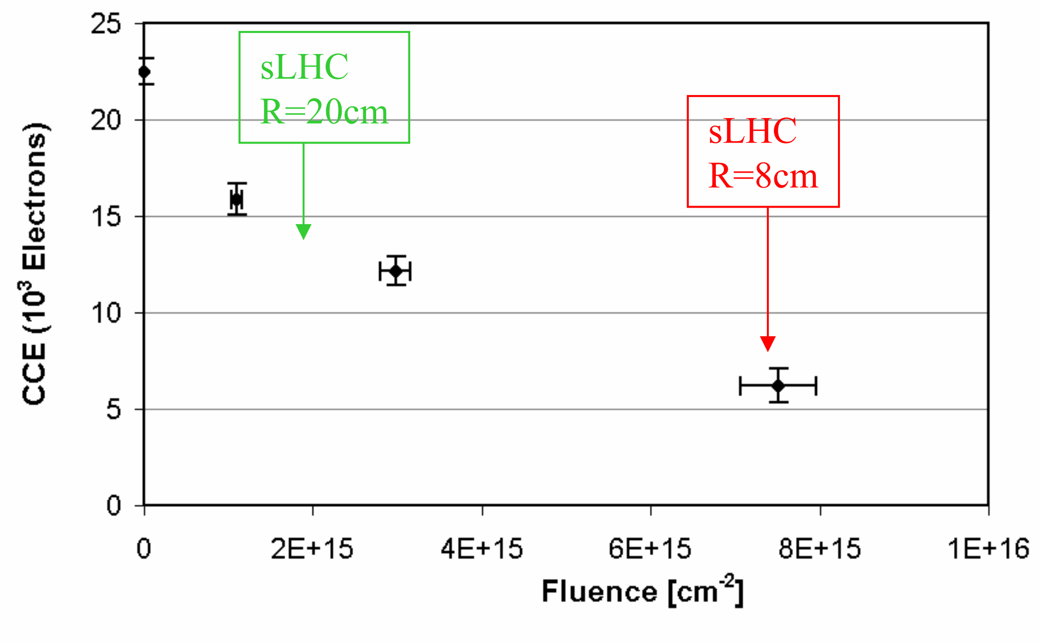
Trapping time $\tau_t \sim 1/\Phi$ (but collection time saturates at high fields!)

$\tau_t = 1.8$ ns for $\Phi = 1.1*10^{15}\ cm^{-2}$
$\tau_t = 0.2$ ns for $\Phi = 1.0*10^{16}\ cm^{-2}$

Charged Trapping in Si: the Good News

Efficiency of Charge Collection in 280 um thick p-type SSD

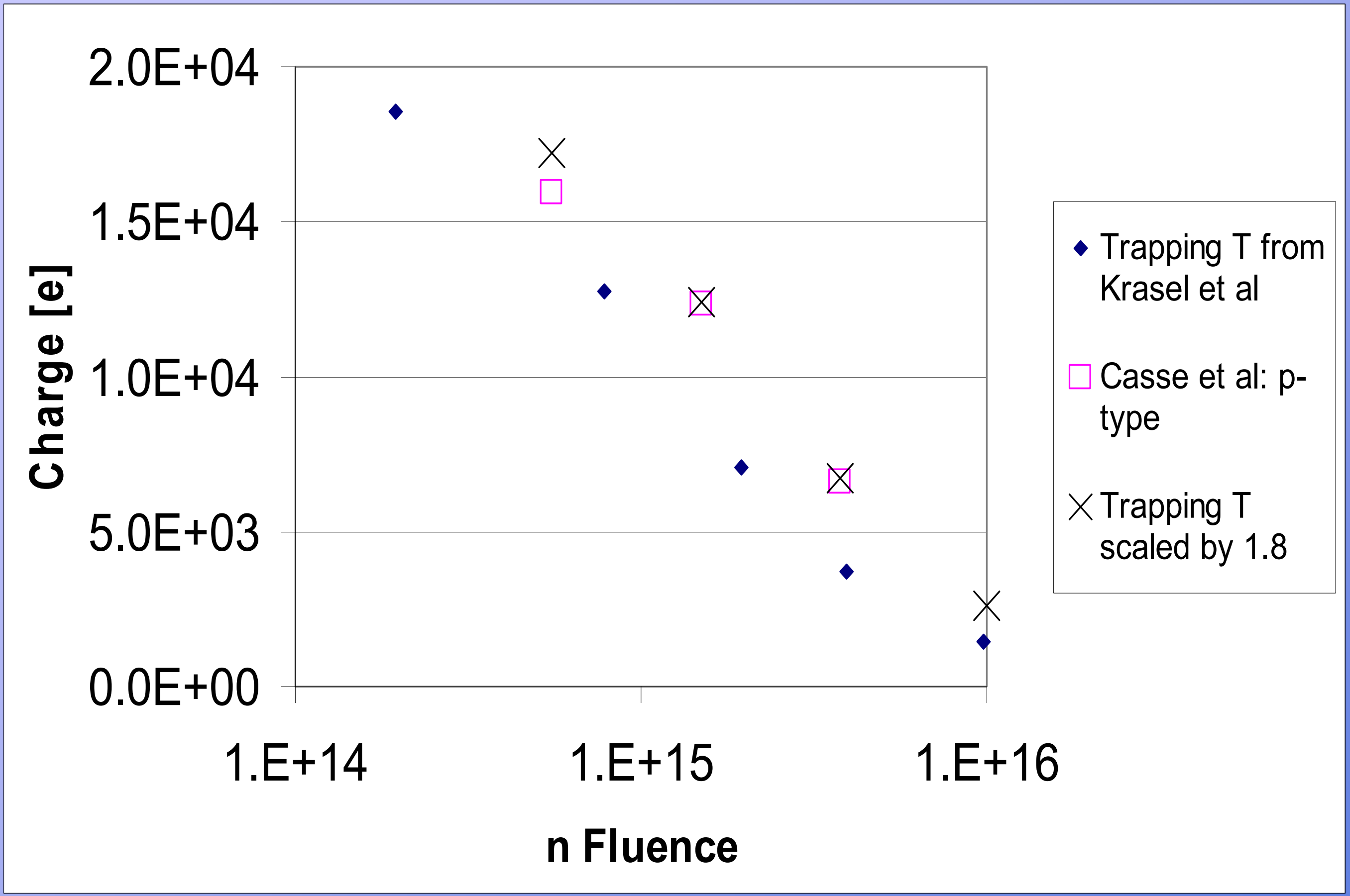
G. Casse et al., (RD50): After 7.5 $*10^{15}$ p/cm^2, charge collected is > 6,500 e^-



Charge collection in Planar Silicon Detectors might be sufficient for all but inner-most Pixel layer?

For 3-D after 1 $*10^{16}$ n/cm^2, predicted charge collected is 11,000 e^-

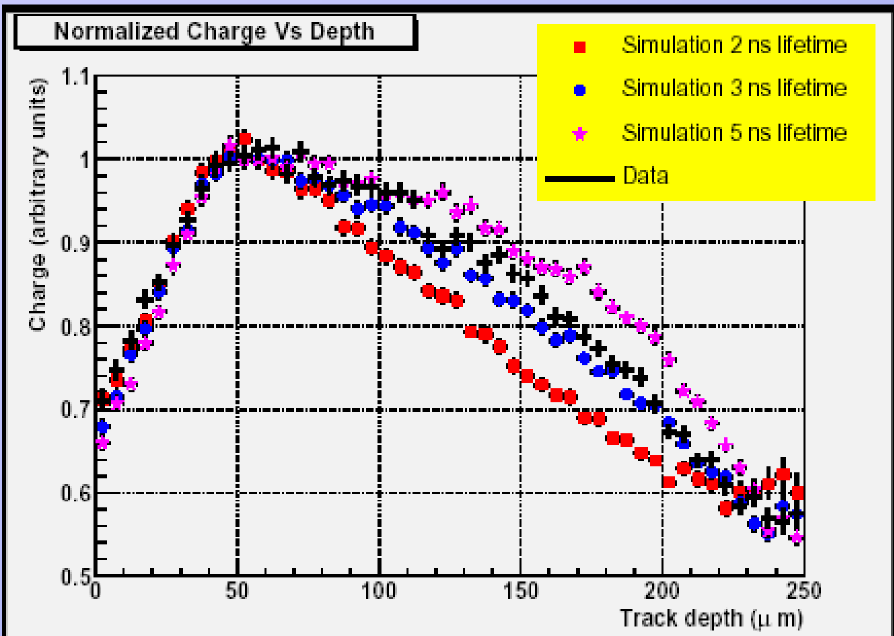
Charge collection in P-type SSD

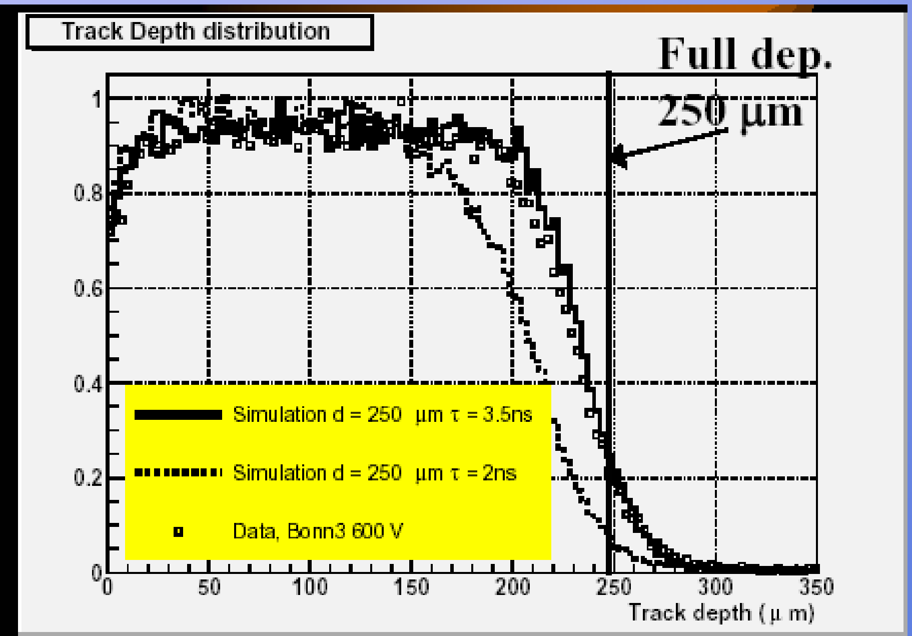


Trapping times 1.8 x larger
than extrapolated from previous measurements.
Difference p-type vs. n-type?

Signal of ATLAS pixel beam test data

T. Lari (previous analysis by T. Rohe et al.)



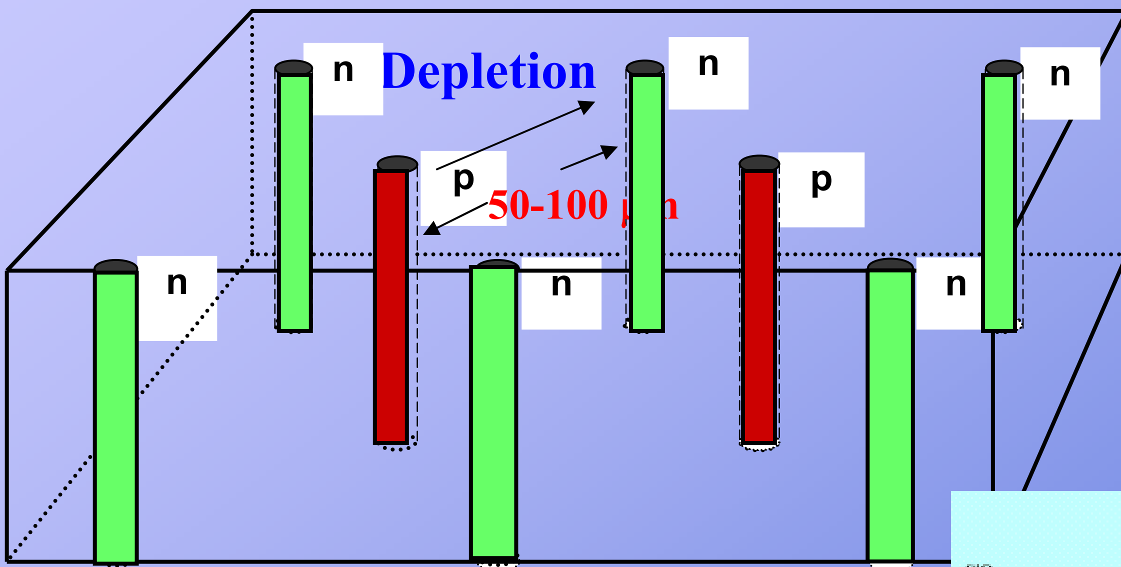


For fluence of $1.1*10^{15}$ n/cm^2 τ_t = 3.5 ns
(i.e. 2x measurement of Krasel et al.)

3-d Detectors

Differ from conventional planar technology, p^+ and n^+ electrodes are diffused in small holes along the detector thickness ("3-d" processing)

Depletion develops laterally (can be 50 to 100 μm): not sensitive to thickness



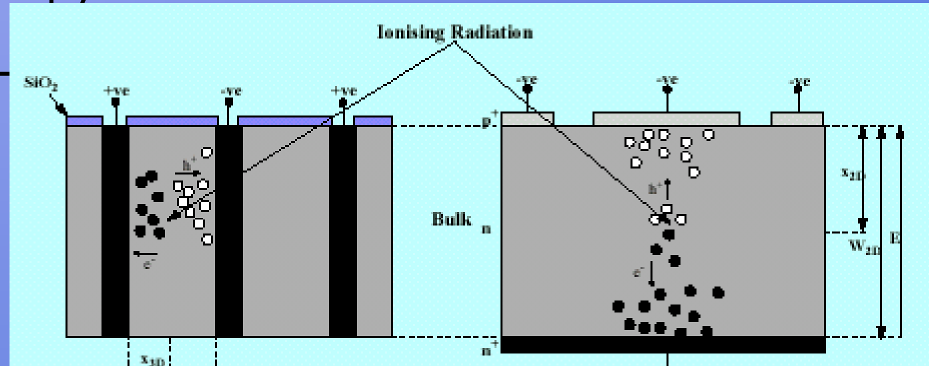
Sherwood Parker et al.,
Edge-less detectors

De-couple depletion / collection

from charge generation:

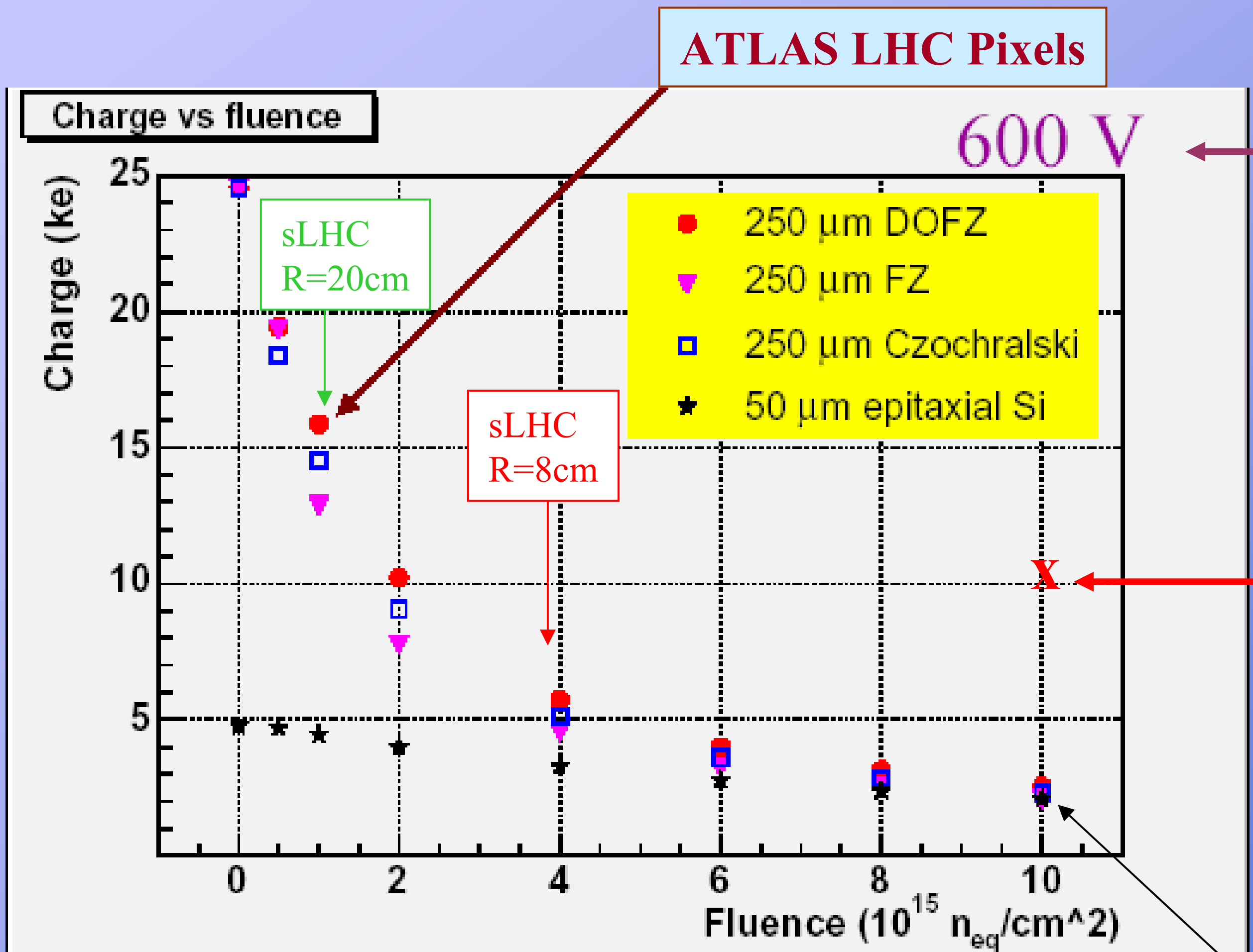
Generated charge ~ thickness

Collected charge ~ electrode distance



Equal detectors thickness
$W_{2D} >> W_{3D}$

Evaluation of collected charge



Redo at higher Bias Voltage?

Estimate for 3D

Lari et al

Trapping is the great equalizer

Detector Materials for Pixels for R ≈ 6 cm

Material		Collected Signal After $10^{16}cm^{-2}$	Comment
Si	RT	~ 2.5 ke^-	Depletion, Trapping
Si -Epi	RT	~ 2 ke^-	Small signal at intermediate fluences,
Si	Cryo	?	Cryo Engineering
Si	3-D	~ 11 ke^-	Efficiency "Holes"?
SiC	Epi	< 2 ke^-	Trapping? Slow collection Cost of wafers
Diamond	Poly	< 3 ke^- ?	Trapping ? Cost of wafers?
Diamond	Single	"Same as Poly?"	Trapping ? Cost of wafers?

Signal-to-noise

Signal-to-noise ratio S/N is essential for performance of the tracking system.

RMS noise σ [electrons]

depends on shaping time and size (i.g. C, i) of the detector channel

Threshold Thr

set to suppress false hits Thr = n* σ + threshold dispersion

SCT: $\sigma \approx 600+C*40 \approx 1500e$, n = 4, --> Thr ≈ 6,000e

Pixels: $\sigma = 450e$ n = 5, --> Thr ≈ 2,500e

threshold dispersion = 300

Since single-bucket timing is needed, use short shaping times $\tau_R = 15ns$.

yet there is still a problem with time walk: signal is in time

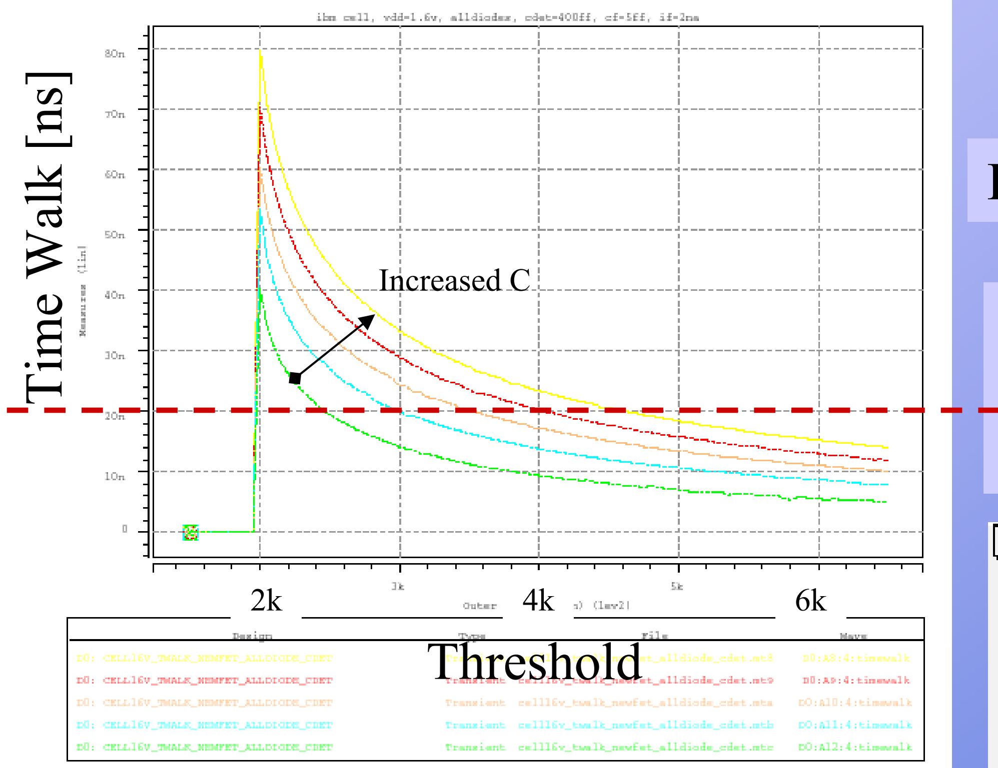
only if it exceeds the threshold by large amount ("overdrive")

"In-time threshold" = physical threshold + overdrive ≈ 2* physical threshold

Average signal must exceed the "In-time threshold"

Time walk for fast shaping

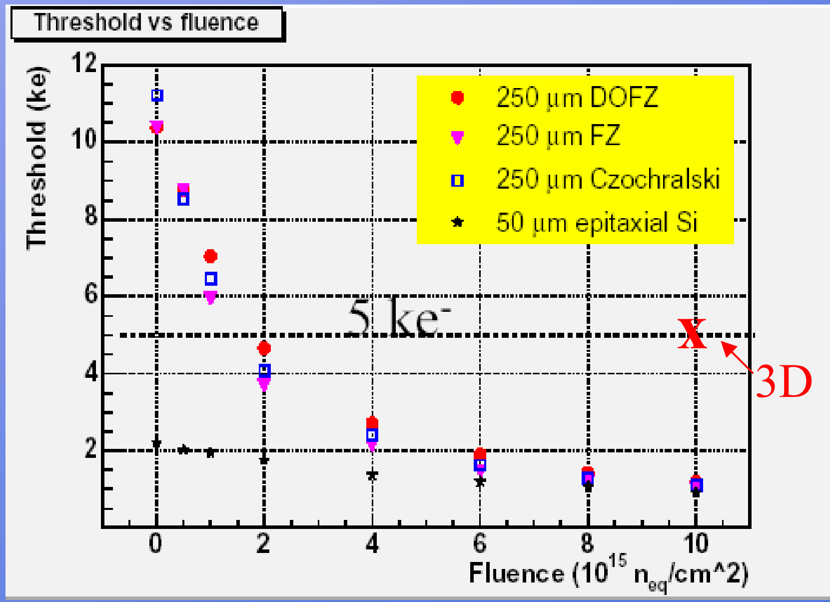
•Timewalk performance (relative to 100Ke) with Cfb=5ff, for CDet from 0f



•Overdrive for Cfb=5fF and CDet=200fF predicted to be only 1500e for 2(
timewalk. For CDet=400fF, this deteriorates to 2500e.

Einsweiler et al

Time walk < 20 ns
= 2.5 ke overdrive
-> in-time threshold =5ke



T. Lani prediction:
In-time Threshold required ≈ 0.5*Q
Optimistic: assumes smaller pixels

Required Frontend Noise

Assume:

In-time Threshold ≈ ½*Signal

σ ≈ (In-time threshold - overdrive)/5

σ ≈ 0.1 * (In-time threshold)

Required noise figure for Planar Detectors:

σ = 1500 e for $1*10^{15}$ (sLHC outside 20 cm) "easy" for short strips?

σ = 500 e for $2*10^{15}$ (present ATLAS/CMS pixel)

σ = 100 e for $1*10^{16}$ (+ very little dispersion)

very tall order for hybrid pixels!

(smaller pixels still have finite inter-pixel capacitances)

F.E.E. Technologies for sLHC:

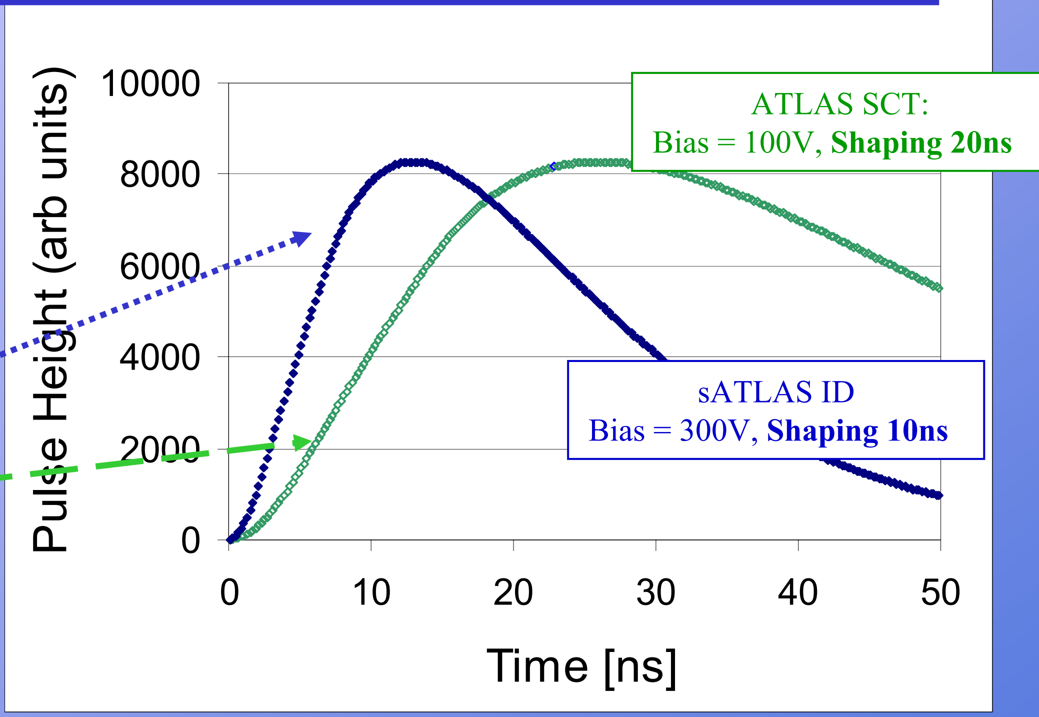
Sub-μ CMOS	"accidentally" rad-hard, low power, used for pixels,CMS, also in sCMS
Bipolar BiCMOS	power-noise advantages for large capacitances and fast shaping, also excellent matching technologies used in ATLAS SCT are not sufficiently rad-hard beyond the LHC because of current gain β degrading from about 100 to about 40 at $10^{14}cm^{-2}$, limited availability
SiGe BiCMOS	very fast (f_T > 50GHz and β > 200), used in cell phones, backend: DSM CMOS "du jour", available IBM–MOSIS rad hardness has been measured to 10^{14}cm we have now test structures in the CERN beam!
SiGefor sLHC?	Expect that largest area of sLHC tracker will be made of strips, so SiGe could give an advantage, specially for short shaping times (noise, overdrive). (Power (SiGe) < Power (0.25 μm CMOS) for "long" strips).

Single-Bucket Timing

Pulse rise time depends on both charge collection and shaping time
If rise time falls within the clock cycle, single-bunch timing is possible

Decrease collection time with increased bias voltage

p-on-n (n-on-p even faster) (M.Swartz)	Collection Time [ns] 100V	300V
Holes	**14**	**7**
Electrons	**5**	**2.5**



With 20ns shaping and 100V bias, do single-bunch timing at LHC (25ns)
With 10ns shaping and 300V bias, the entire rise of the pulse is within 12 ns:
80MHz single-bunch timing is possible for sLHC, reducing occupancy by 1/2

Summary

The LHC luminosity upgrade to 10^{35} $cm^{-2}s^{-1}$ (sLHC)

- allows to extend the LHC discovery mass/scale range by 25-30%
- extends the LHC program in a efficient way into 2020

sLHC looks like giving a good physics return for modest cost

⇒ Get the maximum out of the (by then) existing machine

"Big Bang for the Buck" "No-brainer"

The sLHC will be a challenge for the experiments:
Detector R&D has started now to upgrade the Inner Tracker to all Si in order to be ready to "go" soon after 2013/2014

Layout is driven by particle flux (->short strips!) which counters the need to incrase multiplexing

Expectation is that detector technology is close (in hand?) for all but the inner-most pixel layers.

Electronics will face major challenges: S/N, Power, Services