Evaluation of the Radiation Tolerance of SiGe Heterojunction Bipolar Transistors Under 24GeV Proton Exposure

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***Abstract*-For the potential use in future high luminosity applications in High Energy Physics (HEP) (e.g. the Large Hadron Collider (LHC) upgrade), we evaluated the radiation hardness of a candidate technology for the front-end of the readout Application-Specific Integrated Circuit (ASIC) for silicon strip detectors. The devices were a variety of Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) manufactured by IBM in a modified 5HP process.**

The current gain as a function of collector current has been measured at several stages: before and after irradiation with 24 GeV protons up to fluences of 10^{16} p/cm^2, and after annealing at elevated temperature. The analog section of an amplifier for silicon strip detectors typically has a special front transistor, chosen carefully to minimize noise and usually requiring a larger current than the other transistors, and a large number of additional transistors used in shaping sections and for signal-level discrimination. We will discuss the behavior of both kinds of transistors, with a particular focus on issues of noise, power and radiation limitations.

I. INTRODUCTION

Bipolar circuits using SiGe technology have potential advantages when compared with Complimentary Metal Oxide Semiconductor (CMOS) for fast shaping times and large capacitive loads. As a front device for large detector loads and fast shaping times, SiGe bipolar devices have excellent noise/power ratios, minimal base resistance, and high output impedance. For fast shaping times, SiGe bipolar devices have very efficient bandwidth/power ratios. Thus they are good candidates for the technology choice of the front-end of readout ASICs for the silicon strip detectors planned for the LHC upgrades, if their radiation hardness up to a fluence level of 10^{15} p/cm^2 can be proven.

In a future high luminosity collider, e.g. the LHC upgrade, the instantaneous flux of particles dictates the detector geometry as a function of radius. In the inner detector layers, pixel detectors will be needed, and their small capacitances allow the use of deep sub-micron CMOS as an efficient readout technology.

Starting at a radius of about 20 cm, short strips can be employed, with a detector length of about 3 cm and capacitances of the order of 5 pF. This is the region where the accumulated fluence over the detector lifetime is about 10^{15} p/cm^2. At a radius of about 60 cm, the expected fluence is about a few times 10^{14} p/cm^2, and longer strips of about 10 cm with capacitance of 15 pF can be used. In the two outer regions where bipolar SiGe might be used in the front-end readout ASICs, power savings and fast shaping to identify the beam time crossing are important requirements.

We present the measurements of the current gain as a function of collector current for a variety of SiGe heterojunction bipolar transistors manufactured in a modified 5HP process, taken before and after irradiation at fluences up to 10^{16} p/cm^2, and after annealing at elevated temperature.

The data allows the design and layout of prototype front-end ASICs and their optimization with respect to noise performance as a function of strip length and with respect to power consumption.

II. DEVICES

The devices were a variety of SiGe heterojunction bipolar transistors (HBTs) manufactured in a modified 5HP process, listed in Table I, together with their measured current gain β for a fixed collector current I_c = 150 μA, pre-rad, post-rad after a fluence of 3.5×10^{14} and 1.3×10^{15} p/cm^2 and post-anneal.

TABLE I
TRANSISTOR SIZES AND MEASURED CURRENT GAIN, β, FOR I_C =150 μA.

	Fluence [p/cm^2]					
	3.5×10^{14}			1.3×10^{15}		
Transistor Size [μm^2]	β_{pre}	β_{irrad}	β_{anneal}	β_{pre}	β_{irrad}	β_{anneal}
0.5 x 1				200	80	105
0.5 x 2.5	260	130	190	270	65	89
0.5 x 10	267	89	142	258	40	81
0.5 x 20	271	74	131	260	28	62
4 x 5	324	121	177	325	51	96

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III. IRRADIATIONS

The irradiations were performed in October 2004 at CERN with 24 GeV protons as part of the common RD50 project. The following fluence steps were taken: 4.15×10^{13}, 1.15×10^{14}, 3.50×10^{14}, 1.34×10^{15}, 3.58×10^{15}, 1.05×10^{16} p/cm^2. The devices were irradiated with all terminals grounded. Studies indicate this is a worst-case scenario compared to irradiation under operating bias conditions [1]. The irradiations were performed at room temperature at constant flux (with the highest fluence taking 5 days); then the parts were kept in a freezer at –23 ºC before being re-measured. Annealing was performed for 11days at room temperature, followed by one day at 60 ºC, and one day and additional 6 days at 100 ºC.

IV. RESULTS ON TRANSISTOR PERFORMANCE

A. *Forward Gummel Plots Pre-rad and Post-rad*

The Forward Gummel plot (Fig. 1) for the fluence of 1×10^{15} p/cm^2 shows the degradation in the base current after irradiation and annealing . This is the typical response for a SiGe HBT exposed to proton irradiation. Fig. 2 shows the Forward Gummel plot for a 0.5x10 μm^2 transistor at several fluences and after annealing.

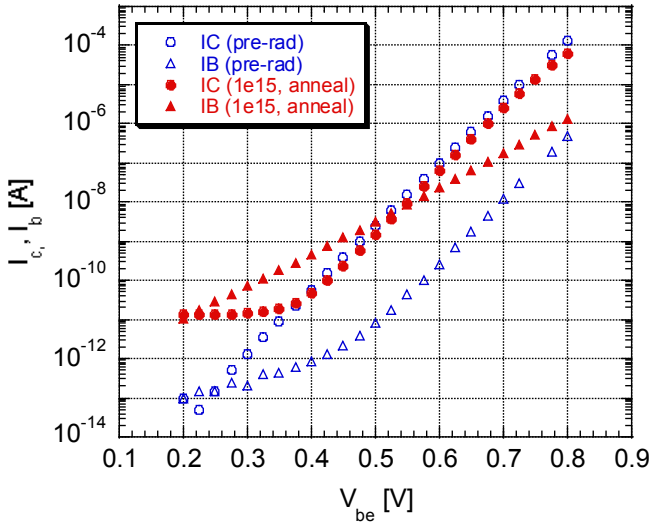

Fig. 1. The Forward Gummel plot for a 0.5x2.5 μm^2 SiGe HBT at 1×10^{15} p/cm^2. After irradiation and annealing, the base current increases substantially while the collector current remains the same causing the gain of the device to decrease.

B. *Radiation Damage Mechanisms*

The structural design of SiGe HBTs lends itself to a strong immunity to radiation damage. The small active volume of the transistor reduces the effects of displacement damage. The emitter-base spacer (the spot most susceptible to damage) is also relatively thin and comprised of an oxide/nitride composite, which increases radiation tolerance. Even the location of the base directly below the EB spacer contributes to radiation tolerance [2].

There are two principal mechanisms that cause radiation damage—ionization damage and displacement damage (DD). Ionization damage creates oxide trapped charges and interface states in the EB spacer, consequently increasing the base current and degrading the gain of the device as shown in the Forward Gummel plot in Fig. 2. The displacement damage shortens hole (minority carrier) lifetime, which is inversely proportional to the base current, thus degrading the base current and gain [2], [3]. A comparison of the radiation damage of different device geometries reveals that ionization effects are the major cause of the radiation damage. The squarish 4x5 μm^2 device shows significantly less degradation than the longer rectangular devices (see Fig. 5 and 6) probably due to the relatively smaller oxide layer area where the ionization damage occurs.

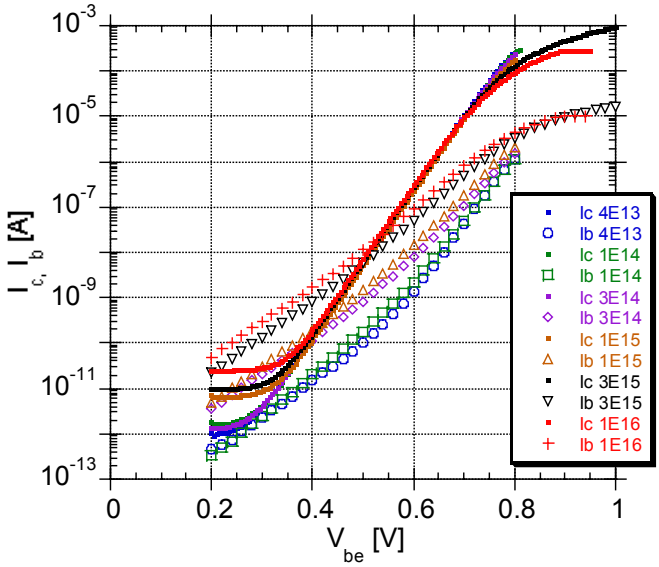

Fig. 2. The Forward Gummel plot for a 0.5x10 μm^2 device for several fluences. The base current I_b increases with increasing fluence while the collector current I_c is relatively unchanged causing the gain of the device to degrade.

C. *Annealing effects*

Annealing appreciably improves the post-radiation performance [4]. Annealing was performed for 11days at room temperature followed by one day at 60 ºC, and one day and then an additional 6 days at 100 ºC. Fig. 3 shows the annealing of the current gain β vs. collector currents I_c in these steps for the 0.5x2.5 μm^2 transistor and a fluence of 1.34×10^{15} p/cm^2. Although appreciable annealing is observed, only part of the radiation induced performance deterioration is recovered. The annealing effects are expected to be sensitive to the biasing conditions. We plan to study this in the future.

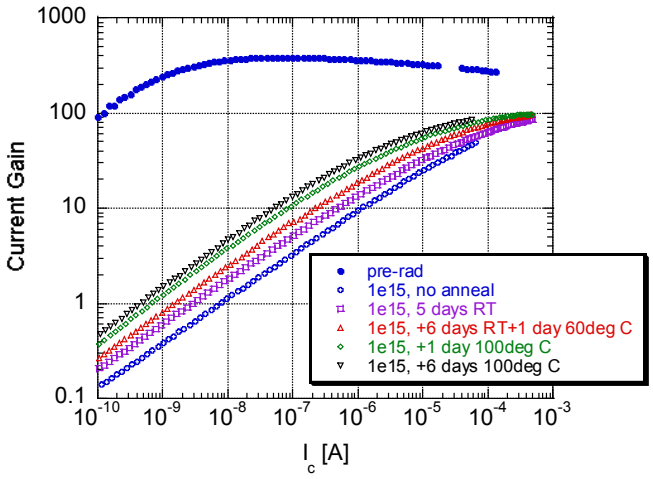

Fig. 3: Annealing of the current gain vs. collector current for a 0.5x2.5 μm^2 transistor at a fluence of 1.3×10^{15} p/cm^2. The device recovers with increased annealing steps. The worst-case scenario is represented by the data taken right after irradiation, but without annealing. Successive anneal steps are shown. The devices were annealed to more closely represent the irradiation conditions seen during real operation of ATLAS Upgrade.

D. Current Gain β Pre-rad and Post-rad

Fig. 4 shows the current gain β vs. the collector current I_c for different fluences, after annealing. The gain degrades with increased fluence as a result of the increased base current.

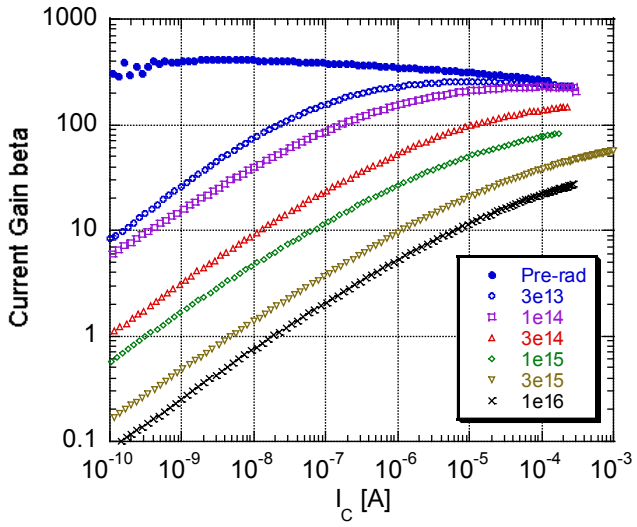

Fig. 4: Current gain β vs. collector current I_c for a 0.5x10 μm^2 device for several proton fluences, including full annealing. The gain of the transistor degrades with increasing fluence. Performance is still acceptable at 3×10^{15} p/cm^2.

The similarity of the radiation induced degradation in performance of different device sizes is shown in Fig. 5 where the current gain ratio post-rad over pre-rad is plotted vs. the fluence for a fixed collector current density of J_c=10 $\mu A/\mu m^2$. As expected, for equal current density, the radiation damage is an unique function of the fluence, independent of the transistor geometry, with the notable exception of the 4x5 μm^2 device. The same fact is shown in Fig. 6, where Δ(1/β), the difference between 1/β post-rad and 1/β pre-rad, is plotted for all devices at the same current density. As expected, the values are about linear with the log of the fluence and agree reasonably well. This allows one to predict the performance of similar devices and will guide further test structure investigation, as well as optimization of noise and power.

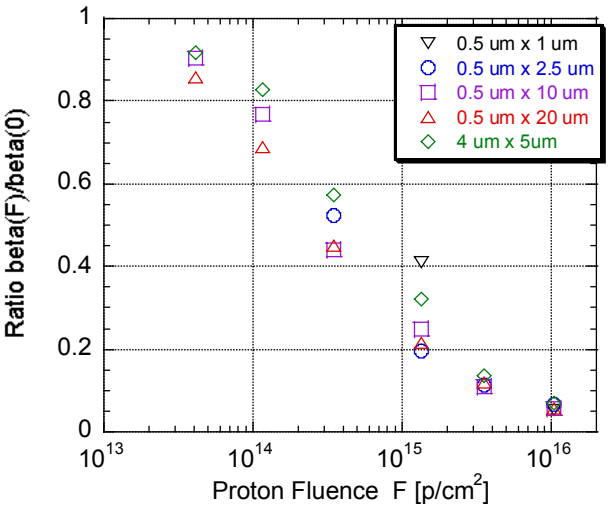

Fig. 5: Ratio of current gain, β post-rad over pre-rad, vs. fluence for all devices at a fixed collector current density of J_c = 10 $\mu A/\mu m^2$, after annealing. The different device geometries now scale as a function of collector current density indicating predictable behavior for the devices.

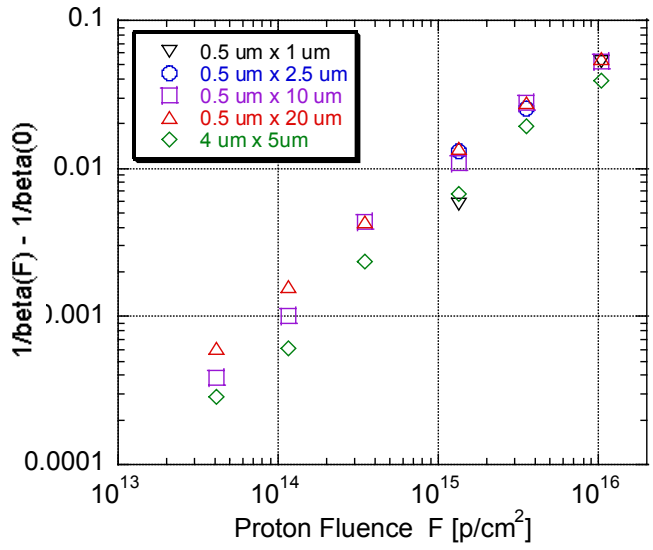

Fig. 6: Difference of 1/β post-rad and pre-rad vs. fluence for all sizes of devices at a fixed collector current density of J_c = 10 $\mu A/\mu m^2$, after annealing. The geometries scale with collector current density. Δ1/β depends little on the initial gain value revealing a tighter linear fit. We also see that the devices with a higher aspect ratio are more affected by radiation damage especially at lower fluences probably due to the larger ratio of oxide to bulk.

Table II shows the current gains pre-rad, after a fluence of 1.34×10^{15} p/cm^2 and after anneal for two fixed current density of J_c = 10 and 50 $\mu A/\mu m^2$, respectively, to be compared with Table I. The radiation effect is essentially independent of the

transistor geometry when equal current densities are considered as discussed below.

Table II
Current Gain β pre-rad, post-rad and post-anneal for the different transistors at two collector current densities for a fluence of 1.3×10^{15} p/cm^2.

	Collector Current Density					
	J_c = 10 μA/μm^2			J_c = 50 μA/μm^2		
Transistor Size [μm^2]	β_{pre}	β_{irrad}	β_{anneal}	β_{pre}	β_{irrad}	β_{anneal}
0.5 x 1	254	28	104	225	47	115
0.5 x 2.5	316	27	62	281	47	85
0.5 x 10	276	27	69	247	50	88
0.5 x 20	265	25	57	225	65	80
4 x 5	318	56	102			

V. CONSIDERATIONS FOR FRONT-END READOUT ASICS FOR SILICON STRIP DETECTORS

As mentioned before, we will consider for the LHC upgrade two different regions where bipolar technology could be used. They are characterized by detector capacitances of about 5 pF and fluences of about 10^{15} p/cm^2 ("short strips"), and capacitances of about 15 pF and fluences of about 10^{14} p/cm^2 ("long strips"), respectively. In the so-called binary readout systems for silicon strips, the front-end consists of an analog amplifier-shaper-comparator circuit followed by a digital data storage and data transfer part. While the front-end is a candidate for bipolar technology, the latter two parts are built with CMOS circuitry, thus requiring a BiCMOS technology. The analog section of an amplifier typically has a special front transistor, chosen carefully to minimize noise and usually requiring a larger current than the other transistors, and a large number of additional transistors used in shaping sections and for signal-level discrimination. Our experience with the design of bipolar front-end readout for silicon detectors [5], [6], indicates that current gains of about β = 50 are required for efficient circuit designs. In Table III, the currents required to reach a current gain β = 50 are shown for the different transistors investigated after a fluence of 3.5×10^{14} p/cm^2 and 1.3×10^{15} p/cm^2, with and without annealing.

Table III
Collector current I_c required to reach a current gain β =50 post-rad and post-anneal after fluences of 3.5×10^{14} p/cm^2 and 1.3×10^{15} p/cm^2.

	Fluence [p/cm^2]			
	3.5×10^{14}		1.3×10^{15}	
Transistor Size [μm^2]	$I_{c,irrad}$ [μA]	$I_{c,anneal}$ [μA]	$I_{c,irrad}$ [μA]	$I_{c,anneal}$ [μA]
0.5 x 1	2.2		30	0.12
0.5 x 2.5	4.6	0.048	72	4.2
0.5 x 10	26	0.8	210	9.3
0.5 x 20	46	1.8	280	58
4 x 5	8.6	0.54	140	13

A. *Short strips*

The currents required for sufficient current gain are very modest even after the expected fluence of 10^{15} p/cm^2. Our annealing data indicate that it will be possible to use SiGe HBT technology throughout the entire front-end with currents approximately 5μA to 10μA. Thus we expect that a bipolar technology of similar radiation tolerance will afford a power and performance improvement in the front-end transistor, which will be biased to the needed ~150 μA current, as well in the remainder of the front-end circuitry. More studies are needed and are currently under way.

B. *Long strips*

The currents required for sufficient current gain are small and make it possible to build the entire analog front-end section in the bipolar technology. The typical currents in the transistors excepting the first transistor will be less than 1 μA, much less than an equivalent CMOS circuit requires [7], resulting in substantial power savings.

VI. CONCLUSIONS

Inherent radiation tolerance of SiGe HBTs make them a leading candidate for design of front-end readout ASICs for use in an upgraded LHC. The technology shows acceptable degradation in current gain at fluences of 3.50×10^{14} and 1.34×10^{15} p/cm^2, which will be reached at the 60 cm and 20 cm radii respectively of the upgraded ATLAS detector. The tested SiGe exhibits far superior performance pre- and post-rad than the BiCMOS technology used for the readout ASIC built for the ATLAS SCT [6].

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