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Operation of Short-Strip Silicon Detectors based on p-type Wafers in the ATLAS Upgrade ID

Hartmut F.-W. Sadrozinski, Abraham Seiden
SCIPP, UC Santa Cruz, CA 95064

Mara Bruzzi
INFN Firenze - Univ. of Florence, Italy and SCIPP, UC Santa Cruz, CA 95064

Abstract

Based on recent data of radiation effects in p-type detectors, the expected performance of planned short silicon strip detectors (SSSD) in the ATLAS upgrade tracking detector are evaluated. The signal-to-noise ratio and power generated will be presented as a function of a set of realistic values for the operating parameters: fluence ($3\cdot10^{14}$, $1\cdot10^{15}$, $3\cdot10^{15}$ neq/cm^2), operating temperature (-30^{o}C, -20^{o}C, -10^{o}C) and bias voltage (400, 600, 800V), detector thickness (200, 300 μm) for both Float Zone (FZ) and Magnetic Czochralski silicon p-type detectors.

1. Reasons for using p-type SSD

Based on the charge collection results from RD50 [1,2], we anticipate p-type (n-on-p) detectors will be the main contender for the Silicon Strip Detectors (SSD) technology in the intermediate region at the LHC upgrade. In that region with radius from ~20 to ~55 cm, occupancy considerations dictate the use of short strip detectors of about 3 cm length. If proven to be reliable, affordable (single-sided processing!) and supported by high-volume manufacturers, p-type might get used in the long strips in the outer region of the upgrade detector beyond a 55 cm radius as well.

The main radiation damage phenomena to SSDs are [3]: an increase of the leakage current, a change in the effective doping concentration at heavy fluences leading to increased depletion voltage, a shortening of the carrier lifetimes due to increased trapping at radiation-induced defects, responsible for a loss of charge, and the appearance of surface effects causing changes in the interstrip capacitance and resistance.

An important effect in radiation damage is the annealing, which can significantly change the detector properties after the end of radiation. Since the times characterizing annealing effects tend to depend exponentially on the temperature, the temperature of operating and maintaining the detectors is constrained by these annealing times [4,5].

As shown below, the character and size of these effects are very much the same in p-type and n-type at very high fluences [6]. A significant difference resides in the fact that defects induced by radiation in Si are dominantly deep acceptor like traps [7]. Radiation damage in p-on-n-detectors will therefore eventually lead to an inversion of the space charge sign (SCSI), so that the region of high field will shift from the strip implants (which are connected to the readout) to the rear electrode of the detector. On the contrary, in p-type Si radiation will increase the effective doping concentration without causing type inversion. For this reason, at high fluences, when the SCSI occurrs, n-type (p-on-n) detectors need to be fully depleted or over-depleted to maximize the collected charge [8].

Thus, in terms of the operation, p-type SSD (like the more expensive n-on-n detectors used in the ATLAS Pixel System [9]) have a critical advantage over the customary n-type SSD: because the signals are collected on the junction side throughout the life time of the detector, the detector can be operated under-depleted, i.e. the bias voltage does not have to exceed the depletion voltage for the detector to be efficient, as in the p-on-n detectors after type inversion.

If the bias voltage is less than the depletion voltage, only part of the detector can be depleted, and only charge created in this "active" thickness can be collected. This applies to n-on-p detectors, but not to p-on-n detectors, which require full depletion.

Trapping of the charge during drift to the electrodes adds to the loss of charge, and here the p-type detectors have the advantage of collecting electrons, which have an almost three times higher mobility than holes.

2. Data on Radiation Damage

Much of the radiation damage data has been collected using charged hadron beams, e.g. the 24 GeV proton beam at CERN. On the other hand, expected fluence levels are often expressed in terms of 1 MeV neutron equivalent. There are important differences between the radiation damage by neutrons and protons, e.g. in the formation of a double-junction in n-type detectors, which will not be discussed here [10]. For most effects, the neutron fluence required to do the same damage as high energy protons is well described by the NIEL hypothesis and scales as 0.62 [5]. Here, the effects are evaluated for protons and attributed to a neutron equivalent fluence of 0.62 magnitude.

To investigate a possible beneficial effect of the increased oxygen concentration in terms of radiation induced defects, within the RD50 CERN collaboration the radiation hardness of both magnetic Czochralski (MCz), Diffused Oxygenated Float Zone (DOFZ) and standard Float Zone (FZ) materials are now investigated as p-on-n and n-on-p detectors [2,7]. It is well known in fact that MCz has a concentration of interstitial oxygen of about 10^{17}-10^{18}cm^{-3}, while in standard FZ Si it is 10^{15}-10^{16}cm^{-3}. Indeed there is experimental evidence that under irradiation with charged hadrons, n-type DOFZ and MCz Si are less prone to type inversion than pure FZ [3,7,8]. This has been related both to a depressed accumulation of the deep radiation induced defect with energy level close to 0.5eV [11] and, especially in MCz, to the creation with radiation of shallow donors [12].

2.1. Annealing

Similar to n-type detectors [4], p-type detectors can show complex annealing effects [13]. The radiation induced increase in leakage current is reduced over a temperature dependent time scale. The leakage current constant α_n for neutrons (see the following section) is usually taken after annealing for 80 min at 60 ^{o}C, which for n-type detectors is $\alpha_n = 4 \cdot 10^{-17}$ A/cm [5], continuing annealing reduces the leakage current logarithmically [13]. Earlier papers comparing n-type detectors made with several n-type FZ wafers of different resistivity, one n-type Czochralski from Polovodice and one low resistivity p-type epitaxial wafer from ITME, Warsaw, showed that the alpha damage constant is independent of the material kind [3,14]. First results on p-type detectors made with high

resistivity Magnetic Czochralski Si irradiated with 24GeV/c and 27MeV protons showed that a value $\alpha_p = 2.5 \cdot 10^{-17}$ A/cm is reached after 2 days at 60 ^oC and after 10 days at room temperature (RT) [13].

The increase in depletion voltage anneals beneficially down to a stable value in > 14 days at RT, in about 20 min at 60 ^oC and about 3 min at 80 ^oC. From the same reference, the observed reverse ("anti-") annealing appears to have a different time scale in MCz and FZ p-type Si: for MCz it starts at about 10 min at 80 ^oC and about 250 min (=4 hrs) at 60 ^oC and much longer than 20,000 min (14 days) at RT, while the p-type FZ anti-annealing starts at about 20 min at 60 ^oC [13]. (For comparison, n-type FZ starts to anti-anneal at about 120 min at 60 ^oC) [3]. This 10-fold time delay in reverse annealing could provide p-type MCz an advantage over p-type FZ, permitting a wider choice in the temperature management.

The charge collection data on p-type FZ of Ref [15] provide a measurement of the annealing of the trapping. During high temperature annealing corresponding to several years at RT, the charge collection efficiency at bias voltages greater than 500 V are constant through the anneal cycle, while the one at 300 V bias drops slightly at large anneal times. These observations are consistent with the assumption that the trapping times are constant during annealing, but that the depletion voltages of the p-type FZ anti-anneal, i.e. increase during the late anneal cycle.

2.2. Leakage current

The fluence dependence of the leakage current increase in silicon is very well established. It is parametrized in terms of the current I per volume as a function of the fluence Φ

$$\frac{I}{Volume} = \alpha \cdot \Phi \qquad (1)$$

with a proton leakage current constant damage for 24 GeV protons $\alpha_P = 2.5 \cdot 10^{-17}$ A/cm quoted at 20°C after canonical annealing [14]. As mentioned above, the leakage current constant depends on the annealing history of the detector, and from the anneal times mentioned in the previous section, it is likely that this value will be reached, even if the detector has to be kept cold to limit the anti-annealing of the depletion voltage. In fact this value for α is conservative, and could well be a factor 2 lower.

It is well known that the leakage current *I* in silicon is mainly originated by the presence of generation-recombination deep levels close to midgap which make the current strongly dependent on the absolute temperature T. If $T_0 = 293K$, the current at T is parameterized as:

$$I(T) = I(T_0)\left(\frac{T}{T_0}\right)^2 \exp\left(\frac{E_b}{2K}\left(\frac{1}{T_0} - \frac{1}{T_0}\right)\right) \qquad (2)$$

with E_b =1.12 eV silicon band gap. This strong dependence is used to lower the leakage current after irradiation by keeping the detector cold. Table 1 shows the relative value of the leakage current constant α at 20, 0, -10, -20, -30^{o}C respectively. If the detector is under-depleted, the volume in eq. (1) will be scaled by the ratio of depletion thickness over physical thickness.

Table 1: Relative leakage current constants α_P for different temperatures

Temperature [°C]	20	0	-10	-20	-30
$\alpha(T)/\alpha(20)$	1	0.197	0.0797	0.0300	0.0104

2.3. Depletion Voltage

First data on Magnetic Czochralski (MCz) and Float Zone (FZ) detectors made on p-type high resistivity ($\rho \geq 1k\Omega cm$) silicon [6,13,16,17,18] have shown that after irradiation the pre-anneal depletion voltage is increasing with fluence. We use an approximate linear fluence dependence for the depletion voltage of 300 μm thick SSD in analogy with n-type FZ:

$$V_{dep} = V_0 + \beta \cdot \Phi \qquad (3)$$

with V_0 (of the order 150 V – 200V) the pre-rad depletion voltage determined by the resistivity of the wafer. The slope β is slightly different for different p-type materials (we estimate $\beta = 2.67 \cdot 10^{-13}$ V/cm^2 for MCz, $\beta = 2.86 \cdot 10^{-13}$ V/cm^2 for FZ from [13,16]). Table 2 shows the expected depletion voltages at 3 target fluences, with V_0= 161 V. The full depletion voltage scales with the square of the thickness of the detector, i.e. for 200 μm thick SSD the depletion voltage is 4/9 of eq. (3).

Immediately after irradiation, the two p-type detector types show very similar operational parameters, but, as mentioned above, first results on p-type detectors [13,17] after irradiation show that there is a large difference between different p-type wafer materials in terms of the annealing time scale, and potentially the amount of anti-annealing.

Careful temperature management might be required, although the ratio of short term to long-term anneal time of about 10 should allow the selection of optimal operating (and annealing) temperatures. The depletion voltage prediction is accurate to 20%.

Table 2: Depletion Voltage for 300 μm p-type SSD vs. Fluence (no annealing treatment)

Fluence Φ [neq/cm^2]	$3 \cdot 10^{14}$	$5 \cdot 10^{14}$	$1 \cdot 10^{15}$	$3 \cdot 10^{15}$
MCz V_{dep} [V]	290	376	591	1451
FZ V_{dep} [V]	299	392	622	1545

The depleted detector thickness w is given by the physical thickness t when the bias voltage V_{bias} is larger than the depletion voltage V_{dep} and scales like the square root of the ratio V_{bias} / V_{dep} when it is smaller.

$$w = t \qquad V_{bias} \geq V_{dep}$$
$$w = w = \sqrt{\frac{V_{bias}}{V_{dep}}} \cdot t \qquad V_{bias} < V_{dep} \qquad (4)$$

The annealing behavior of the depletion voltage is not well understood beyond the rough identification of the annealing times. Fairly substantial reductions of the depletion voltage have been observed, which seem to lead to stable depletion voltage values (before anti-annealing), which are not linear in the fluence [13]. This exciting fact and the anneal time of the depletion voltage at various lower temperatures need to be established in the near future before one can rely on it in the planning of the detector operations.

2.4. Trapping

The radiation induced trapping of charge is characterized by the decrease of the trapping time τ_t with the fluence, following the law [19]:

$$\frac{1}{\tau_t} = c \cdot \Phi \qquad (5)$$

Early estimations by Transient Current Technique of the c constant for neutron damaged n-type pad detectors, giving $c_n = 5.1 \cdot 10^{-16}$ $cm^{-2}ns^{-1}$, are not in agreement with several later measurements of charge collection efficiency in heavily irradiated detectors. Among them, several recent data on highly irradiated p-type strip detectors in our target fluence range are consistent with a value 2.4 times larger [1]. We will adopt a trapping constant for proton damaged p-type detectors that is consistent with the recent experiments: $c_p = 1.3 \cdot 10^{-16}$ $cm^{-2}ns^{-1}$. The trapping effects are evaluated in a simple toy simulation, which only considers the electron drift, but includes the saturation of the drift velocity at high electric fields. Table 3 shows the trapping times τ_t for 4 target fluences.

Table 3: Trapping time τ_t for FZ p-type after 4 fluences

Fluence Φ [neq/cm^2]	$3 \cdot 10^{14}$	$5 \cdot 10^{14}$	$1 \cdot 10^{15}$	$3 \cdot 10^{15}$
Trapping time [ns]	16	9.6	4.8	1.6

The trapping mechanism in p-type material is not well understood, for example during the annealing, but the estimation in our fluence range is accurate to about 20%, based on the measurements of Refs. [11,15].

2.5. Surface Parameters

Very little is known about the behavior of strip detectors, and the dependence of surface parameters like the interstrip capacitance and the strip isolation, both pre- and post-rad, on the wafer material and processing steps (e.g. p-isolation). The interstrip capacitance exhibits a large bias voltage dependence, and becomes constant only above several hundreds volts [20,21]. There are indications that this effect is reduced after irradiation [20]. Below we will assume fairly high bias voltages beyond which this effect should not be a problem. Typical total strip capacitances are about 2 pF/cm (pre-rad) for a width over pitch ratio w/p = 0.3. This is somewhat larger than for n-type detectors pre-rad [22], and again are very similar for MCz and FZ.

3. Expected Tracker Performance as a Function of Fluence, Temperature and Bias Voltage

3.1. Electrical performance

The performance of a tracker is characterized by the signal-to-noise ratio S/N. Since all parameters are similar for both FZ and MCz p-type SSD, with the exception of annealing, and charge collection studies after irradiation have been performed up to now only on FZ [1], the following discussion of performance will be based on the numbers for FZ. The discussion will concentrate on "short strips" of 3 cm length, 80 μm pitch and width/pitch ratio of 0.3.

3.1.1. Signal

At very high fluences the signal, i.e. the charge collected within the shaping time of the amplifier τ_s, is affected by the inability to deplete the detector (Sec. 2.2) and by trapping (Sec. 2.3). It is assumed that the signal is independent of the operating temperature. Table 4 shows the collected charge for different fluence levels as a function of the maximum bias voltages The applied bias voltage needs to be sufficient to deplete the detector without over-depletion. During the operation of the detectors, one would adjust periodically the bias voltage to assure the depletion of the detector, and employ the maximum voltage only at the highest fluences. The material is MCz, and a yield of 80e/μm is assumed. After a fluence of $3 \cdot 10^{15}$ neq/cm^2 and with a bias voltage of 800V, the collected charge is 39% of the one generated in a non-irradiated 300 μm thick detector. While the inability to deplete the detector leads to an efficiency of 72%, trapping decreases the charge collection by an additional 54%. For a fluence of $3 \cdot 10^{14}$ neq/cm^2, characteristic for the outer-most tracker region, the detector can be depleted with a bias voltage of 247 V, and the charge loss due to trapping is about 10%.

Table 4: Charge collected for MCz SSD (in ke$^-$)

Fluence Φ [cm^{-2}]		SSD Thickness 300 μm			SSD Thickness 200 μm		
n	p	400 V	600V	800V	400 V	600V	800V
0	0	24.1	24.1	24.1	16.1	16.1	16.1
1.00E+13	1.61E+13	22.9	22.9	22.9	15.0	15.0	15.0
3.00E+13	4.84E+13	22.7	22.7	22.7	14.9	14.9	14.9
1.00E+14	1.61E+14	22.2	22.2	22.2	14.7	14.7	14.7
3.00E+14	4.84E+14	20.8	20.8	20.8	14.1	14.1	14.1
5.00E+14	8.06E+14	19.7	19.7	19.7	13.6	13.6	13.6
1.00E+15	1.61E+15	14.3	17.1	17.3	12.1	12.1	12.1
3.00E+15	4.84E+15	7.7	8.7	9.4	7.7	8.7	9.0
5.00E+15	8.06E+15	5.4	6.0	6.3	5.4	6.0	6.3
1.00E+16	1.61E+16	3.2	3.4	3.5	3.2	3.4	3.5

3.1.2. Noise

The noise RMS σ_{Noise} of the detector can be parameterized in the form

$$\sigma^2_{Noise} = (A + B \cdot C)^2 + (2 \cdot I \cdot \tau_s)/q \qquad (6)$$

where C is the total capacitance, and the last term is due to the leakage current I (Sec. 2.1) ($q = 1.602 \cdot 10^{-19}$ C). For A and B we will adopt ATLAS SCT like numbers A = 500 e^-, and B = 60 e^-/pF, which are also typical for a recent CMOS design in Deep submicron CMOS [23]. In the following section, we will also explore the extent to which modern bipolar technology in SiGe allows to minimize the noise by optimizing the shaping time. The largest contributor to the capacitance, the interstrip capacitance (Sec 2.4), depends on the geometry of implants, the starting material (n-type vs. p-type) and on the way the surface is processed, for example p-stop implants vs. p-spray and the p-spray dose. Not much is known on the effects of radiation on the surface properties. An ATLAS SCT shaping time of τ_s = 20 ns is assumed. The dependence of the total capacitance on the bias i.e. on the depletion depth of the detector is deemed to be small for fluences up to $3 \cdot 10^{15}$ neq/cm^2, where the depleted thickness is 200 μm or more. Because the leakage current is temperature dependent, the noise is temperature dependent (eq. (6)). Fig. 1 shows the signal-to-noise ratio S/N as a function of fluence n_{eq} for short strips (6 pF) for two detector thicknesses (300 μm and 200 μm), and three maximum bias voltages (400 V, 600V, 800V), for an operating temperature of –20 °C. As mentioned above, the detectors need to be biased at their depletion voltage or at the maximum voltages, whichever is smaller. The choice of the maximum bias voltage plays a role only in the fluence range of $1 \cdot 10^{15}$ neq/cm^2: much below that fluence, the depletion voltage of 300 μm detectors is below 400V, and much above that fluence, the trapping effects limit the depth of the effective active region. There seems to be no advantage to use 200 μm thick detectors.

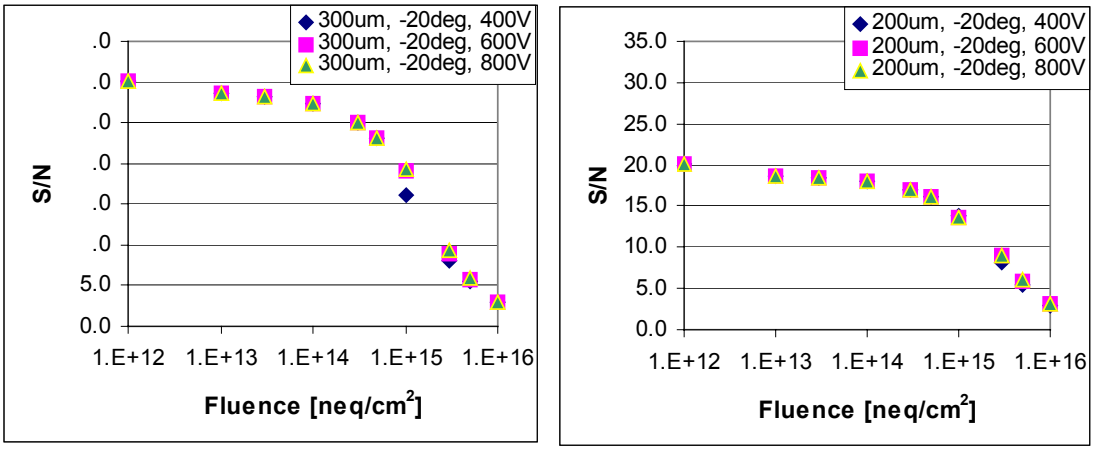

Fig. 1 Signal-to-Noise ratio S/N for p-type MCz short strip SSD as a function of fluence for two detector thicknesses: 300μm at the left, and 200 μm at the right. The operating voltage is varied from 400 to 600 to 800V. The leakage current constant is set to $\alpha_p = 2.5 \cdot 10^{-17}$ A/cm. The operating temperature is set at –20°C. The strips are 3 cm long with a pitch of 80 μm.

3.1.3. *Shaping Time*

The shaping time can be used to balance the different noise terms in equation (6). The first and third terms are proportional to the shaping time, while the second term is proportional to the inverse of the shaping time. For bipolar transistors, the collector current and the current gain play a role too. The noise is calculated as a function of fluence using recent measurements on SiGe transistors [24].

Fig. 2 shows the dependence of the noise RMS on the shaping time for different fluences and detectors capacitances C. Here the short strip option (C = 6 pF) and a long strip version (C=15 pF) are calculated The operating temperature is –10 ^{o}C for all series of points but one, where -20 ^{o}C is used.

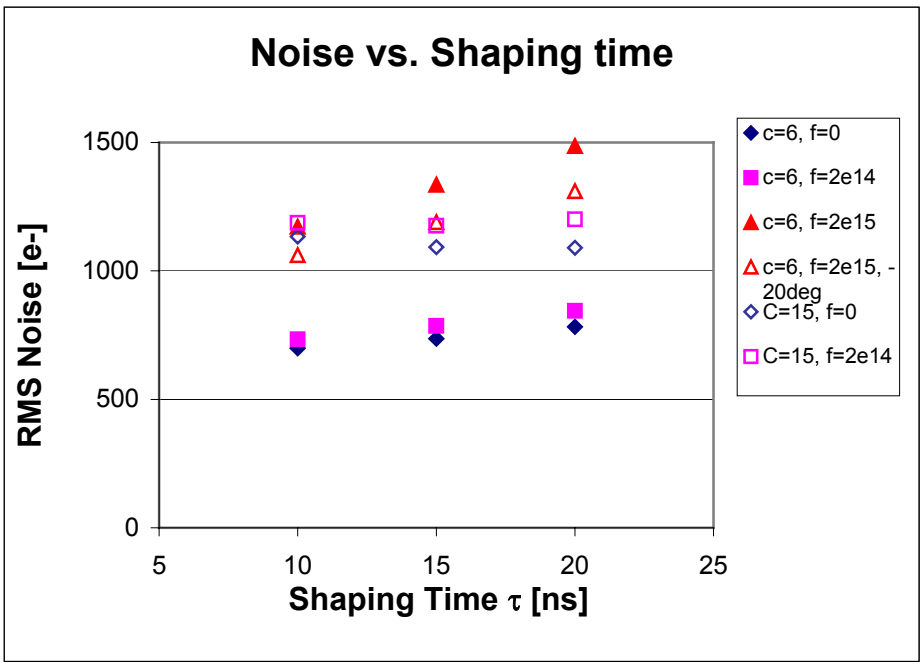

Fig. 2 Noise RMS for p-type MCz SSD as a function of shaping time for short strips prerad, and after fluences of $2.2 \cdot 10^{14}$ and $2.2 \cdot 10^{15}$ neq/cm^2 and long strips pre-rad and after a fluence of $2.2 \cdot 10^{14}$ neq/cm^2 . The maximum bias voltage is 600 V. The leakage current constant is set to $\alpha_p = 2.5 \cdot 10^{-17}$ A/cm.

The temperature dependence of the signal-to-noise ratio S/N is shown in Fig. 3 for end-of-life fluences for both short (C = 6 pF) and long strips (C = 15 pF) for three different shaping times. The noise exhibits only a weak dependence on this parameter, meaning that the operating temperature can be selected first and the S/N performance then optimized by choosing the shaping time. A short shaping time is useful to reduce the noise from large leakage currents.

In the target fluence range < $3 \cdot 10^{15}$neq/cm^2, a few conclusions can be drawn from Figs. 1, 2 and 3:

- The S/N are almost identical for a bias voltage of 600 V and 800 V, but markedly smaller for a bias of 400 V. The reason is that for heavily damaged SSD, where the depletion voltage is much larger than these bias voltages, the depletion depth is only a fraction of the physical thickness. At these fluences, trapping is important, so that the charge could not be collected even if more of the detector could be depleted.
- There is no advantage to using 200 μm SSD instead of 300 μm thick detectors. Since the charge is collected on the junction, the active thickness can be regulated with the bias voltage. Thicker detectors will improve the heat conduction.
- At the end-of life fluences, decreasing the operating temperature of short strips by 10 ^{o}C improves the S/N by about 10%. A similar effect is achieved by reducing the shaping time by 5 ns.

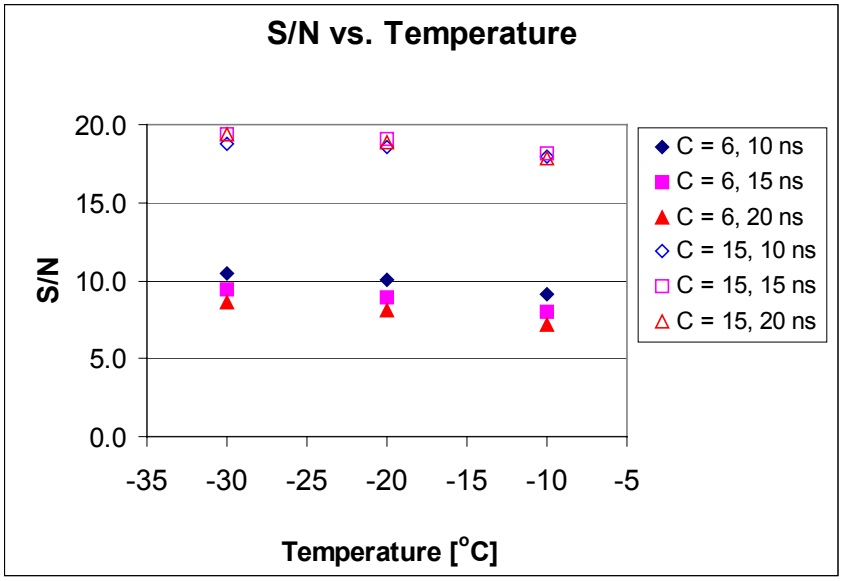

Fig. 3 Signal-to-Noise ratio S/N for p-type MCz SSD of 300 μm thickness as a function of operating temperature for three shaping times for short strips after a fluence of $2.2 \cdot 10^{15}$ neq/cm^2 and long strips after a fluence of $2.2 \cdot 10^{14}$ neq/cm^2 The maximum bias voltage is 600 V. The leakage current constant is set to $\alpha_p = 2.5 \cdot 10^{-17}$ A/cm.

3.2. Thermal Performance

The generated heat depends both on the leakage current and the bias voltage. The fact that the electrons are collected on the junction makes over-depletion unnecessary unlike in the case of inverted p-on-n SSD and even allows under-depleted operation. Thus the generated heat is calculated by assuming the detectors are operated at the depletion voltage until the depletion voltage reaches one of three target maximum bias voltages (400, 600, 800V), and that the thickness of current generating volume w in eq. (1) is determined by eqs. (4). Table 5 shows the generated heat as a function of operating temperature and fluence for three maximum bias voltages for MCz p-type detectors. As mentioned before, the leakage current constant used is $\alpha_P = 2.5 \cdot 10^{-17}$ A/cm at 20 ^{o}C.

Since the leakage current is collected from the depleted region only, and at high fluences, the depleted depth w is smaller than the physical detector thickness t, there is no advantage to using 200 μm instead of 300 μm thick SSD.

Table 5 Heat from Leakage Current in 300 μm SSD

			Generated Heat Flux [W/cm^2]			
Φ neq	Vbias [V]	w [μm]	T = 20°C	T=-10°C	T=-20°C	T=-30°C
3E+14	290	300	1.05E-01	6.75E-03	2.35E-03	7.54E-04
5E+14	376	300	2.27E-01	1.46E-02	5.09E-03	1.63E-03
1E+15	400	247	3.98E-01	2.55E-02	8.90E-03	2.85E-03
1E+15	591	300	7.15E-01	4.59E-02	1.60E-02	5.13E-03
3E+15	400	157	7.62E-01	4.89E-02	1.70E-02	5.46E-03
3E+15	600	193	1.40E+00	8.99E-02	3.13E-02	1.00E-02
3E+15	800	223	2.16E+00	1.38E-01	4.82E-02	1.55E-02

4. Discussion

Based on the evaluated data, one can state preferences to some of the detector choices:

P-type wafer : MCz silicon is preferred over FZ because of the delayed anti-annealing. Determination with more precision of the annealing behavior will be very important.

SSD Thickness : 300 μm preferred over 200 μm because of larger charge collected, better heat conduction.

Bias Voltage: 600 V is preferred over 400 V because of better charge collection, 600 V is preferred over 800 V because of reduced heat generation, and very little difference in charge collection.

Operating Temperature: - 10^{o}C preferred because it simplifies operations, (about 15% worse S/N than at -20^{o}C, can be offset by shorter shaping times).

Shaping time shaping times of 10 ns -15 ns can be used on bipolar SiGe ASICs for both short strips and long strips for optimal noise performance, allowing higher operating temperatures.

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