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INTERSTRIP CAPACITANCE OF A PROTOTYPE STRIPIXEL DETECTOR

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Abstract

We measured the inter-strip capacitance on a prototype DC-coupled "stripixel" detector (SPD) employing circular spirals with two methods, each of them employing a RC-chip to bias and read out the detectors. Both yielded the same value of C_{int} = 1.1 pF for a strip length of 1.4 mm, indicating the total inter-strip capacitance to be much larger than on ordinary silicon strip detectors (SSD).

1. INTRODUCTION

The "stripixel" detector (SPD) [1] is a novel silicon strip detector that allows readout of two coordinates from the same side of the detector, thus yielding 2-D information with single-sided processing. The signal collected on the implant side is split between two implant strips, which are ganged with neighboring strips to form two readout directions. To allow for uniform charge sharing between the two readout directions, the implants need to be very close so that the charge cloud is intercepted by both. Thus in the present SPD, a strip has very close coupling with all strips of the alternate readout direction in addition to the neighboring strips. Additionally, the SPD investigated is DC coupled, which complicates the measurement; this was somewhat facilitated by the use of an RC-chip [2] which permits biasing and AC-readout of DC coupled strips. An in depth investigation into the components of the experimental setup was conducted. First, the AC-capacitance was measured, which required the evaluation of the capacitance of the RC chip, and then the DC capacitance of the SPD was measured directly.

2. PROTOTYPE STRIPIXEL DETECTOR

Fig. 1 shows the prototype SPD. It is fabricated on n-type wafers of 200 μm thickness. There are 16x16 channels of 80 μm pitch with interweaved circular spirals of p-type implants to create a two-dimensional position detector; the readout strips and bonding pads are located on two adjacent sides. This is a DC coupled detector with no integrated bias resistors or capacitors, which makes it difficult to bias the entire detector at the same time without a probe card. This will be remedied by adding an RC chip, to allow for biasing and readout of the entire SPD. More information on the SPD is given in [1]. While the strip length is 0.14 cm, the implant length of one strip inside the spirals is 0.358 cm. The width and spacing of the implants are 5 um, much closer than on an ordinary SSD.

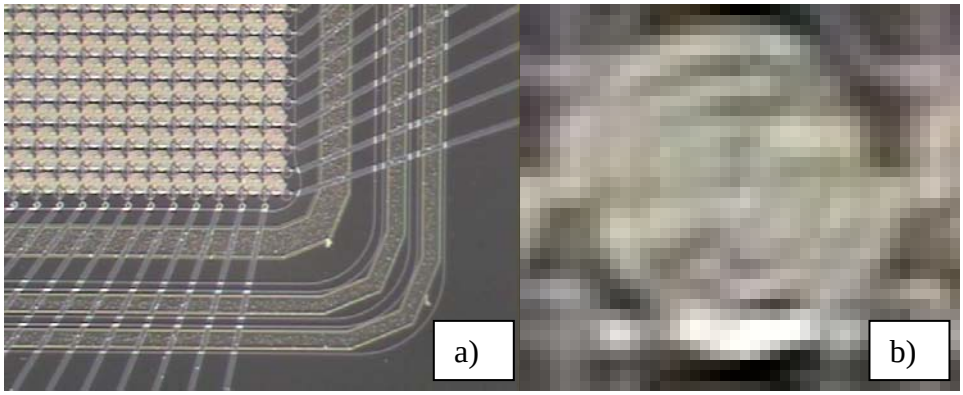

Fig. 1: Strip-pixel detector used a: one corner of the strip-pixel detector showing the X and Y strip readout lines, b: view of one pixel showing the intertwined circular spirals connected to the two readout directions.

3. RC-CHIP

The RC chip [2] was used in the readout of the CLEO II vertex detector and was provided by Prof. H. Kagan from Ohio State University. It consists of 128 channels, each composing of a resistor and a capacitor built on a quartz substrate. The channels are staggered to keep real estate to a minimum. The purpose of the RC chip is to properly bias the detector and isolate the bias from the input of the sensitive front-end electronics. Figure 2 is an electrical schematic of the RC chip.

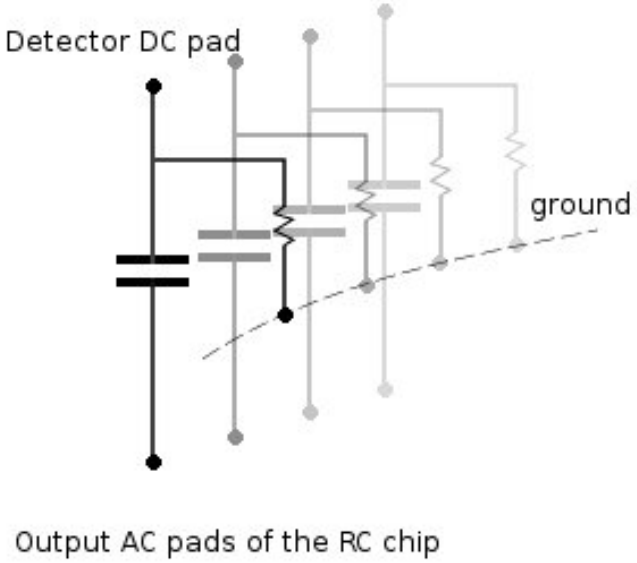

Figure 2: Electrical schematic of RC chip, the resistors bias the detector and the capacitor isolates the front-end electronics.

4. SPD AC INTERSTRIP CAPACITANCE

a. SPD+RC CAPACITANCE: SETUP AND PROCEDURE

To measure the inter-strip capacitance of the ‘stripixel’ detector we isolated a single ‘Y’ test strip in respect to its neighbors by bonding out three ‘Y’ neighbors to each side to each other and three additional ‘Y’ strips outside of the neighbors to each other to shield. All the ‘X’ strips were bonded out to each other and connected to neighbor ‘Y’ strips. It was shown in prior experiments at SCIPP that 95% of the inter-strip capacitance is attributed to the first three neighbors on each side of the test strip [3].

A five-point setup was required to measure the inter-strip capacitance of the detector. Three probes from the HP4145B (SMU1-3) were used to bias the detector and ground the guard ring as done previously in the current-voltage measurements. Two additional probes, HIGH and LOW from the HP4284A test fixture were connected to the AC pads of the test strip and neighbors respectively. Following open and short corrections, the series capacitance was measured and collected for a range of frequencies with the AC signal at 50 mV.

b. SPD+RC RESULTS

Figure 3 shows a plot of the inter-strip capacitance of the ‘stripixel’ detector as a function of bias voltage for various frequencies. At higher frequencies, the measured values converge to 3.0 pF as the voltage is increased. This is sum of the inter-strip capacitances of the SPD and the RC chip. To determine the inter-strip capacitance of the SPD alone, the effect of the RC chip has to be subtracted.

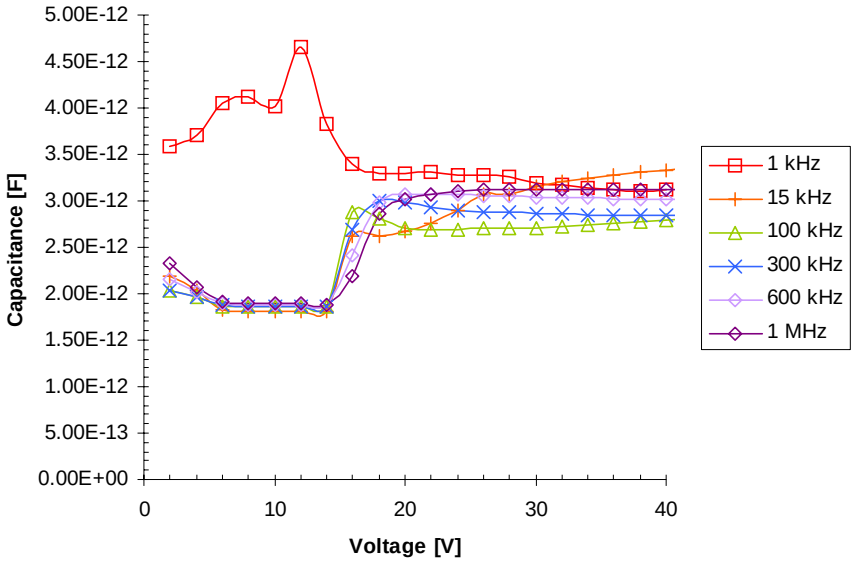

Figure 3: C-INT plot of the AC set-up of the 2D silicon detectors (SPD)

c. RC CHIP CAPACITANCE: SETUP AND PROCEDURE

An RC chip was bonded out to closely mirror the bonding on the SPD/RC chip setup used for the inter-strip capacitance measurement. Three channels on each side of the test strip were bonded together along with three additional channels to each side for shield. This makes for a total of twelve channels used. Additionally, a collection of twenty-one channels were bonded together for the purposes of closely matching the original setup used for inter-strip capacitance of the SPD. The inter-strip capacitance from the test strip to the rest of the bonded strips was measured using three probes. A probe was connected to the test channel (HIGH of HP4284A LCR meter). Another probe was connected to the participating channels (LOW of LCR meter). The last probe was connected to the bias line that is also connected to shield.

d. RC CHIP CAPACITANCE RESULTS

Measurements were done twice to ensure accuracy, and the results are plotted in Figure 4. The inter-strip capacitance of the RC chip was found to be 1.91 pF at high frequency where the capacitance saturates. Subtracting this value from the combined AC inter-strip capacitance of the SPD and the RC chip (Section 4b) yields the inter-strip capacitance of the SPD.

$$C_{int}(AC) = 1.09 \text{ pF}$$

The coupling capacitance value for the RC chip was found to be C_{coup} =133 pF . This is in good agreement with the published value of >125 pF [2].

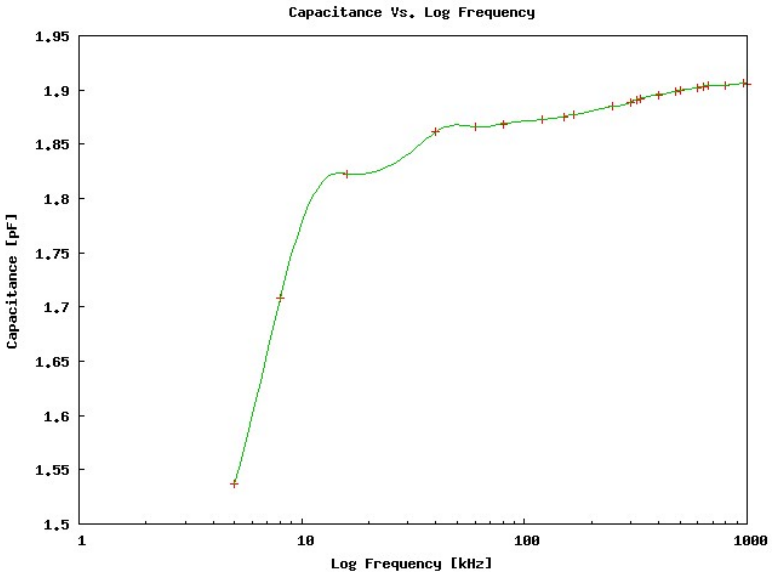

Figure 4: RC chip inter-strip capacitance vs. frequency.

5. SPD DC INTERSTRIP CAPACITANCE

a. SETUP

For this portion of the investigation, the AC setup of the SPD and RC chip of Sec. 4 was modified as follows. Three probes from the HP4145B (SMU1-3) were used to bias the detector and ground the guard ring as mentioned earlier. HIGH and LOW from the HP4284A test fixture were connected to the DC pad of the test strip located on the SPD and the AC pads of all neighboring strips located on the RC chip, respectively. Originally, the interstrip capacitance of the RC chip and the detector test strip were in parallel. In this set-up, the test strip is disconnected from the RC chip, so that the capacitances of the RC chip appear only in series and parallel with all the strips except the test strip. All these other strips are short circuited to each other and to the LOW terminal via the very large strip coupling capacitance C_{coup} = 133 pF, as mentioned in Sec 4.d. Thus the true SPD interstrip capacitance is measured.

b. SPD DC CAPACITANCE RESULTS

Figure 5 shows the interstrip capacitance for several frequencies as a function of bias voltage. For large bias voltages and frequencies, the interstrip capacitance is

$$C_{int}\,(DC) = 1.15 \pm 0.10\ pF.$$

This is in agreement with the AC measurement, which yielded 1.09 pF.

Normalizing the C_{int} of the SPD by the effective strip length of 0.14 cm gives 8.2 pF/cm. Part of this rather large value is due to the large length of the strips within the spirals. Normalizing the inter-strip capacitance by dividing the measured capacitance by the "unraveled" strip length 0.358 cm, gives a capacitance of 3.2 pF/cm, which is much larger than the inter-strip capacitance of about 1.5 pF/cm observed on normal SSD, and can be understood as a consequence of the proximity of the implants to allow for efficient charge sharing (Fig. 1).

6. CONCLUSION

The inter-strip capacitance of prototype silicon stripixel ("2-D") detectors were measured with two different methods and yielded 1.15 ± 0.1 pF for 0.14 cm long strips. This translates into 8.2 pF/cm. Part of this rather large value for the inter-strip capacitance is due to the effective implant length, which is about 3 times the strip readout length. The other part is due to the proximity of the implants of the two readout directions, required by the need to collect the shared charge uniformly.
The results are from a very small detector built on n-type wafers. They should be confirmed on larger detectors, where the measurement is less influenced by parasitic capacitances. In addition, the interstrip capacitance on p-type detectors should be measured.

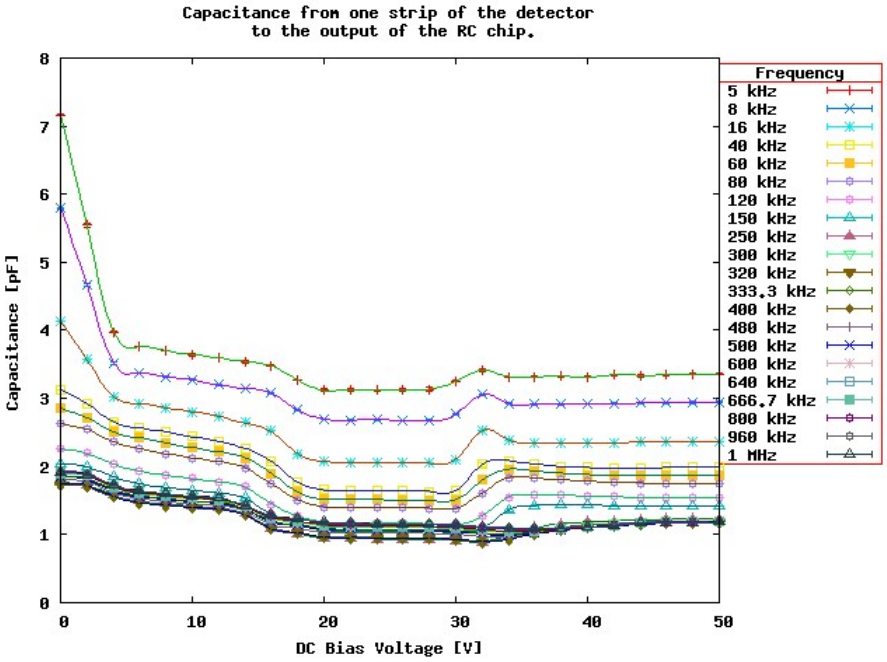

Figure 5: Effective capacitance of the SPD.

7. ACKNOWLEDGMENTS

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8. REFERENCES

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