Total Dose Dependence of Oxide Charge, Interstrip Capacitance and Breakdown Behavior of sLHC Prototype Silicon Strip Detectors and Test Structures of the SMART Collaboration

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Abstract

Within the R&D Program for the luminosity upgrade proposed for the Large Hadron Collider (LHC), silicon strip detectors (SSD) and test structures were manufactured on several high-resistivity substrates: p-type Magnetic Czochralski (MCz) and Float Zone (FZ), and n-type FZ. To test total dose (TID) effects they were irradiated with ^{60}Co gammas and the impact of surface radiation damage on the detector properties was studied. Selected results from the pre-rad and post-rad characterization of detectors and test structures are presented, in particular interstrip capacitance and resistance, break-down voltage, flatband voltage and oxide charge. Surface damage effects show saturation after 150 krad and breakdown performance improves considerably after 210 krad. Annealing was performed both at room temperature and at 60 ^{o}C, and large effects on the surface parameters observed.

Keywords: Silicon microstrip detectors; Surface radiation damage; MOS capacitors

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1. Motivation

The future luminosity upgrade proposed for the Large Hadron Collider, the Super-LHC (sLHC), requires a critical evaluation of the radiation hardness of the silicon strip detectors (SSD) proposed as main tracking detectors in the Inner Detector (ID) of the upgraded LHC detectors [1]. The CERN R&D collaboration RD50 was formed to investigate radiation damage in semiconductor detectors and develop radiation-tolerant tracking detectors [2]. The INFN funded SMART project that involves several Italian institutes belonging to RD50, has fabricated silicon strip detectors and test structures on various high-resistivity substrates [3]. The aim of this activity is to thoroughly characterize the different design/technology options so as to understand the details of fabrication steps which will permit the fabrication of radiation-tolerant SSDs.

As far as bulk radiation damage is concerned, which is the main problem to face since it reduces the collected charge, promising results have already been reported [4]. However, surface damage effects should also be considered, since they might influence the noise performance. This is especially relevant for detectors built on p-type substrates, for which isolation structures (p-stop or p-spray) are needed in between the n^+ strips to interrupt the inversion electron layer induced by the positive fixed oxide charge. In fact, simulation studies have clearly evidenced the strong impact of surface effects (oxide charge, surface states) on the interstrip capacitance and the breakdown voltage, as well as on the isolation properties of the p-stop/p-spray regions [5]. This paper describes experimental results from the electrical characterization of strip detectors and test structures irradiated with ^{60}Co to test total dose effects. The TID levels for the sLHC, mainly due to charged particles, are expected to exceed 100 Mrad close to the collision region, while effects at the Si-SiO_2 interface have been shown to saturate typically at the 100 krad level [6].

2. Devices

A set of test structures and SSDs were fabricated on several different wafer types at ITC-irst in Trento, Italy. They include, as shown in Table I for this study, short SSD of varying strip width and pitch, circular MOS capacitors with aluminum top electrode, and capacitance test structures (TS), which are mini strip detectors. Results are presented for a subset of the available SMART wafers, as listed in Table II. The n-

type FZ and the p-type MCz were 300 μm thick, while the p-type FZ had a thickness of 200 μm. The p-type wafers were processed with two different p-spray doses to isolate the strips: 3×10^{12} cm^{-3} ("low p-spray dose") and 5×10^{12} cm^{-3} ("high p-spray dose"). Table III lists the details of the SSD investigated.

3. Sample Preparation

The test structures are comprised of 9 AC coupled strips, of which the inner-most three allow the measurement of the interstrip capacitance from the central strip to its pair of next neighbors, and the outer three strips on each side are connected together to allow bonded connections to a shield, for which we used the bias ring. We compared the interstrip capacitance of a test structure with the one of a 4.45 cm long mini-SSD, where the interstrip capacitance was measured to 3 pairs of next neighbors, with the next 3 strips on each side grounded to shield. Results of these measurements are shown in Fig.1. The expected ratio of 1.2 between the geometrical values of capacitance/length to the next pair and to the next three pairs is observed [7]. It should be noted that pre-rad one observes a large effect on the interstrip capacitance whether the shield strips are bonded to the bias ring or not. This difference disappears post-rad.

4. Data

a. Irradiations

Irradiations were performed in the UC Santa Cruz ^{60}Co source in steps of approximately 70 krad, corresponding to one day irradiation at a dose rate of 3.15 krad/hr. The parts were irradiated with their electrical terminals floating.

b. Annealing

With the devices being irradiated with their terminals floating, a certain amount of room temperature annealing has to be expected. The devices were stored at room temperature and the time between irradiations and measurement could vary by a few days. The annealing is shown in the graphs as double-valued parameters for the same dose. A more thorough annealing was performed at the end of the irradiation, lasting for one week at room temperature and two weeks each at $60^{o}C$.

c. Measurements

Frequency dependent C-V characterizations using an HP 8241 LCR meter were performed before the irradiation, and within a few days after each step. At the end, the capacitance-voltage (C-V) data at 10 kHz are reported for the MOS capacitors, while the interstrip capacitances (Cint-V) are reported at the highest frequency, e.g. 800 kHz or 1 MHz.

The bias dependence of currents and capacitances could be determined before irradiation only in a restricted interval of applied bias voltages because of breakdown which occurred in some cases before depletion. In fact, before irradiation, detectors with high-dose p-spray isolation had a breakdown voltage in the 50-150 V range, depending on the width/pitch value. A considerable increase in breakdown voltage after irradiation can be observed (see below).

The interstrip resistance was determined on the mini-SSD with a 2 probe measurement using an HP 4145 Semiconductor Analyzer with the following set-up: one source channel biased the detector to 50 V, the bias ring was set to ground, the current I_1 on one strip was determined by measuring the potential across the biasing resistor of 600 kΩ with a measuring channel, and the voltage on its two next neighbors V_2 was swept with a second source channel from -5 to +5 V. The interstrip resistance is then Rint = $2*\Delta V_2/\Delta I_1$.

During data taking on the MOS capacitors, several observations were made which limit the accuracy of the extraction of flatband voltage and the oxide charge. First the C-V curves display hysteresis (Fig. 2). The capacitance values during voltage ramp-up differ from the ones during ramp-down, for the same value of the bias voltage. This is due to an extremely slow charge-up and discharge of the capacitor, and presumably could be avoided with much longer waiting time. Second, the C-V curves show “notches” in the C-V curve and/or bi-stable capacitance values at certain voltages. A similar instability has been also reported for high voltage stressed MOS capacitors [8], [9].

d. Results on MOS capacitors

The C-V measurements on MOS capacitors are being analyzed to extract the flatband voltage V_{FB} and the oxide charge density Qox (the oxide charge per unit area) and their evolution through the irradiation [10]. Since the flatband voltage is directly proportional to the oxide charge density, we only show the latter. The doping density can be extracted as part of the process and is of the order 10^{16} to 10^{17} cm^{-3} for p-type and 10^{11} to 10^{12} cm^{-3} for n-type, as predicted from process simulations [5]. Fig. 3 shows the effect of the dose on the density of the oxide charge Qox/q, where q is the electron charge. Saturation is observed after about

150 krad for all measured devices regardless of the bulk material. The charged trapped in the oxide reaches similar densities for all p-type devices ($\sim 1.5\times10^{12}$ cm^{-2}) while an higher value is observed for FZ n-type ($\sim 2\times10^{12}$ cm^{-2}). This difference is expected since FZ n-type wafer was oriented <111> while the p-type wafers were <100>. Annealing reduces the effect both during the irradiation process and after the elevated anneal. A saturation of the annealing is visible after the first high temperature annealing step. Such a strong annealing effect has been observed before on MOS structures processed at ITC-irst and irradiated with X-rays [11].

e. Results on SSD and SSD test structures

The current – voltage (I-V) curves at different doses shown in Fig. 4 reveal an improved performance in breakdown voltage after irradiation. In fact, before irradiation, detectors with high-dose p-spray isolation had a breakdown voltage in the 50-150 V range, depending on the width/pitch value. After a dose of 210 krad a much larger reverse bias, of the order 500 V, can be applied without the risk of breakdown for all the devices regardless of the strip geometry. Large annealing effects lower the breakdown voltage again between intermediate irradiation steps and at the post-radiation elevated annealing step. Table IV shows the breakdown voltage at several steps in the irradiation campaign. Wafers where implant isolation has been done with high p-spray implantation dose seem to exhibit large annealing-out of the improved breakdown performance.

The results from capacitance measurements on test structures show a saturation trend similar to the MOS capacitors (Figs. 5 and 6). The irradiation lowers Cint drastically for p-type SSD, and the Cint geometrical value is approached as the voltage is increased. This result is in good agreement with simulation predictions, and is due to the depletion region widening inside the p-spray at the surface [5]. Saturation is reached at a dose between 70 and 150 krad. The wafer with low-dose p-spray isolation reaches the saturation already with 70 krad, with very little residual voltage dependence of the interstrip capacitance. The n-type test structures show increased interstrip capacitance with increased dose, while the p-type test structures exhibit reduced interstrip capacitance. There is no dependence of wafer type, i.e. MCz and FZ behave the same, separately for high and low p-spray dose, respectively. The amount of annealing is very limited.

The same trends are seen with the mini-SSD. Figure 7 compares the interstrip capacitance vs. bias voltage for two p-type wafer types (MCz and FZ) and two p-spray doses. There is no difference between MCz and FZ, but large differences due to the surface treatment, i.e. between low- and high-dose p-spray.

The interstrip resistance was measured pre-rad and after radiation and annealing. A value in excess of 10^{10} Ω was measured pre-rad and post-rad for the 1.15 cm long test structures, for all wafers and surface treatments.

5. Conclusions

The investigation of radiation damage of surface effects showed no dependence on the p-type wafer type (FZ vs. MCz), but large dependence on the surface treatment (high vs., low p-spray dose).

Saturation was observed for the interstrip capacitance at about 100 krad, with very little annealing.

The flatband voltage and the oxide charge density showed also saturation at about 150 krad, but in addition a very large annealing by a factor 3.

The breakdown voltage was increased by the gamma irradiation, but also showed very strong annealing for the SSD with high p-spray dose. The strips showed good isolation before and after irradiation and annealing.

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7. References

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Table I: Structures Investigated

Type	Dimension	Measurements	Frequency
MOS Capacitor	Circular Area =3.14mm^2	C-V	10 kHz
Capacitance TS	Length = 1.15 cm Pitch = 50, 100 μm Implant = 15, 25 μm Poly width = 10 μm Metal = 23, 33 μm	Cint-V C-V i-V	~ 1 MHz 10 kHz n.a.
SSD	Length = 4.46 cm Pitch = 50, 100 μm Implant = various	Cint-V C-V i-V	~ 1 MHz 10 kHz n.a.

Table II: Wafers Investigated

Wafer Type	Wafer #	Thickness [μm]	P-spray Dose [cm^{-2}]	SSD / TS / MOS
n FZ	W1254	300	n.a.	TS, MOS
p FZ	W084	200	5×10^{12}	TS, MOS
p FZ	W014	200	3×10^{12}	SSD
p FZ	W037	200	5×10^{12}	SSD
p MCz	W044	300	3×10^{12} , no passivation	TS, MOS
p MCz	W253	300	5×10^{12} , no passivation	TS, MOS
p MCz	W066	300	3×10^{12} , no passivation	SSD
p MCz	W182	300	5×10^{12} , no passivation	SSD

Table III: P-Type SSD Investigated

SSD	Substrate	P-spray Dose [cm^{-2}]	Pitch (μm)	# strips	Implant Width (μm)	Poly Width (μm)	Metal Width (μm)
14-5	FZ	3×10^{12}	50	64	15	10	27
14-8	FZ	3×10^{12}	100	32	35	30	43
37-5	FZ	5×10^{12}	50	64	15	10	27
37-8	FZ	5×10^{12}	100	32	35	30	43
66-8	MCz	3×10^{12}	100	32	35	30	43
182-5	MCz	5×10^{12}	50	64	15	10	27
182-8	MCz	5×10^{12}	100	32	35	30	43

Table IV Breakdown Voltage

Device	**Breakdown Voltage [V]**				
	pre-rad	**75 kRad**	**300 kRad**	**~650 kRad**	**~650 kRad +7d @60 °C**
66-8 p MCz low	250	550	900		
182-8 p MCz high	70	>200	350	>1000	500
14-8 p FZ low	240	600	600	700	600
37-8 p FZ high	70	200	300		

Figure Captions

Fig. 1 Voltage dependence of the interstrip capacitance (Cint) for p-type MCz pre-rad. For the mini-SSD W037, the capacitance to the 3 pairs of next neighbors are measured, with the following neighbors bonded to shield, while for the test structure W084 R 3-4, the capacitance to only the pair of next neighbors is measured. The expected ratio of 1.2 is measured. For the test structure W084 R 3-4, the effect of bonding out the shield strips to the bias ring is shown. The capacitance is scaled to a length of 1.15 cm.

Fig. 2 Capacitance – voltage (C-V) characteristics of a MOS capacitor fabricated on a p-type MCz wafer with high-dose p-spray, both pre-rad and after a total dose of 210 krad of ^{60}Co gammas. The flatband voltage increases from about 3 V pre-rad to about 65 V after a total dose of 210 krad. The hysteresis between data taken with increasing (filled symbols) and decreasing (un-filled symbols) voltage is seen.

Fig. 3 Effect of the total dose on the density of the oxide charge Qox/q for four different wafers: a) n-type FZ b) p-type FZ high-dose, c) p-type MCz high-dose, d) p-type MCz low-dose. Data at the same dose indicate annealing. For the largest dose point, the highest value is right after irradiation, the second highest right after one week of room temperature annealing and the third and fourth highest each after an additional one week annealing at 60 ^{o}C, respectively.

Fig. 4 Typical leakage current – voltage (I-V) curves for several irradiation steps. The breakdown voltage is increased considerably with increased dose.

Fig. 5 Interstrip capacitance of the 50 µm pitch test structures as a function of the total dose for p-type MCz high-dose wafers. All other p-type test structures behave the same way, including the absence of strong annealing effects.

Fig. 6 Interstrip capacitance of the 100 µm pitch test structures as a function of the total dose for the n-type FZ wafer. Saturation is seen at about 100 krad, and annealing is limited.

Fig. 7 Comparison of the interstrip capacitance of the 100 µm pitch mini-SSDs, pre-rad and after saturation a) FZ (wafers 14 and 37), b) MCz (wafers 66 and 182). The differences between different wafer types are small, but are large depending on the p-spray dose. Saturation below 150 krad and only limited annealing are observed.