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Track Time Tagging in Multi-layer Silicon Trackers

Hartmut F.-W. Sadrozinski
SCIPP, Univ. California Santa Cruz, CA 95064

Abstract
The accuracy with which the time of a track in a collider can be determined is being investigated. A comprehensive study of the hit and track timing in Babar [1] is summarized, in which a track time resolution much better than given by the clock period was achieved. It has been used to eliminate tracks and hits from background processes. The ability of the ATLAS SCT to tag the single bunch crossing is then reviewed [2]. Careful clock distribution will confine all hits on a track to within the clock window of 25 ns. An extension of the ATLAS scheme involving faster charge collection, shorter shaping time and higher clock frequency is proposed which will allow the hits on a track to be time tagged with a resolution of better than 3 ns, with the track time tagged to 1.5 ns.

A. INTRODUCTION

In many collider applications with backgrounds from uncorrelated sources, it is desirable to tag hits or entire tracks with the event time. In a large tracking system using silicon detectors, where the collection time and the shaping time are much larger than a nanosecond, this requires careful data analysis. For example, in Babar at PEP2, where the collisions occur quasi-continuous, the time-tagging of hits has a resolution of about 20 ns and an entire track can be time-tagged to 6 -7 ns, resulting in cleaning up the events [1]. In the SCT ATLAS at the LHC, the shaping time is adjusted such that all hits fall within one time bucket of the 40 MHz clock [2]. Thus the time resolution of the ATLAS SCT is about 8 ns (i.e. 25ns /√12). The question arises if the hit time resolution can be improved. In the proposed Short-Shaping Time Silicon Tracker (SSTSiT) [3], the experience with ATLAS is extrapolated by a factor 2.5 in clock frequency.
In all cases, the readout is a "binary" system where a fixed threshold determines if hit is recorded. If the charge on a strip Q exceeds this threshold Q_{thr} the address of the strip is recorded, otherwise it is not used. With proper shaping, the pulse length can become a measure of the strip charge, and thus reading out the pulse length yields the pulse charge. The intrinsic time resolution σ_I of a time measurement can be estimated from the signal-to-noise ratio S/N and the rise time of the pulse τ_R:

$$\sigma_I = dt/dQ * \sigma_Q = (dQ/dt)^{-1} * \sigma_Q \approx (Q/\tau_R)^{-1} * \sigma_Q = \tau_R * (S/N)^{-1} \qquad (1)$$

B. BABAR

Time- tagging for the Babar SVT data has been studied by Gerry Lynch [1]. The system parameters and the performance are given in Table 1. The shaping time τ_S is much longer than the collection time of the charge due to noise consideration: the SVT has fairly long ladders, presenting large capacitances to the front-end, and the shaping time is adjusted to have acceptable noise performance. The pulse height Q is determined with Time-over-

Threshold ToT with a frequency of 16 Mhz (pulse period 67 ns). This is absolutely necessary for good timing resolution, because the time walk ΔT_w depends on the rise time τ_R:

$$\Delta T_w = Q_{thr}/Q^* \tau_R , \qquad (2)$$

where Q_{thr} is the discriminator threshold, and the rise time τ_R is close to the shaping time of 100ns (400 ns in the outer layers). After the hits in all clusters are corrected for the time walk, the time resolution σ_H of the hits is 20 ns, which is the expected resolution for the frequency selected:

$$\sigma_H = 67ns/\sqrt{12} = 20 \text{ ns}. \qquad (3)$$

The surprising results is the time resolution on the entire track: combining the many time measurements in clusters and layers yields a track resolution of σ_H = 6-7 ns. The walk correction introduces a certain amount of randomization which allows a sqrt(N) reduction in error, but it seems unlikely to be the dominant cause of such an improvement in the track resolution. Rather, it is conjectured that the fact that the clock is distributed across the SVT with two distinct phases differing by ½ clock cycle is the main cause of such an improvement. This trick to essentially doubling the clock frequency and thus improving the track time resolution by a factor 2 could be employed with a reasonably large number of layers available.

C. ATLAS SCT

The ATLAS Semi-Conductor Tracker (SCT) has a truly binary read-out system, without charge determination. The shaping is adjusted such that all hits in one event fall into one bucket of the 40 MHz clock, corresponding to the machine collision frequency, allowing "single-bucket" determination of the event (Table 1). This is necessary to suppress the contribution from adjacent time buckets of the large background from minimum-bias events in every collision. Although the SCT uses relatively short strips (12cm), the shaping time needs to be as long as possible to suppress noise hits (Table 1). The achieved time resolution of $25ns/\sqrt{12} = 8$ ns is mainly due to the range of the time walk between largest and smallest accepted pulses of ΔT_w = 16 ns.
One could then ask if the time resolution could be improved by decreasing the shaping time. This is shown in Fig.1, where the pulse shapes for the charge collection with 100V bias are shown for two shaping times (10 ns and 20 ns) using the simple RC-CR formula $f(t) = t*\exp(-t/\tau_S)$. Two observations can be made: at 20 ns shaping time, the entire pulse is captured within the 16 ns time walk window mentioned above. And the improvement in timing characteristics of the pulse are limited by the collection time of the pulse.

D. SHORT-SHAPING TIME SILICON TRACKER SSTSiT

The ATLAS experience can be extended to shorter shaping times and higher clock frequency in Short-Shaping-Time-Si-Tracker SSTSiT. A truly binary system is assumed, without the possibility of walk correction. This means that the entire rise of the pulse has to be captured in the 10 ns clock period. To achieve this, the bias voltage of the detectors has to be increased to achieve a factor two faster charge collection. Assuming a bias

voltage of 300V, the holes are collected within 7 s, and the electrons in 2.5 ns [4]. The expected pulse shapes for shaping times of 10 ns and 5 ns are shown in Fig. 2, showing again no real advantage to shape faster than 10 ns with the given collection time. The anticipated performance is shown in Table 1. Note that this a factor 2 extension of the ATLAS system, and it will a straightforward time resolution per hit of 3 ns.
The ultimate limit on timing per layer, eq. (1), would be $\sigma_I < 1$ ns, with a rise time $\tau_R \approx$ 10 ns and a $S/N_Q \approx 15$.
Based on the Babar experience, one might expect that the track time resolution could be improved by a factor 2 by judicious phasing of the clock in different layers.
Decreasing the shaping time by a factor 2 from the ATLAS design will increase the noise, and potentially the power. In the implementation of the shorter shaping time front-end, one would extrapolate from the current use of Silicon bipolar technologies in ATLAS to newly developed SiGe technologies developed for the communications industry, which afford lower power and lower noise solutions to the bipolar front-end [5].

E. CONCLUSIONS

Existing and soon to be operational silicon strip trackers achieve hit time resolution of 30% of the clock period. For a 100 MHz clock, this translates into 3 ns time resolution. There is an expectation that the time resolution on a track can be improved to 1.5 ns by phasing of the clock to different layers.

F. REFERENCES:

[1] G. Lynch: http://costard.lbl.gov/~grl/SvtTime/SvtTimeCalibration.html
http://costard.lbl.gov/~grl/SvtTime/SvtTimeCalibration2.html

[2] 1999 SCT week:
http://atlas.web.cern.ch/Atlas/GROUPS/INNER_DETECTOR/SCT/meetings/hmoser/sct_week_sep99_program.txt

[3] H. F.-W Sadrozinski: http://rd50.web.cern.ch/RD50/4th-workshop/

[4] M. Swartz: Pulse shapes in silicon detectors at different bias voltages, (private communication)

[5] D.E. Dorfan et al.: Investigation of the SiGe Process for Applications in Particle Physics, ADR proposal to DoE.

Table 1: Timing Characteristics of several Silicon Strip Detector Systems

	Babar [1]	**ATLAS** [2]	**SSTSiT** [3]
Clock Period T [ns]	67	25	10
Shaping Time τ_S [ns]	100 {400}	22	10
Hole Collection Time τ_C [ns]	25	14	7
Electron Collection Time τ_C [ns]	8	5	2.5
Charge Measurement	ToT	no	no (?)
Hit resolution σ_H [ns]	20	8	3
Track resolution σ_T [ns]	6-7	8	1.5 - 3

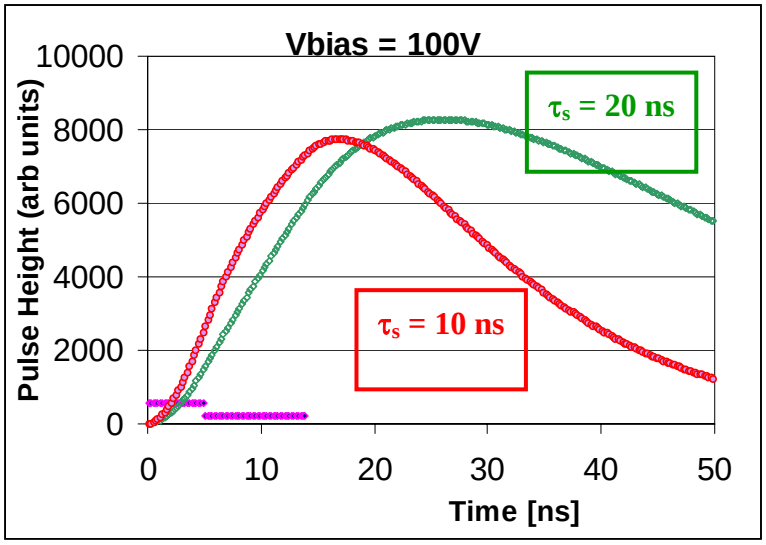

Fig. 1 Pulse shapes with 10 ns and 20 ns RC-CR shaping times. At 100V bias, the electrons are collected in 5 ns, and the holes in 14 ns.

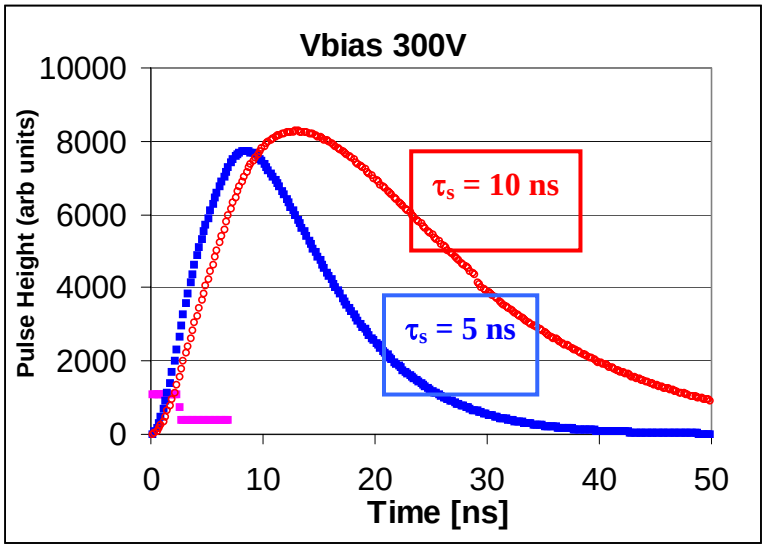

Fig. 2 Pulse shapes with 5 ns and 10 ns RC-CR shaping times. At 300V bias, the electrons are collected in 2.5 ns, and the holes in 7 ns.