

Tracking Detectors for the sLHC, the LHC Upgrade

Hartmut F.-W. Sadrozinski and Abraham Seiden
SCIPP, UC Santa Cruz, CA 95064 USA

Abstract

The plans for an upgrade of the Large Hadron Collider LHC to the the Super-LHC (sLHC) are reviewed, with special consideration of the environment for the inner tracking system. A straw-man detector upgrade for ATLAS is presented, which is motivated by the varying radiation levels as a function of radius, and choices for detector geometries and technologies proposed, based on the environmental constraints.

A few promising technologies for detectors are discussed, both for sensors and for the associated front-end electronics. On-going research in silicon detectors and in ASIC technologies will be crucial for the success of the upgrade.

1. Introduction

While the production phase for the LHC detectors is in full swing, a program for a future upgrade of the LHC is taking shape [1]. Machine studies have shown that a 10 fold luminosity increase might be possible, extending the physics reach of the LHC significantly [2]. Given that it will take close to 10 years to develop a new detector from concept to switch-on, the planning has started for an upgrade to be ready for data taking in the 2015 time scale.

2. The LHC machine upgrade

The LHC machine will have first beam collisions in Spring 2007. Depending on the evolution of the machine, with a luminosity from 3 up to 10 times $10^{33} \text{ cm}^{-2} \text{ s}^{-1}$, each experiment could collect 200-300 fb^{-1} in the following 5-6 years time.

Two LHC upgrade options are presently discussed/studied [2] (Table 1):

a) Higher luminosity $L \sim 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$

This upgrade needs changes in the machine and particularly in the detectors, with the sLHC mode starting some time in 2013-2016. One would collect $\sim 2500 \text{ fb}^{-1}$ per experiment in 3-4 years of data taking.

b) Higher energy

The LHC can reach $\sqrt{s} = 14 \text{ TeV}$ with the present 9 Tesla magnets. An energy increase to \sqrt{s} of 28 (25) TeV needs ~ 17 (15) T magnets, which would require extensive R&D and a costly rebuilding of the machine, and is thus less likely to occur in the near time scale.

Thus one could envision 3 main phases for the LHC upgrade, as shown in Table 1.

3. Goals for the sLHC upgrades

A practical view of the LHC upgrade is that it will be a necessity if the LHC science potential is to be exploited to the fullest. By the year 2015, the LHC detectors will have

seen 8 years of beams and parts of them will need to be replaced because of radiation damage. In addition, the potential for further discovery at the LHC will have been reduced. This can be measured by the time needed to halve the statistical error of the data: in 2012, after only two years at full luminosity, the time to halve the statistical errors will be 8 years [3].

Assuming that the machine upgrade happens in 2013-2014, where the time to halve the error becomes very large, one starts in 2015 with a luminosity ramp which brings this number down to a few years before reaching 7 years in 2018.

For the detector upgrades, an R&D program needs to start in 2004 lasting until 2009, followed by construction in 2010 to 2013, and installation in 2014. This is already very aggressive based on the LHC experience.

In summary, the LHC luminosity upgrade to $10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ (sLHC) allows to extend the LHC discovery mass/scale range by 25-30% [1] and extends the LHC program in an efficient way into the 2020 era.

4. Issues for the detector upgrades

The LHC detectors and electronics have been optimized for a luminosity of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and attempting to extend the operation to $10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ will cause severe problems for all of the subsystems.

The structure of the physics events are determined by the center-of-mass energy and will not change, while the backgrounds from minimum bias events will increase by a factor 10 (Table 2). A potential helpful feature might be a shortened bunch spacing in phase 1 of the upgrade from 25 ns to 12.5 ns. If the tracking systems can exploit this by shortening the shaping times, then the occupancies will increase “only” by a factor of 5. Recently there have been studies, which cast into doubt the possibility of the shortened bunch spacing, potentially making this a moot point [5].

Faced with the prospects of a much more difficult experimental problem, the two large experiments have started to investigate detector upgrade scenarios in workshops [6], [7]. There seems to be a clear immediate consensus about a number of goals for the upgrades. The upgraded detectors should provide the same detector performance at the sLHC as at the LHC. This is governed by the need to detect rare modes such as $H \rightarrow \mu\mu$, $H \rightarrow Z\gamma$, Z_L-Z_L . The detector reliability will have to be very high. Detector elements and electronics sufficiently rad-hard have to be able to run for long periods at the luminosity of $10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ ($\sim 1,000 \text{ fb}^{-1}/\text{yr}$), without replacement of components on the one year time scale.

Thus the detector upgrades will have to be preceded by detailed simulations of the radiation environment, although for the present analysis a simple scaling-up of the environment based on the LHC case provides a first good look at what to expect.

5. Issues for the ATLAS upgrades

For ATLAS [8], [9], [10] an upgrade means a replacement of the entire Inner Detector (ID): the Transition Radiation Tracker (TRT) at large radius will have prohibitively large occupancy, and the Semiconductor Tracker (SCT) and Pixel System at smaller radii will have reduced performance because of radiation damage to the sensors and front-end

electronics. The upgraded ID tracker would have about 200m^2 of semiconductor detectors, similar to the CMS inner detector [11], and ATLAS has to develop reliable assembly methods like CMS, which managed to develop identical systems at 7 sites to produce $\sim 20,000$ modules [12]. Because of the increased particle fluence, the search for rad-hard sensors will be of highest priority, coupled with an optimization of the detector layout with respect to the radius, and increased granularity, which might require increased multiplexing. A major constraint on the tracker is the existing ATLAS detector, implying a maximum radius of about 1m and a 2 Tesla magnetic field, and the limiting existing gaps for services. The outer silicon layers require more services than the TRT they are replacing, which means that for ATLAS the space available seems to preclude an increase in services due to granularity, implying that the multiplexing must be improved drastically [13].

6. Tracker Regions in the ATLAS Upgrade

The tracker layout is governed by two considerations due to the 10 fold increase in overlapping minimum bias events: a high instantaneous rate causing pile-up of tracks, and the integrated particle flux leading to radiation damage and nuclear activation.

6.1. Pile-up and Occupancy

At the LHC, occupancies and cluster merging are less severe (x2) in pile up events than in B-jets from Higgs decay. At the sLHC the situation is reversed by a factor 5. This requires adjustment of the detector geometry with radius, and one can scale from the SCT: a reduction of the detector length from 12 cm to 3 cm, at twice the radius, results in a factor 10 less occupancy. Or one could use 6 cm long detectors at twice the radius with 12.5 ns bucket timing, if this crossing time proves feasible

6.2. Straw-man Layout

Figure 1 shows the expected radial fluence distribution for a sLHC detector after an integrated luminosity of 2500fb^{-1} [14]. At a radius R of about 5cm, the fluence is about 10^{16}cm^{-2} , at 20cm, it decreases to about 10^{15}cm^{-2} , and at 50 cm it is about $2 \cdot 10^{14}\text{cm}^{-2}$. This suggests three different regions for a tracker with different technologies and layouts as indicated in Fig. 1 [15]: an Outer Region at $50\text{ cm} \leq R \leq 1\text{ m}$ where the present SCT technology can be used, a Middle Region (“Short Strips”) at $25\text{ cm} \leq R \leq 50\text{ cm}$, where present pixel detector technology might work, and an Inner Region (“Pixels”) at $6\text{ cm} \leq R \leq 12\text{ cm}$ requiring new sensor technology. The survival of the detector (and the electronics and optical readout) is a crucial issue [16- 25], and the suitability and availability of p-type substrates should be explored. Like the more expensive n-on-n detectors, n-on-p detectors would give head room in depletion voltage. They have no type inversion and allow operation with partially depleted sensors.

6.2.1. Region of Outer-Radius $R > 50\text{ cm}$

This region could be covered by 4 layers of “long strips”, and a single coordinate measurement might be adequate.

No sensor problems are expected for the outer region – if the detectors work at the LHC.

But the limited space for services for the outer region will require careful tradeoffs between detector length, front-end electronics power/noise and amount of multiplexing and granularity.

The present individual SCT modules used between 30 and 57 cm [10] will have to be replaced by a future ATLAS ID “stave” a la CMS [8] and CDF [26], which has the advantage that it permits, besides a reduction in the power and cable plant, assembly and testing of large sub-assemblies.

6.2.2. Region of Mid-Radius $20 \text{ cm} < R < 50 \text{ cm}$

This region would be covered by 4 layers of short strips providing space points. Scaling of the SCT rates allow a readout region of about $80 \mu\text{m} \times 1 \text{ cm}$, which is too coarse a z – measurement. The options are either very short strips (long-pixels) with dimension of order $80 \mu\text{m} \times 2 \text{ mm}$ [14], which requires a very large number of readout channels, or strips of longer ($\sim 3 \text{ cm}$) length, coupled with faster electronics and using small angle stereo for the z coordinate. With improved rise-time by a factor two (assuming that the machine crossing frequency is doubled) one reduces the occupancy by a factor of 4 due to the detector length and a factor of 2 due to the electronics wrt present SCT, compensating for the higher luminosity. Fig. 2 shows a possible layout of a short strip module, combining a pair of 3 cm long strip detectors on one 6 cm long wafer, with a hybrid with pairs of ASICs straddling the area between the strips like in the ATLAS SCT. Small-angle stereo arrangement as in the present SCT would provide sufficient resolution along the beam line ($\sigma_z < 1\text{mm}$), or one could use 2D Interleaved Stripixel Detectors (ISD) [27], which have a reduced signal-to-noise ratio S/N, but might work because of the shortened strip length. Confusion area in matching hits in the back-to-back stereo arranged detectors is proportional to the detector length squared. Thus, compared to the present SCT, confusion is reduced by factor of 16 due to reduced length and factor of 2 due to faster electronics, which represents an improvement wrt present ATLAS.

6.2.3. Inner Region: $R < 20\text{cm}$

Here 3 layers with pixel style readout at small radii would provide adequate pattern recognition. A very detailed layout of the pixel region for the upgraded CMS, including power consumption and cost, is provided in Ref. [14]. Again survival of the sensors is a main issue.

7. Specification of Sensor Performance

Based on present performance, (i.e. without drastic improvement of electronics), one can provide an initial specification of the collected charge needed in the three regions. This is shown in Table 3, which indicate that sensor technologies for both the outer and mid-radius regions are in hand, while the sensors for the inner regions will be limited by charge trapping during collection. They will require intensive R&D, and might be in need for new structures like 3-D detectors [25], [28].

8. Radiation Damage in Silicon Sensors

New measurement of the charge collection efficiency in 280 μm thick p-type SSD

has been reported [29]. After a fluence of high energy protons of $7.5 \cdot 10^{15}$ p/cm², the collected charge is 6,700 e⁻. This indicates that trapping times are about 2.4 times larger than extrapolated from previous measurements [4]. The fluence in this measurement corresponds to the one expected at the sLHC at a radius of about 10 cm (Fig. 1), and one might expect that the charge collection in planar silicon detectors at fairly high bias voltages might be sufficient for all but the inner-most pixel layer. At a radius of 20 cm, one would expect a collected charge of about 14,000 e⁻. For 3-D detectors [25], after $1 \cdot 10^{16}$ n/cm², the predicted charge collected is 9,000 e⁻.

9. Front-end electronics for sLHC

9.1. Material Challenge

Both ATLAS and CMS show large amounts of material in the tracking region, in excess of one radiation length in the $\eta = 1$ region. To reduce the amount of material will pose a challenge because most of the material is directly connected to the large number of electronics channels and the associated services. It was pointed out [30], [22] that in the CMS all-silicon strip tracker at the LHC, 10% of the material at $\eta = 1$ is from the active detector, 10% from the support structures and 80% due to the electronics (ASICs, hybrids, cables, fibers, cooling pipes). Thus reducing the number, size and power consumption of the electronics channels and increasing the multiplexing to reduce the number of cables and cooling pipes will be an important aspect of the tracker upgrades.

9.2. Front-end Electronics

The deep sub-micron DSM CMOS technologies used in pixel systems, and in most of the CMS detector is “accidentally” rad-hard and will provide a low-power solution for the front-end electronics of CMS upgrade [22]. Bipolar (BiCMOS) have shown to provide a power-noise advantage for large capacitances and fast shaping times, and show also excellent matching [31], but technologies used in ATLAS SCT are not sufficiently rad-hard beyond the LHC luminosity because the current gain β degrades from about 100 to about 40 at 10^{14} cm⁻², and their availability is limited. The newer BiCMOS technologies based on SiGe bipolar transistors are very fast ($f_T > 50$ GHz and $\beta > 200$). They are used widely in cell phones, and are available from IBM and through MOSIS “married” to a variety of DSM CMOS processes. Their radiation hardness has been measured to fluences of 10^{14} p/cm² [32] and when extrapolated up to 10^{15} cm⁻² seems to be adequate for the strip systems in the tracker upgrades: their advantage is that they start out with higher β and F_t than the old bipolar processes. It will be important to measure the radiation hardness up to the fluences required for the sLHC.

The largest area in the sLHC tracker will be made of long strips like the SCT, so SiGe could give an advantage, specially for short shaping times strips. Thus after careful simulations, first the layout should be optimized, then the optimal FEE technology should be selected, based on trade-offs of noise, power, speed and radiation hardness.

9.3. Single-Bucket Timing

If the luminosity increase for the sLHC is achieved by shortening the bunch length, the occupancy from minimum bias events can be reduced by a factor 2 if the hits and tracks can be associated with a single bunch crossing. If the rise time falls within the clock

cycle, single-bunch timing is possible in a straight forward way. The pulse rise time depends on both charge collection and shaping times. For the LHC where the detectors are normally biased at about 100V, the holes (electrons) are collected in 14 (5) ns. Increasing the bias to 300V, the collection time are reduced to 7 ns for holes and 2.5 ns for electrons, which together with a shaping time of 10ns, results in a rise time which falls within one bucket of the 80 MHz machine frequency. This might also be an attractive option for the upgrades of Belle [33] and Babar [34] or the LC [35], where fast timing would help reduce uncorrelated backgrounds [36].

10. Summary

The LHC luminosity upgrade to $10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ (sLHC) will allow to extend the LHC discovery mass scale range by 25-30% and extends the LHC program in a efficient way into the year 2020. The sLHC appears to give a good physics return for modest cost by getting the maximum out of the (by then) existing machine.

The sLHC will be a challenge for the experiments: detector R&D needs to start now to upgrade the Inner Tracker, especially if one wants to be ready to “go” soon after 2013/2014.

This R&D program needs to solve and overcome many issues and problems, and it will be important to apply “lessons learned” from past and existing experiments [37].

The path to the sLHC will be a mix between exciting R&D (rad-hard semiconductor detectors, low-power & fast FEE), sophisticated engineering (modules, cooling, data transmission) and “pedestrian” civil engineering (how to find space for cables).

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Table 1 Phases of LHC upgrades

LHC Phase	CM Energy \sqrt{s} [TeV]	Luminosity [$10^{34} \text{ cm}^{-2} \text{ s}^{-1}$]	Changes wrt LHC	Hardware changes
LHC	14	1	n.a.	
sLHC 0	14	2.3	Beam current	I.R.
sLHC 1	14	5 - 10	Bunch spacing, β^*	Final focus
sLHC 2	25	10?	Higher B-field	Magnets 9T -> 15T

Table 2: Predicted Detector Environment at the LHC and sLHC

	LHC	sLHC
\sqrt{s} [TeV]	14	14
Luminosity [$\text{cm}^{-2} \text{ s}^{-1}$]	10^{34}	10^{35}
Bunch spacing Δt [ns]	25	12.5/25
σ_{pp} (inelastic) [mb]	~ 80	~ 80
# interactions/x-ing	~ 20	$\sim 100/200$
$dN_{ch}/d\eta$ per x-ing	~ 150	$\sim 750/1500$
$\langle E_T \rangle$ charg. Part. [MeV]	~ 450	~ 450
Tracker occupancy *	1	5/10
Dose central region *	1	10
LAr Pileup Noise [MeV]	300	950
μ Counting Rate [kHz]	1	10

* Normalized to LHC values: 10^4 Gy/year R=25 cm

Table 3: Performance Specification of the Upgrade Tracker

Radius [cm]	Fluence [cm^{-2}]	Specification for Collected Signal (CCE in 300 μm)	Limitation due to	Detector Technology
> 50	10^{14}	20 ke $^-$ (~100%)	Leakage Current	“present” LHC SCT Technology, “long” strips
20 - 50	10^{15}	10 ke $^-$ (~50%)	Depletion Voltage	“present” LHC Pixel Technology ? “short” strips -”long” pixels
< 20	10^{16}	5 ke $^-$ (~20%)	Trapping Time	RD50 - RD39 - RD42 Technology 3-D

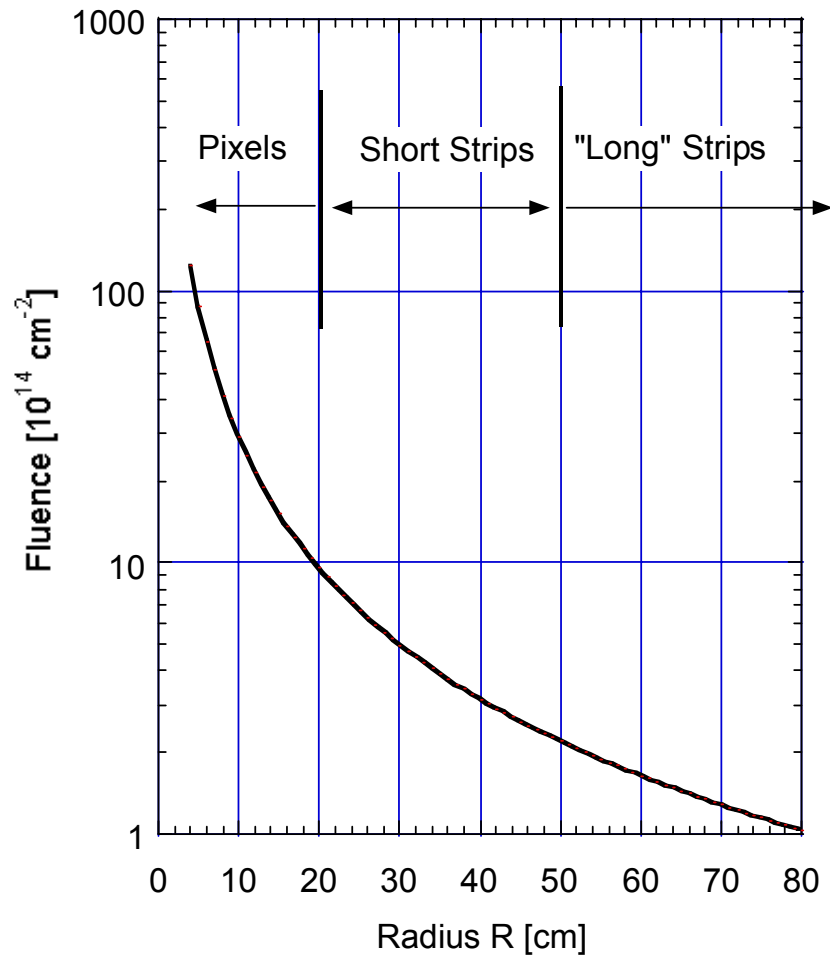


Fig. 1 Fluence as a function of radius R for an integrated luminosity of 2500 fb^{-1} [14]. The radial extend of the proposed tracker regions are indicated.

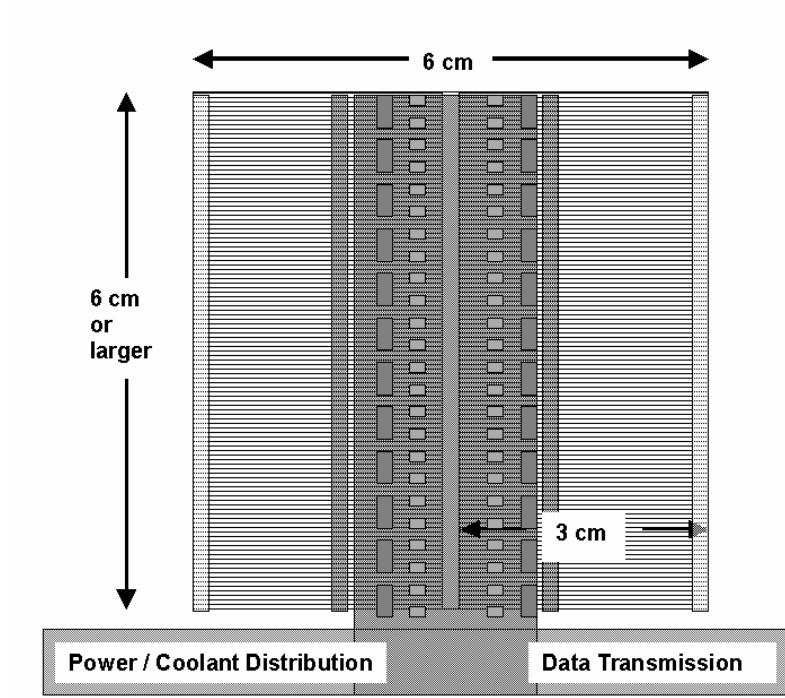


Fig. 2 Schematic layout of a short-strip module