SCIPP-04/03

# Characterization the Front-End electronics in order to Calibrate the PTSM

Completed by:

**John Wray**

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Dr. H.F.W. Sadrozinski

ABSTRACT:

The Proton Tracking Silicone Microscope (PTSM) is being developed as a future generation of medical imaging devices. Protons are used as a probe for imaging on a molecular scale with the use of a new type of detector, the Silicon Strip Detector (SSD). In order to characterize the Front-End electronics of the PTSM, data was collected on the gain of the system. This was done using known quantities such as: an input voltage, the value of the capacitance in the calibration bus, and the threshold voltage. To measure the threshold voltage, a constant input voltage was set; then in anticipation of fifty percent occupancy the threshold voltage was varied. The fifty percent occupancy point is used to average out the noise of the system. The width of the threshold curve is measured as the TOT, and was done by varying the input voltage and holding constant the threshold voltage, and again using the fifty percent occupancy point. A gain curve was assembled; the curve results in a linear relationship between the threshold voltage and the charge from the calibration bus.

INTRODUCTION:

The Particle Tracking Silicon Microscope (PTSM) is based on a detector developed for the GLAST collaboration. The silicon strip detector (SSD) for the GLAST project is very similar to the detector used in the PTSM only the application is much different. The SSD in the PTSM is used to track the position and energy of the incoming high-energy particle.

Bethe and Bloch discovered that charged particles interact with matter in a very predictable way. In fact, one of the reasons the PTSM project uses protons as the charged particle is because, as Bethe and Bloch found, the energy loss of charged particles is proportional to the changes in density of the material along the protons path.

In order to characterize the energy of the proton, the PTSM system uses a value known as Time Over Threshold (TOT). The TOT is measured by the PTSM Front-End (FE) electronics. The value of TOT is the time that the comparator stage of FE measures while the voltage of the strip is over the threshold voltage. The position is calculated by using two SSDs at a ninety-degree angle to each other. A good position reading is characterized as a single particle passing through both SSDs in the correct sequence, i.e. the particle passes though SSD #1 and then SSD #2.

The specifics of this report are concerned with characterizing the gain of the FE in order to calibrate the PTSM. The reason that we need to characterize the FE is because we want to know the exact relationship between the TOT vs. input charge. In essence the FE takes in a charge from the SSDs or in our case a charge from the calibration buses and creates a digital output signal that the can be read out by a computer. The process of characterizing the FE will be done by explanation of what the gain curve means in our case and then how the characterization helps calibrate the PTSM.

EXPERIMENTAL METHODS:

Two types of data were collected. The first was data concerning $V_{th}$ vs. $V_{in}$. The second type of data was pertaining to TOT vs. $V_{in}$. The experiment also lends it self to calculating the charge required for a particular TOT or $V_{th}$. Both types of data we collected using the fifty percent occupancy point because at this point the noise of the system will not give us an inflated or deflated reading of TOT or $V_{th}$.

The $V_{th}$ vs. $V_{in}$ data was collected using the following equipment; a voltage pulser, used for $V_{in}$, a constant voltage power supply, used for the $V_{th}$, the Xilinx board which contains the FE chip, and lastly an oscilloscope. The pulser was connected to an attenuator that divides the signal amplitude by a factor of four. This divided amplitude is comparable to what might be seen from an SSD. After the attenuator, a connection was made to the oscilloscope. Then a connection was made from the oscilloscope to the Xilinx board via the calibration buses. The calibration buses each contain a 50 fC capacitor, which is then internally connected to the beginning of the FE. The FE chip has three main components; first is the transconductance amplifier, which changes the charge from the capacitor back in to a voltage. Next in line is the shaper, which optimizes the signal shape depending on the type of noise from the system. The last part of the FE is the comparator, which has a two-pronged input. The comparator takes the signal originally produced in the transconductance amplifier and compares it to a supplied constant voltage, generally called the threshold voltage. From the comparator a digital signal is sent to out as either a logical yes or no, meaning that the input voltage was over threshold (yes) or it was not (no). The threshold voltage was held constant on a power source that was connected to the FE at the comparator stage. The input voltage and threshold voltage were set with the intention of a fifty percent occupancy reading on the oscilloscope. In doing this for a number of different input voltages, the outcome was data that is graphed in fig.1.

TOT vs. $V_{in}$ was calculated in a similar way. During this experiment, the threshold voltage was held constant at 101 mV. The TOT was read out from the FE on the oscilloscope. TOT is described as the duration of time that the comparator was above this constant threshold voltage. The input voltage was varied to give us a set of readings from which we can begin to characterize the internal electronics of the FE.

RESULTS:

The two graphs below were created using Microsoft Excel. These graphs are usefulness because of what they tell us about how the internal electronics shape the analog signal from the calibration bus (or SSD) into the digital signal, which is eventually readout on the computer.

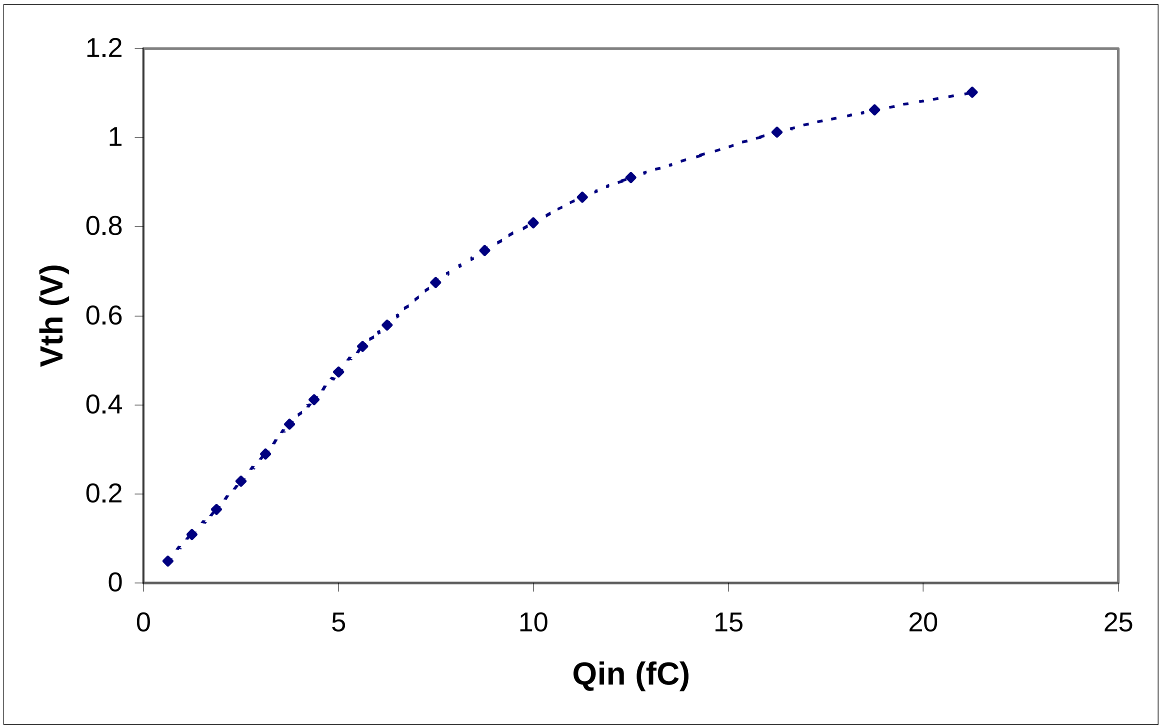


fig.1: Gain Curve for PMFE with $V_{th}$ (V) vs. $Q_{in}$ (fC)

The gain curve is important because this curve relates the input of the FE to the output. This relation is key to the characterization of the Front-End electronics in order to optimize the threshold voltage. This optimization will allow further experiments on the detection aspect of the PTSM to be as accurate as possible.

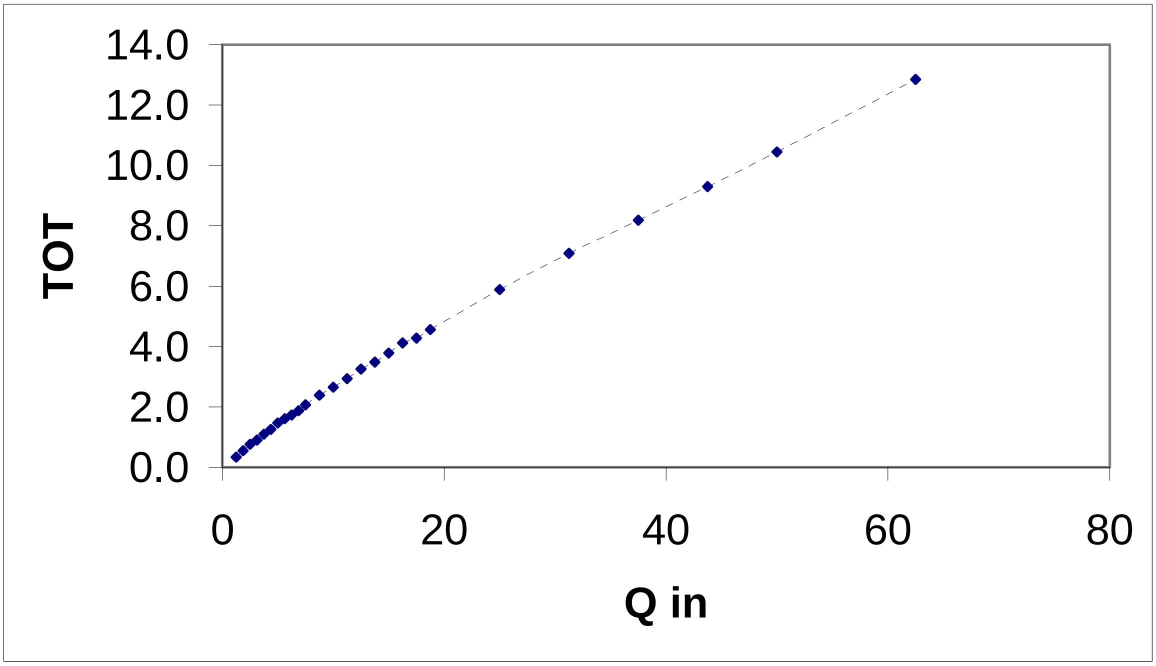


fig.2: TOT (μs) vs. $Q_{in}$ (fC)

The curve in fig.2 is important in showing how the input charge is related to the TOT. Once the optimum threshold voltage is discovered a graph, similar to fig.2, can be generated in order to experiment on the differing values of TOT received from the SSD.

It is observable that both graphs are nearly linear, which tells us that the system lacks any unforeseen electronic signals interfering with the processing of the TOT or threshold voltage.

CONCLUSION:

The results are very nearly exactly, what was expected. The only results that need more study are the data points at the end of fig. 1. At the end of the gain curve an unexpected pick up was detected.

A further study is also needed to extend the gain curve to a point of saturation. Saturation will occur when the gain curve begin to flatten out horizontally. This can be done by the use of an external capacitor, adding to the value of the internal capacitor.

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