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Beam Test of Silicon Detectors with Binary Readout for ATLAS

J. DeWitt, D. E. Dorfan, T. Dubbs, A. A. Grillo, S. Kashigin, W. Kroeger,
T. Pulliam, J. Rahn, W. A. Rowe, H. F.-W. Sadrozinski , A. Seiden,
E. Spencer, A. Webster, R. Wichmann, M. Wilder, D. Williams
SCIPP, Univ. of California, Santa Cruz, CA, USA

J. Dane, A. Lankford, S. Pier, B. Schmid
Univ. of California, Irvine, CA, USA

R. Bonino, C. Couyoumtzelis, P. Demierre
Univ. of Geneva, Geneva, Switzerland

Y. Iwata, T. Ohsugi
Hiroshima Univ., Hiroshima, Japan

H. Iwasaki, T. Kondo, S. Terada, Y. Unno
KEK, Tsukuba, Japan

W. Dabrowski, M. Idzik
IPNT, Krakow, Poland

J. Godlewski
INP, Krakow, Poland

R. Takashima
Kyoto Univ. of Education, Kyoto, Japan

A. Ciocio, T. Collins, J. Emes, M.G.D. Gilchriese, C. Haber , I. Kipnis,
M. Shapiro, J. Siegrist, H. Spieler
Lawrence Berkeley National Laboratory, Berkeley, CA, USA

N. Tamura
Okayama Univ. , Okayama, Japan

A. Grewal, R. Nickerson, R. Wastie
Oxford Univ. , Oxford, UK

Y. Gao, S. Gonzalez, A M. Walsh, Z. Feng
Univ. of Wisconsin,, Madison, WI, USA

ABSTRACT

We report results from a beam test of the binary silicon strip system for ATLAS. The data were collected during the H8 beam test at CERN in August/September 1995. The binary modules tested had been assembled from silicon micro strip detectors of different layout and from front-end electronics chips of different architecture. The efficiency, noise occupancy and position resolution were determined as a function of the threshold setting for various bias voltages and angles of incidence. In particular, the high spatial resolution of the beam telescope allowed the evaluation of the performance as a function of the track location in-between detector strips.

INTRODUCTION

We are proposing to simplify the readout of silicon detectors in the Semiconductor Tracking Detector (SCT) [1] of ATLAS [2] by using a binary readout [3], which records only the addresses of strips with pulse height exceeding a fixed threshold value. Thus the pulse height will not be available directly during data taking. We have shown that the distribution of pulse heights can be recovered by varying the threshold and measuring the counting rate, which is the integral of the pulse height spectrum. Likewise, the noise can be determined from threshold scans without beams. It is important to note that the primary parameters of interest for a tracking device are not the signal and noise, but the single channel efficiency the position resolution, and the noise occupancy.

In the following, we report results from the 1995 ATLAS beam test in the H8 beam line in the CERN North Area. Previous beam tests at KEK [4,5] have shown low noise occupancy at the nominal threshold of 1fC and good efficiency even at higher thresholds. In H8, the use of the beam telescope with a resolution of a few microns allowed the investigation of the efficiency at a fine scale as a function of the inter strip location.

BEAM SET-UP

During the 1995 ATLAS beam test in the CERN H8 beam line [6], several silicon micro strip modules with binary readout were tested. Fig. 1 shows the schematic of the set-up during the September run: the x-y beam telescopes bracketed the binary modules, and allowed the location of tracks within the modules to 2-3micron in the horizontal and vertical directions. Two of the binary modules, called UCSC and DDR2, were held fixed, while the central one, called AT&T, was mounted on a rotary stage and could be rotated about an axis parallel to the strips. The distance between the x-y hodoscope planes was about 80cm, and between the binary modules of the order 5cm, respectively.

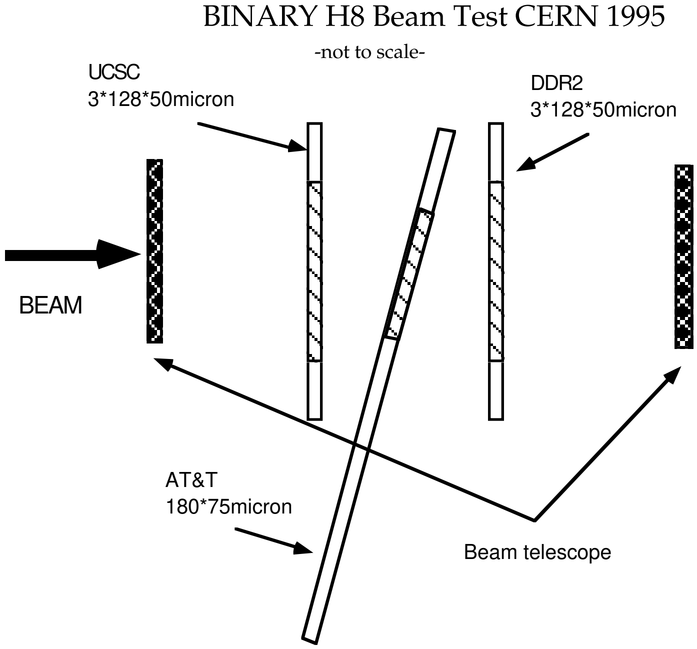


Fig. 1 Set-up of the binary H8 beam test in September 1995.
The shading areas indicate the active regions.

Table 1 lists the detector modules used in the September beam test. All modules are so-called "r-ϕ" modules, where the detector strips are directly bonded to the FEE. In addition, the hybrid, which carries the FEE and the data and control signals, is mounted across the detector strips in the approximate center of the 12cm silicon detector module.

The modules combined SSC-style and newly developed LHC-style detectors with different front-end electronics (FEE). Two bipolar amplifier-comparator chips with peaking time of close to 20ns were used. The LBIC [8] was developed for AC-coupled SSC detectors, while the CAFE [9] chip is designed for operation with finite input current for use with ATLAS DC-coupled detectors. Unfortunately the production run with AT&T yielded too few chips to instrument the full complement of modules. Two CMOS digital pipelines were used, the CDP128 [10] a clock-driven binary pipeline and the DDR2 [11] a data-driven binary pipeline with data compression and a data transmission protocol similar to the ATLAS protocol. Neither of the binary pipelines is edge sensing as required in the baseline design. Thus they sample the output width of the comparator chips, which is 2.5 clock cycles of 25ns for the DDR2 and AT&T3 modules and 0.6 clock cycles for the UCSC module. In order to assess the occupancies properly, they will be scaled in the following by the number of time slices the binary pipeline is "live".

The silicon detectors tested were AC-coupled double-sided detectors with 50μ pitch developed in Japan for the SSC [12] and DC-coupled ATLAS-type 75μ pitch detectors fabricated at LBNL [13]. Both Kapton flex-circuit and ceramic hybrids were successfully used, although the yield of Kapton circuits turned out to be extremely low.

Table 1: Binary r-ϕ Modules in the September H8 Beam Test

Tested Module	Hybrid	Detector [side,type,AC]			Pitch [micron]	Length [cm]	# of strips	Amp Chip	Pipe Line
UCSC	Kapton	n	n	AC	50	6,12	384	LBIC	CDP128
DDR2	Kapton	p	n	AC	50	6	384	LBIC	DDR2
AT&T3	Ceramic	n	p	DC	75	12	180	CAFE	CDP128

The read-out was newly developed for this test and is based on Digital Signal Processors (DSP's) utilizing a 40MHz clock. They were designed to allow a data rate of several kHz, but the data acquisition rate was limited by the readout speed of the telescope to about 100 counts per spill.

In addition to rotation scans, two parameters were varied to map out the performance of the detectors: the detector bias voltage and the threshold of the on-chip comparators. The results from the threshold scans are used to determine the pulse height. The data at different rotation angles help to understand the effects of a finite track crossing angle.

OCCUPANCY

Both the on-beam occupancy and the off-line noise occupancy were measured to verify that the modules were working as designed. The noise occupancy was measured as a function of the threshold voltage to determine the noise sigma's. This was done before and after the run using the full DAQ. Channels which were obviously noisy were removed from the data. 'The occupancy per channel as a function of threshold squared is shown in Fig. 2. The data have been corrected for the number of effective time slices of the 40MHz clock the comparator output level is sensed by the pipe-line, as explained above.

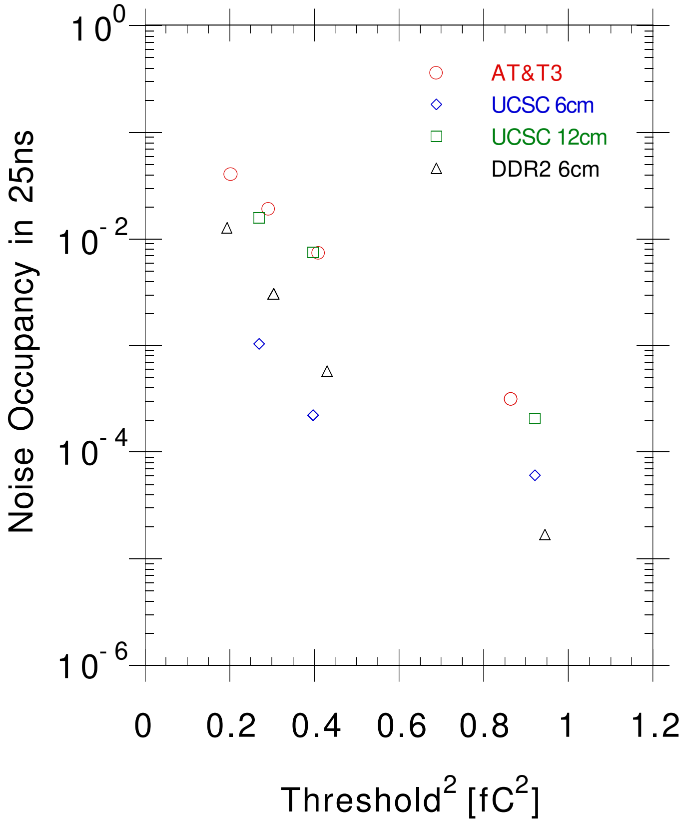


Fig. 2 Noise occupancy of the modules as a function of the threshold

The occupancies are approximate gaussian functions of the threshold voltage [14,15]. The slope is a measure of the noise sigma. We observe the expected dependence of the noise on the strip length (12cm vs 6cm). Table 2 shows the noise occupancies extrapolated to a threshold setting of 1fC.

Table 2: Noise Occupancy at 1fC Threshold for one 40MHz Time Slice

Module	Noise sigma [e^-]	Occupancy @ 1fC
AT&T3	1640	$0.8*10^{-4}$
UCSC, 12cm	1706	$1.5*10^{-4}$

It should be pointed out that the CAFE amplifier chips were operate on their lowest power setting which results in relatively higher noise levels. Even then the extrapolated noise occupancy at 1fC threshold is of the below 10^{-4}.

The on-beam occupancy was determined with the help of a tracking program simultaneously with the efficiency and will be discussed below.

DATA ANALYSIS

a) Event selection

Events were filtered from the DST into a 'mini-DST' by requiring one and only one track reconstructed in each event. For the analysis of a particular module, the projected telescope track was required to be in the fiducial region, defined as:

- the track impact point was not allowed to fall on a dead strip;
- the track impact point was required to be at least 15 strips away from edge in the x-coordinate (the axis perpendicular to the strips);
- the track impact point was required to be approx. 1 mm away from the edge in the y-coordinate, i.e. along the strips.

In addition to the above requirements, only events with a telescope track χ^2 value of less than 30 were kept.

b) Clustering

Before the clustering was done, the module readout order was fixed so that strip numbers are sequential. This fix basically consists of the swapping of even and odd strip numbers. Then clusters were constructed in the following way:

- a cluster seed was started up to +- 2 strips away from the track impact point;
- searches on the left and the right side of the impact point were done independently for hit strips;
- the search stopped when no more hit strips are found;
- all contiguous hits were then clustered.

The cluster position was then taken to be the average strip position for the strips in the cluster. In order to reduce biases in the clustering introduced by noisy or dead channels, events were further rejected if:

* a found cluster contained a hit on a strip flagged as 'noisy';

* the closest dead strip was less than 2 strips away from the expected hit strip.

Clusters and events that passed all the above requirements were then labeled 'good' clusters and 'good' events and were used in the efficiency and resolution measurements.

c) TDC Cuts

The trigger from scintillation counters was synchronized with the 40MHz readout clock and initiated the read-out of the pipelined data. The phase of the trigger and thus the arrival of the particles in the silicon detectors relative to the clock was determined by a TDC with 200ps resolution. At LHC, the data will arrive with a fixed phase relative to the clock; in H8, the arrival was spread over 25ns and the efficiency as a function of the TDC value had to be determined. We expect variations of the efficiency with the clock phase for the LBIC chip, which was designed for p-side detectors and has a very narrow pulse width for n-side detectors (UCSC module). Due to time walk in the comparator, the TDC distribution depends on the threshold, as shown in Fig. 3 for the UCSC module.

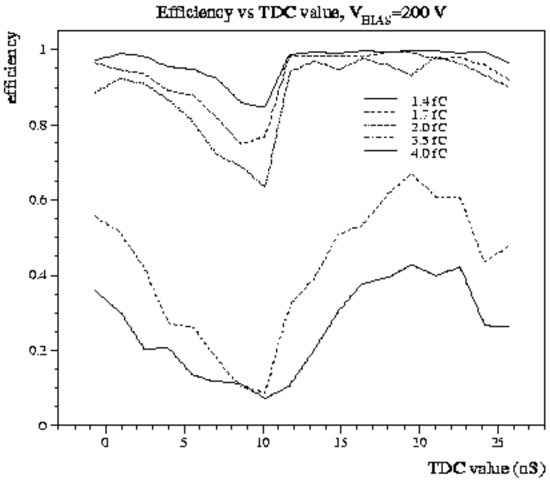


Fig. 3 Efficiency of the UCSC module as a function of the time difference between the trigger and the clock edge. The efficiencies for 1fC and 1.2 fC thresholds are constant and unity.

The data is independent of the TDC value for TDC(UCSC) > 15ns. Likewise for the DDR2 module, the time cut TDC(DDR2) <10.5ns was applied. For the AT&T3 modules which uses an amplifier-comparator chip with a more advanced design, no TDC cut was necessary. Missing or corrupted TDC information was an indication of DAQ problems and caused data runs to be excluded from analysis.

In the following we discuss a few selected results from the data analysis of the different modules.

RESULTS

a) Efficiency as a Function of Inter strip Position -DDR2-

The efficiency for the p-side detector read out with the DDR2 chip is shown in Fig. 4. The efficiency is above 99% even at a threshold 40% higher than the nominal 1fC. It is 50% at close to 3.5fC, the median of the binary Landau distribution.

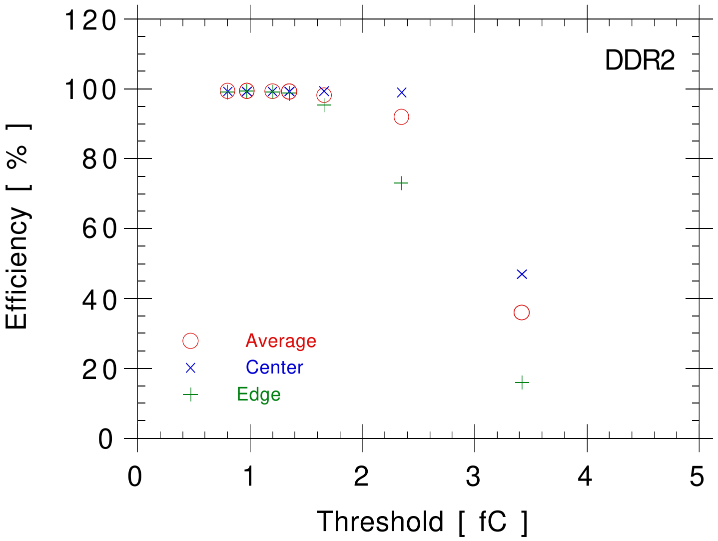


Fig. 4 Efficiency for the DDR2 module as a function of the threshold.

Further insight into the detector performance is gained from the dependence of the efficiency on the inter-strip position of the track. Fig. 5 shows the efficiency as a function of the extrapolated track position between two strips, in fractions of the pitch. The efficiency is shown for two thresholds, 1fC and 1.66fC.

As expected, the efficiency starts to degrade in between the strips first, where the charge sharing decreases the effective pulse height detected in a single strip.

In the middle between strips, the charge sharing causes higher hit multiplicities. In order to isolate the inter strip effects, we quote, in addition to the efficiencies averaged over all positions, two values for specific inter strip position, "edge", and "center" (see Fig. 5). "Edge" refers to the efficiency calculated in a 5micron wide bin at the edge of a strip, while "center" refers to the efficiency in a 5micron wide bin at the center of the strip. The values for edge and center are shown in Fig. 4 together with the average efficiency.

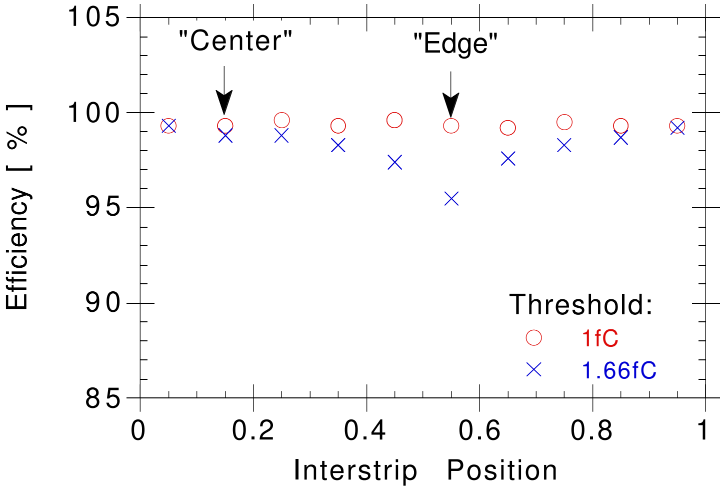
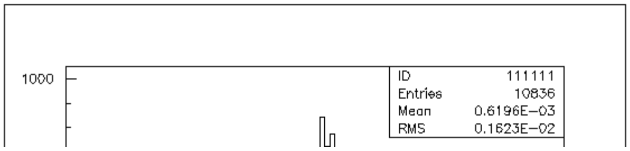


Fig. 5 Efficiency as a function of inter strip position for 1.0 and 1.66fC threshold.

Fig. 6 shows the tracking residuals at 1fC threshold. The distribution is composed of two contributions, one from single hit tracks with a resolution of close to pitch/√12= 14microns and one from multi-hit clusters, with a resolution of about half that.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