Beam Test of Silicon Detectors with Binary Readout for ATLAS

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Goals of the H8 Beam Test with Binary Modules:

6cm vs. 12cm modules

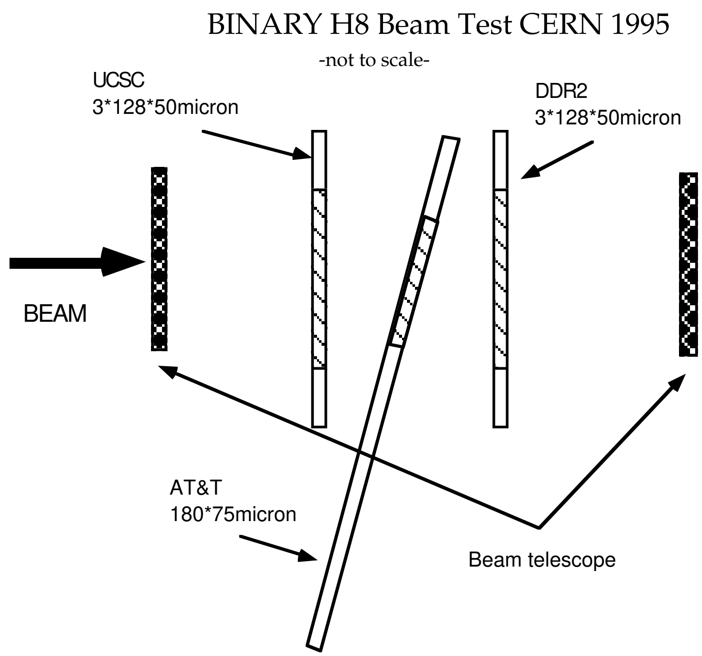
experience with: single-sided DC coupled operation
p-type detectors
ATLAS style FEE

trace out parameter space of binary modules by measuring

efficiency		threshold voltage
noise occupancy	as a function of	bias voltage
position resolution		angle of track incidence

profit from beam telescope with high spatial resolution to map out inter-strip effects

on-line monitoring



Binary r-ϕ Modules in the September H8 Beam Test

Tested Module	Hybrid	Detector [side,type,AC]			Pitch [micron]	Length [cm]	# of strips	Amp Chip	Pipe Line
UCSC	Kapton	n	n	AC	50	6,12	384	LBIC	CDP128
DDR2	Kapton	p	n	AC	50	6	384	LBIC	DDR2
AT&T3	Ceramic	n	p	DC	75	12	180	CAFE	CDP128

Data analysis

Anish Grewal (Oxford)

DDR2 module: inter-strip effects

AT$T3 module: track angle effects

Saul Gonzalez, Zhong Feng (Wisconsin)

UCSC module: bias voltage effects

Noise occupancy for all modules

(with the help of Bill Murray)

Tracks were fitted from space points in the beam hodoscope
and projected with a precision of about 3 microns into the binary modules

Only events with ONE track were accepted

Timing cut due to the limited overlap of the comparator output with the synchronized clock, as measured with TDC:

UCSC: 15-25ns

DDR2: 0-15ns

Available binary pipelines (CDP & DDR2) are level sensing.
Overlap of the comparator output level with the clocked pipe-line :

Module	FEE Chip	# of 25ns Time slices	Remark
AT&T3	CAFE	2.5	n- or p-side
DDR2	LBIC	2.5	p-side
UCSC	LBIC	0.6	n-side

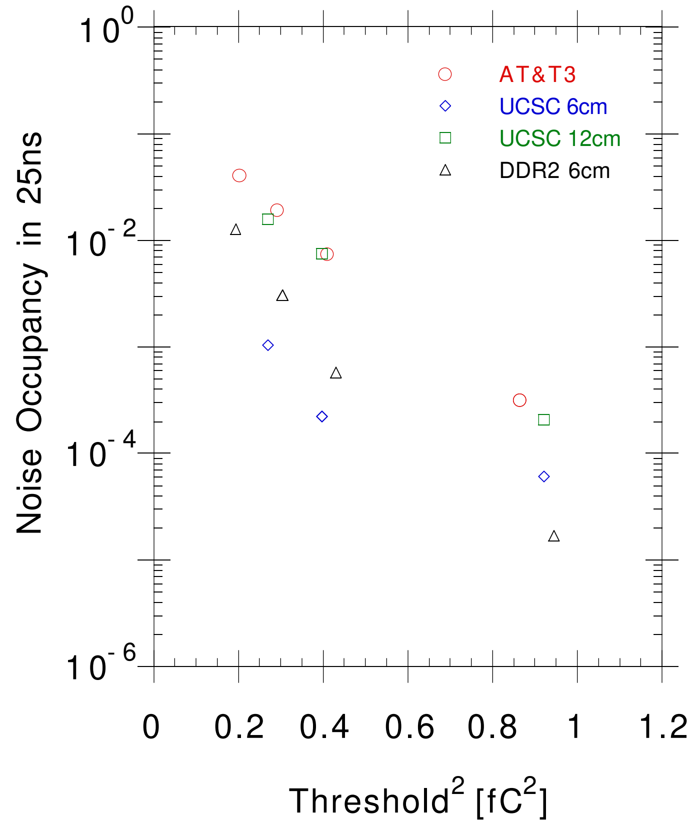
Occupancy were corrected to one 25ns time slice, corresponding to edge triggering.

Noise Occupancy

is a function of the operating threshold and is determined two ways:

off-track occupancy during on-beam data taking

noise occupancy during threshold scans



Noise occupancy has approximate Gaussian dependence on threshold V_t and noise sigma σ

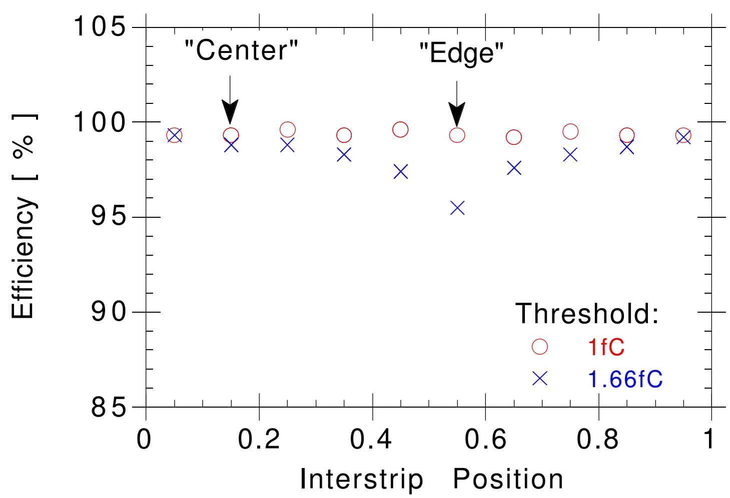
$$Occ = O_o \exp(-V_t^2/2\sigma^2)$$

Noise rms and Occupancy at 1fC Threshold for one 40MHz Time Slice

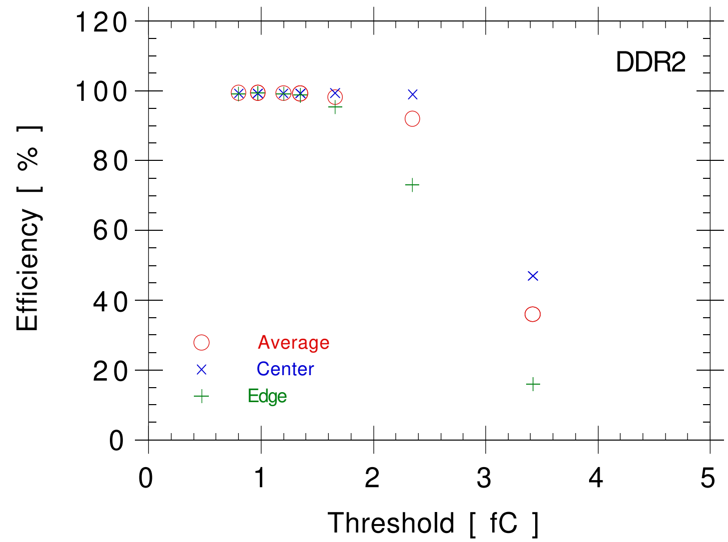
Module	Noise sigma [e^-]	Occupancy @ 1fC
AT&T3	1640	$0.8*10^{-4}$
UCSC, 12cm	1706	$1.5*10^{-4}$

Efficiency as a Function of Inter strip Position
DDR2- 6cm long, 50m pitch, p-side

Efficiency vs inter-strip position for 1.0 and 1.66fC



Efficiency vs threshold for average, center, edge



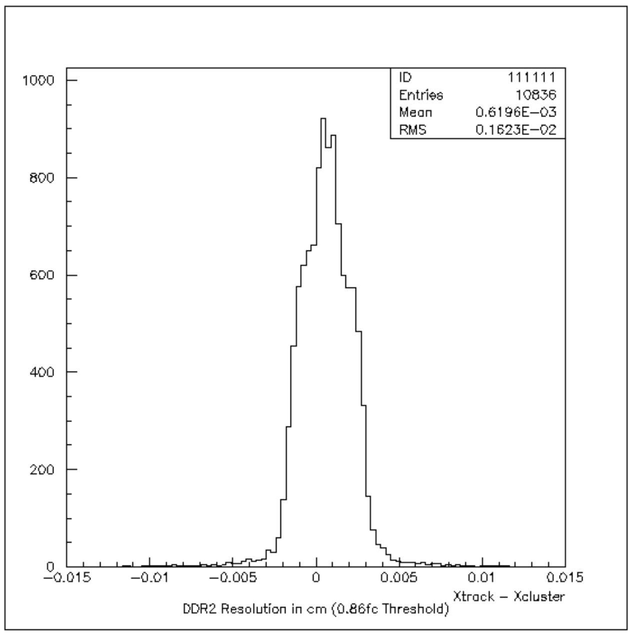
The efficiency is above 99% even at a threshold 40% higher than the nominal 1fC.

It is 50% at close to 3.5fC, the median of the binary Landau distribution.

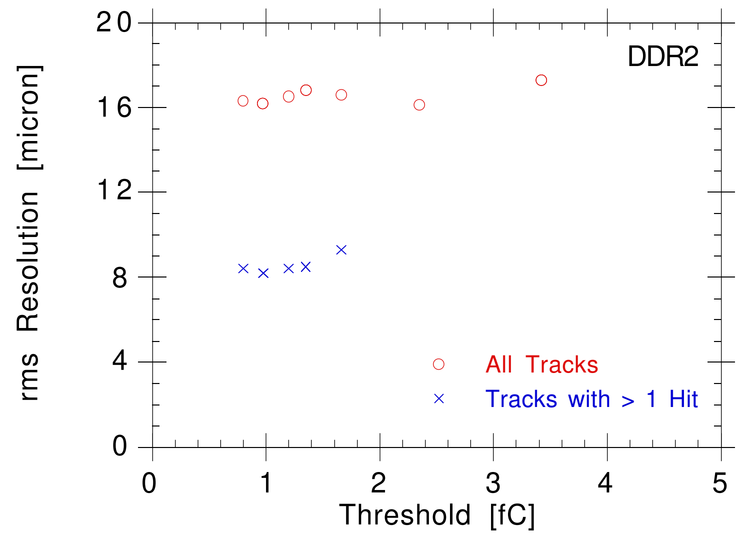
The "edge" of the strips, i.e. the 5μ bin in-between the strips is especially susceptible to efficiency losses due to charge sharing

Sharing of pulses causes

reduction of efficiency
but improves position resolution.



Track residuals



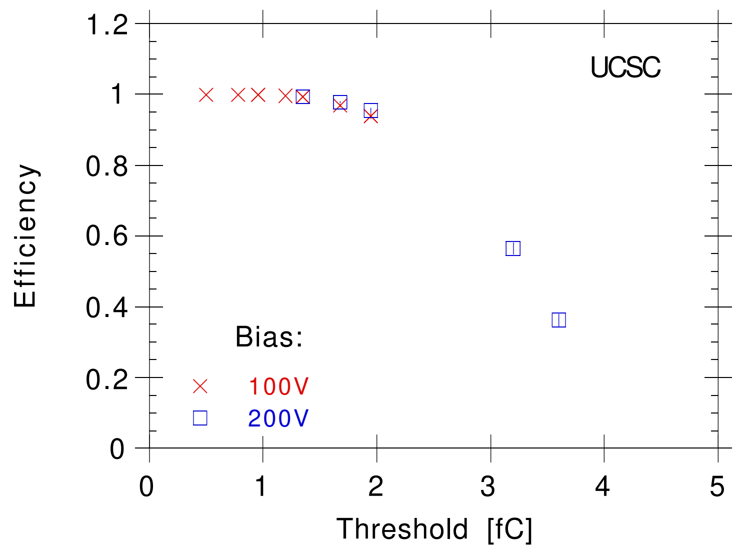
rms Resolution (fitted resolutions 20% lower)

Bias Voltage Dependence of the Efficiency and Position Resolution
UCSC- module, 12cm , 50μ, n-side

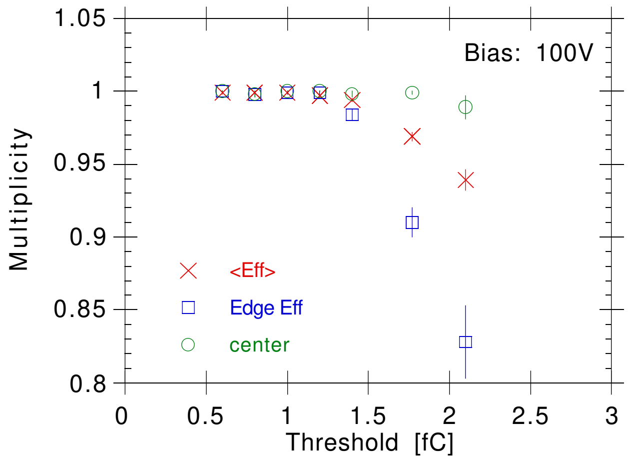
n-in-n detectors deplete from the backside before inversion,
the collection of charge might be less efficient at lower bias voltages than at higher ones.
The UCSC module depletes at about 70V.
We have operated the module at 100V and 200V bias,

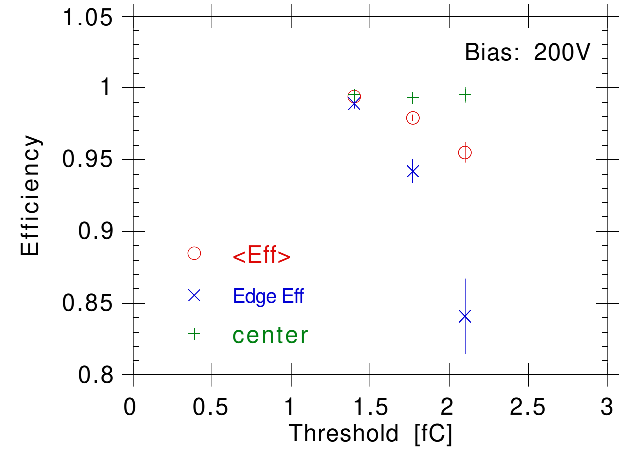
We found that noise improves when raising the bias voltage

Efficiency for two bias voltages:

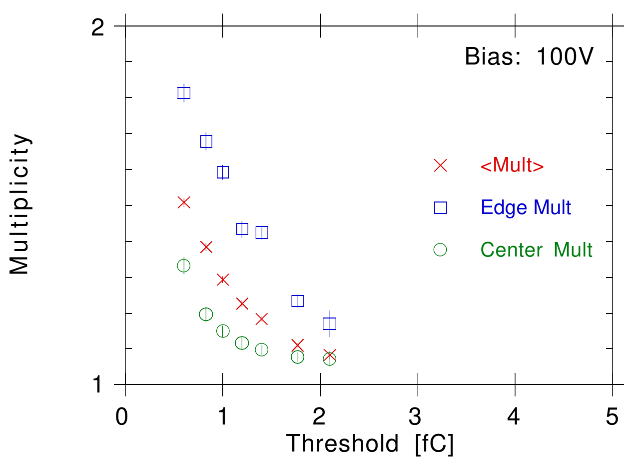


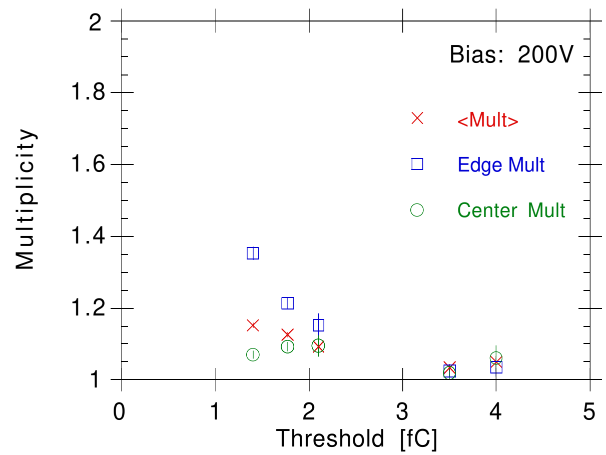
Efficiency close to nominal threshold for the UCSC module



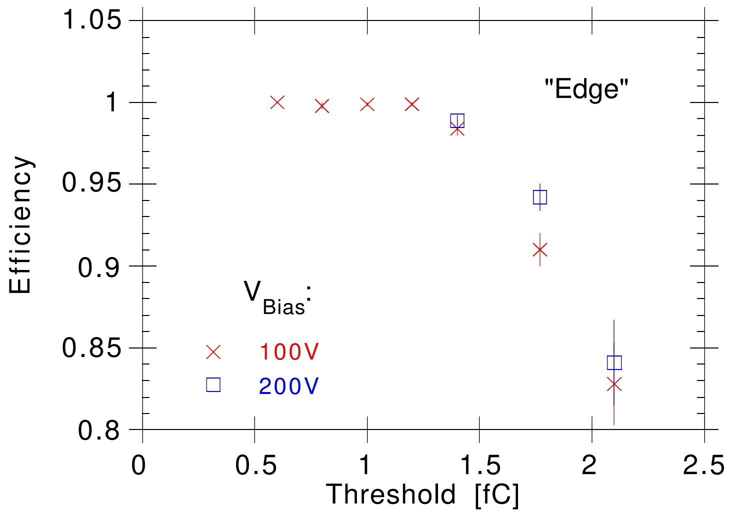


Hit multiplicity as a function of the threshold





Efficiency at the edge of the strip vs. threshold



No strong bias voltage effect close to the nominal threshold of 1fC,
only at 1.7fC, can we observe an increase in efficiency for the larger bias voltage.

Redo this measurement with 75m pitch detector

Efficiency Dependence on Rotation Angle -for under-depleted detector AT&T3 module- 12cm, 75μ pitch, n-on-p

n-on-p bulk detector has higher doping density than the n-bulk detectors

Depletion voltage about 150V,

bias voltage : 85V due to the large leakage current,

75% of the detector is depleted

Operation corresponds to an inverted n-on-n detector operated at partial depletion,

an option for the ATLAS SCT in case of unexpectedly high radiation levels

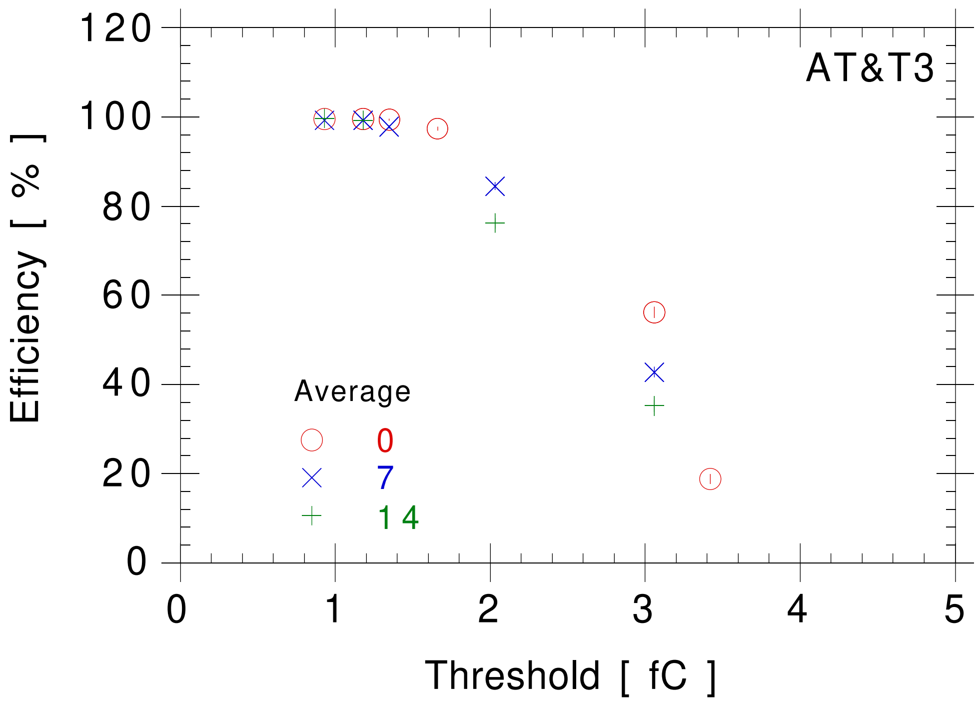
Rotation changes the angle of incidence of the track and the amount of sharing

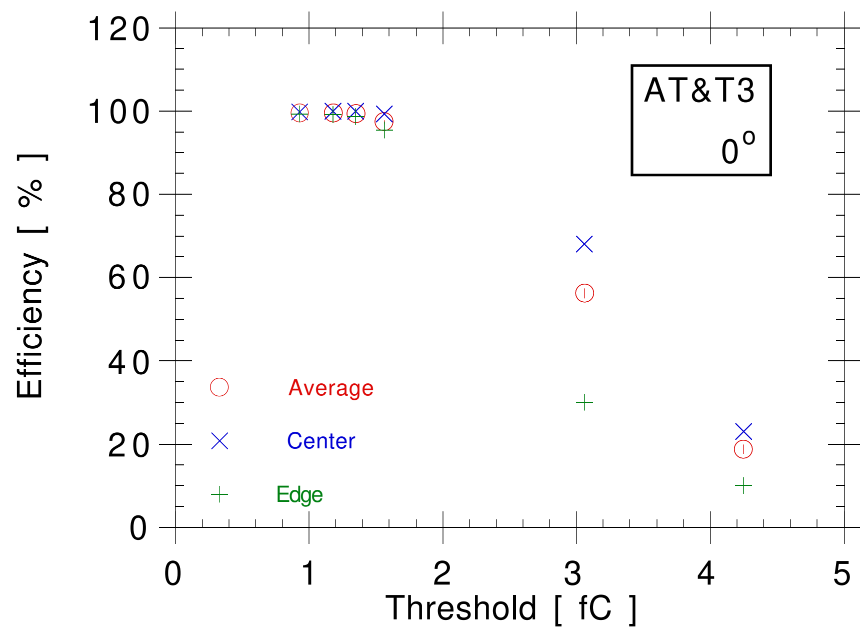
With the high precision tracking sensitivity to effects at the edge is increased

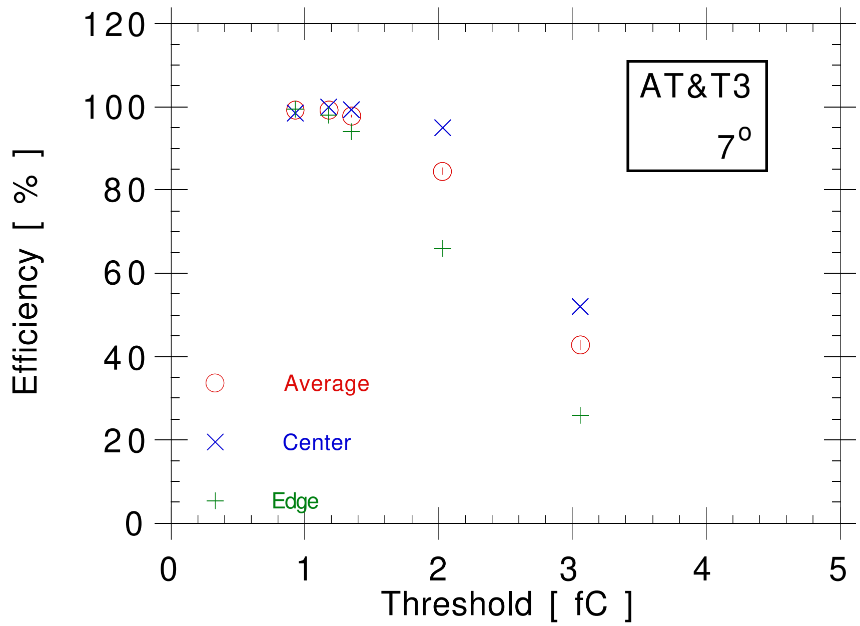
Ideally, one would like to study this as a function of bias voltage

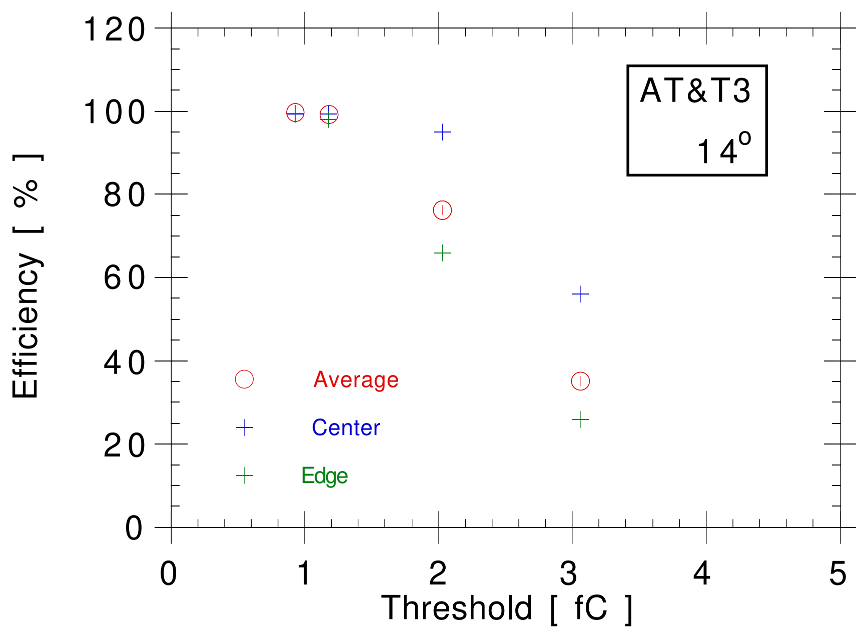
Angle of Incidence of Track changes Sharing between Strips

Efficiency for rotation angles 0° 7°, 14°




AT&T3
0°
Average
Center
Edge
Efficiency [%]
Threshold [fC]
0
20
40
60
80
100
120
1
2
3
4
5

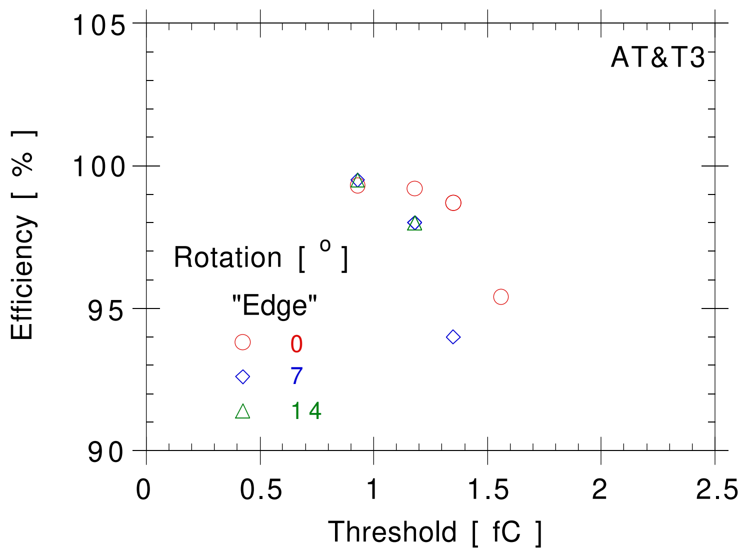

AT&T3
7°
Average
Center
Edge
Efficiency [%]
Threshold [fC]
0
20
40
60
80
100
120
0
1
2
3
4
5



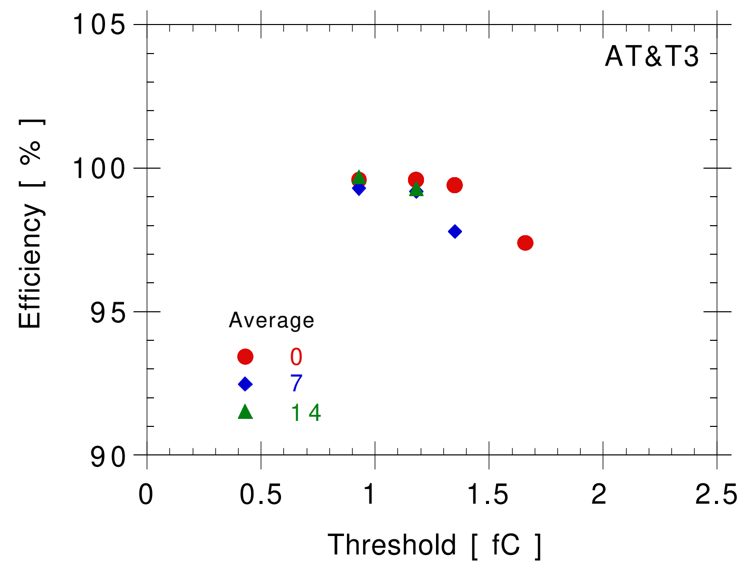
AT&T3
14°
Average
Center
Edge
Efficiency [%]
Threshold [fC]
0
20
40
60
80
100
120
0
1
2
3
4
5

Efficiency as a function of angle for

7.5µ Edge bin



average over 75µ strip



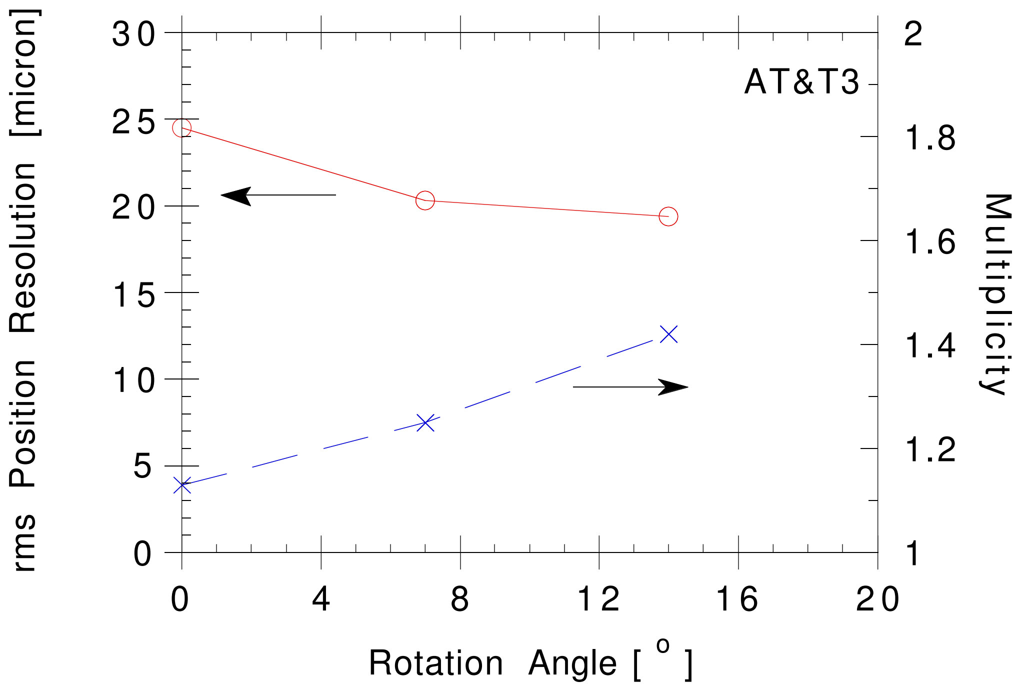
Observable effect at 7^o and 14^o, but insignificant in average at 1.2fC threshold

Efficiency at 7^o and 14^o look identical (?)

Noticeable efficiency loss at 1.4fC threshold , but average still 98% efficient (7^o only)^o

Really missed the 14^o at 1.4fC!

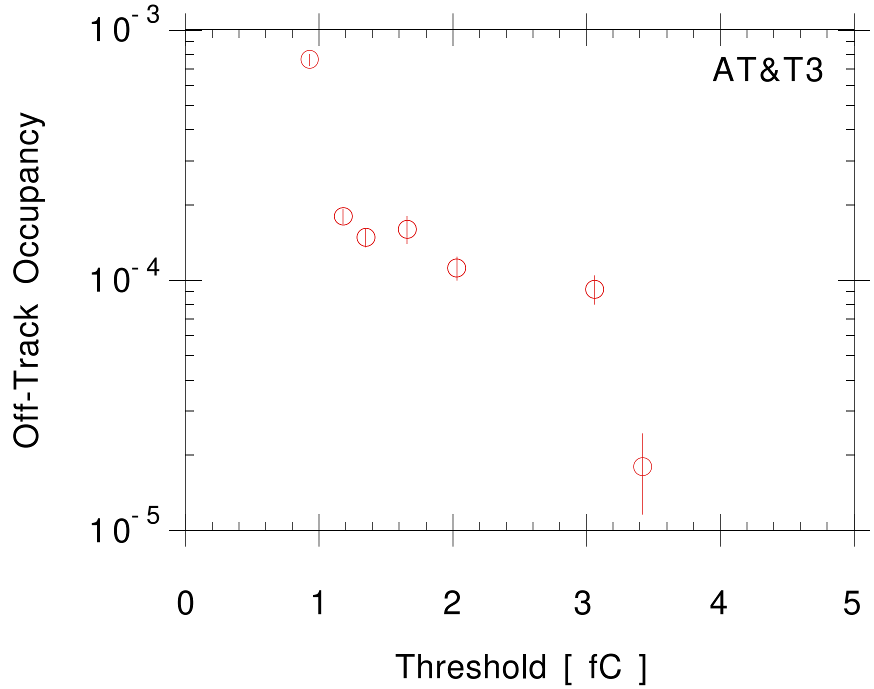
Position resolution and average multiplicity as a function of angle at a threshold of 1fC.



Larger rotation angle increases the sharing, multiplicity, improves position resolution

Off-track occupancy in one 25nsec time slice during beam-on time

all hits in the events which were distant by more than 10 strips from the track projection.

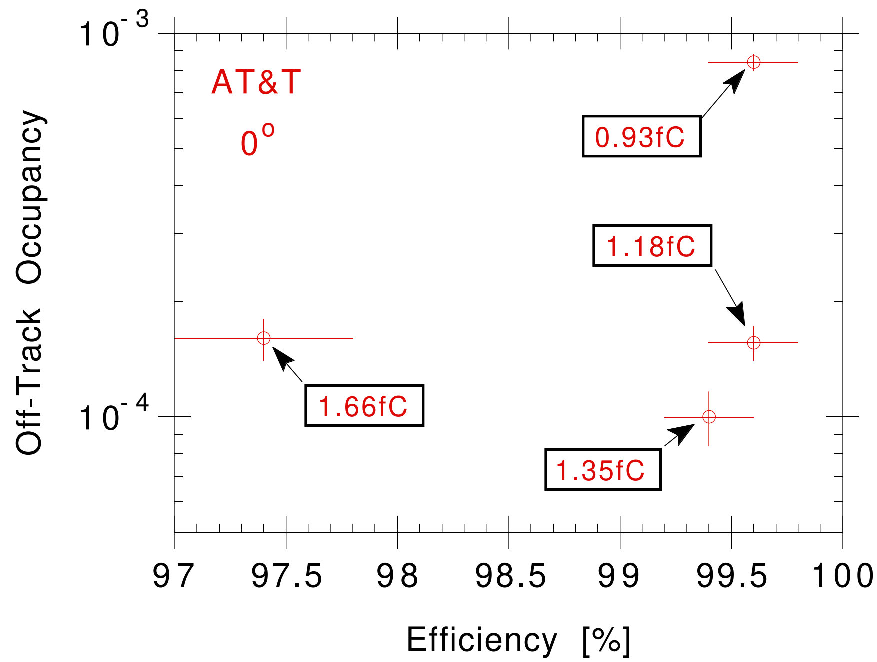


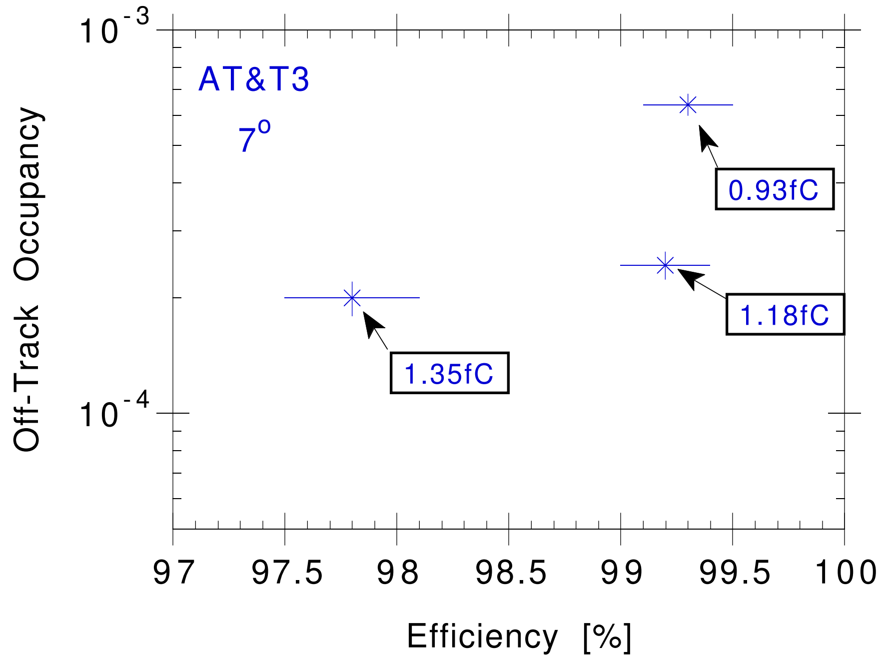
At a threshold of .93fC, the occupancy is due to random noise

At larger threshold, a long tail extending to large thresholds is observed.

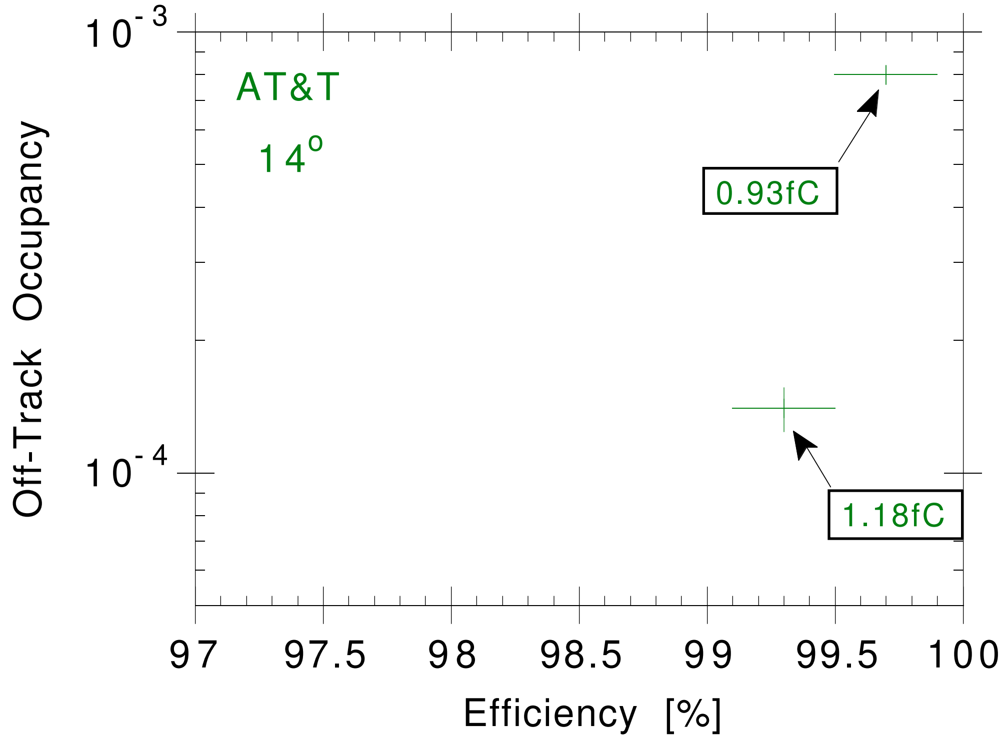
This tail is not observed in the bench noise studies.

A possible source are additional tracks in one event not recognized by the beam telescope, Off-Track Occupancy vs Efficiency for different Thresholds





AT&T3
7°
0.93fC
1.18fC
1.35fC
Off-Track Occupancy
Efficiency [%]
10^-3
10^-4
97
97.5
98
98.5
99
99.5
100



AT&T
14°
0.93fC
1.18fC
10^{-3}
10^{-4}
97
97.5
98
98.5
99
99.5
100
Efficiency [%]
Off-Track Occupancy

Lessons learned for operations of a binary SCT system:

Conditions: 12cm detectors with 75µ pitch,
bias at about 3/4 depletion,
FEE non-optimized.
Track angles up to 14°

Conclusions: Noise occupancy is acceptable at 0.9fC, is to specs above 1.0fC threshold (10^{-4})
Efficiency is acceptable at 1.4fC, to specs below 1.2fC (> 99%)

<u>The binary system will have a "head room" in the threshold setting of between 20% and 50%.</u>

This head room should be reserved for unexpected effects,
like higher than expected radiation levels
NOT for controllable spread in the performance of the FEE.

Need a tight specification of the threshold matching (gain & noise) for the bipolar chips
What can be achieved?
Part of the 10 wafers with the TEKZ chip for ZEUS, fabricated in the Tektronix -now MAXIM- bipolar process were tested thoroughly:
matching of the threshold at 1fC across 4 wafers (660 chips* 64channels) was 4%, corresponding to 25% of the noise rms.
We get away with one threshold for 55k channels, and a calibration once in a while.

For ATLAS, we most likely need to group chips with similar gain to keep the acceptable yield up.

Recommendations for the next binary H8 beam test:

keep the beam telescope!

operate CAFE with optimized power setting

redo measurements with irradiated n-on-n detectors,

operate at partial depletion, and large bias voltage

test twin module in pre-rad state simultaneously

include points at larger angles and at more thresholds (0.8, 0.9, 1.1, 1.4)

schedule a high flux run to investigate short term effects